NEC

MOS INTEGRATED CIRCUIT
μPD42S4170, 424170, 42S4270, 424270

4 M-BIT DYNAMIC RAM
256K-WORD BY 16-BIT, FAST PAGE MODE, BYTE WRITE MODE

DESCRIPTION

The μPD42S4170, 424170, 42S4270, 424270 are 262 144 words by 16 bits dynamic CMOS RAMs. The fast page mode and byte write mode capability realize high speed access and low power consumption.

Besides, the μPD42S4170, 42S4270 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh. Refresh cycles are 1 024 cycles on the μPD42S4170, 424170 and 512 cycles on the μPD42S4270, 424270.

These are packaged in 44-pin plastic TSOP, 40-pin plastic SOJ and 40-pin plastic ZIP (only for μPD42S4170, 424170).

FEATURES

- 262 144 words by 16 bits organization
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S4170-70	660.0 mW	70 ns	130 ns	45 ns
μPD424170-70				
μPD42S4170-80	577.5 mW	80 ns	150 ns	50 ns
μPD424170-80				
μPD42S4270-70	880.0 mW	70 ns	130 ns	45 ns
μPD424270-70				
μPD42S4270-80	797.5 mW	80 ns	150 ns	50 ns
μPD424270-80				
μPD42S4270-10	660.0 mW	100 ns	190 ns	65 ns
μPD424270-10				

- μPD42S4170, 42S4270 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4170	1 024 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.1 mW (CMOS level input)
μPD42S4270	512 cycles/128 ms		
μPD424170	1 024 cycles/ 16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μPD424270	512 cycles/ 8 ms		

The information in this document is subject to change without notice.

The mark ★ shows revised points.

Document No IC-2933A
(O D No IC-8477A)
Date Published March 1993 M
Printed in Japan

• Multiplexed address inputs

Part number	Row address	Column address
μPD42S4170, 424170	A0 to A9	A0 to A7
μPD42S4270, 424270	A0 to A8	A0 to A8

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S4170G5-70-7JF	70 ns	44-pin Plastic TSOP	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{RAS}$ only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh Hidden refresh
μPD42S4270G5-70-7JF			
μPD42S4170G5-80-7JF	80 ns		
μPD42S4270G5-80-7JF			
μPD42S4270G5-10-7JF	100 ns		
μPD42S4170G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD42S4270G5-70-7KF			
μPD42S4170G5-80-7KF	80 ns		
μPD42S4270G5-80-7KF			
μPD42S4270G5-10-7KF	100 ns		
μPD42S4170LE-70	70 ns	40-pin Plastic SOJ	
μPD42S4270LE-70			
μPD42S4170LE-80	80 ns		
μPD42S4270LE-80			
μPD42S4270LE-10	100 ns		
μPD42S4170V-70	70 ns	40-pin Plastic ZIP	
μPD42S4170V-80	80 ns		
μPD424170G5-70-7JF	70 ns	44-pin Plastic TSOP	$\overline{RAS}$ only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh Hidden refresh
μPD424270G5-70-7JF			
μPD424170G5-80-7JF	80 ns		
μPD424270G5-80-7JF			
μPD424270G5-10-7JF	100 ns		
μPD424170G5-70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD424270G5-70-7KF			
μPD424170G5-80-7KF	80 ns		
μPD424270G5-80-7KF			
μPD424270G5-10-7KF	100 ns		
μPD424170LE-70	70 ns	40-pin Plastic SOJ	
μPD424270LE-70			
μPD424170LE-80	80 ns		
μPD424270LE-80			
μPD424270LE-10	100 ns		
μPD424170V-70	70 ns	40-pin Plastic ZIP	
μPD424170V-80	80 ns		

QUALITY GRADE

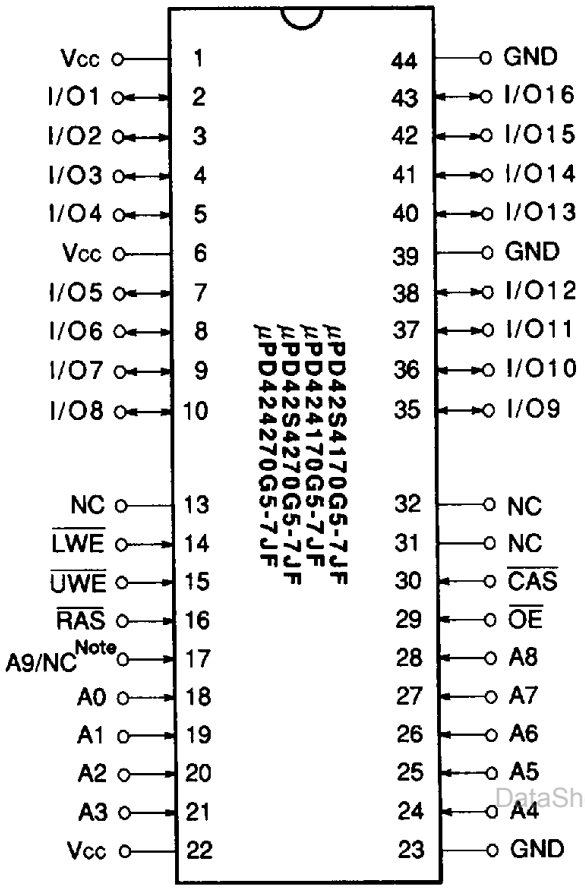
STANDARD

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

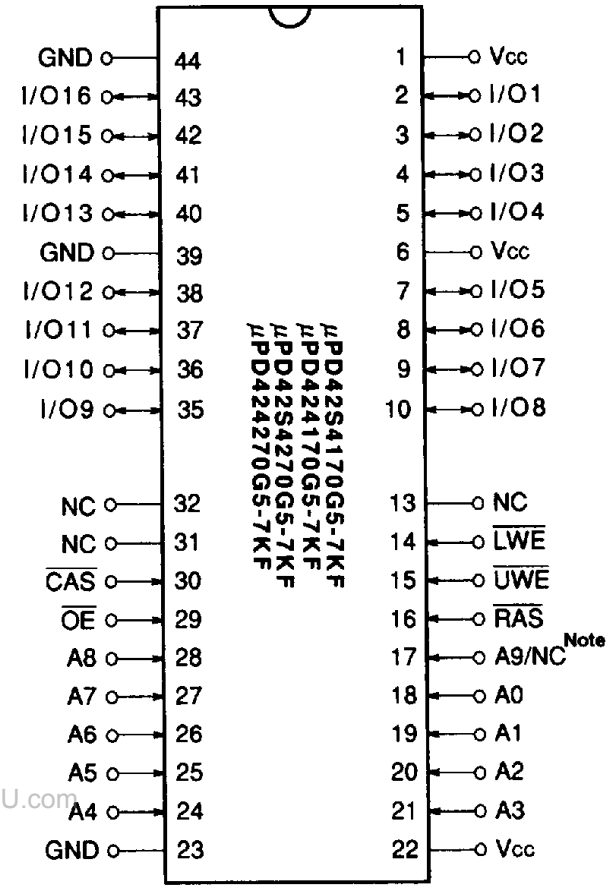
PIN CONFIGURATIONS

★

44-pin Plastic TSOP
(Marking Side)



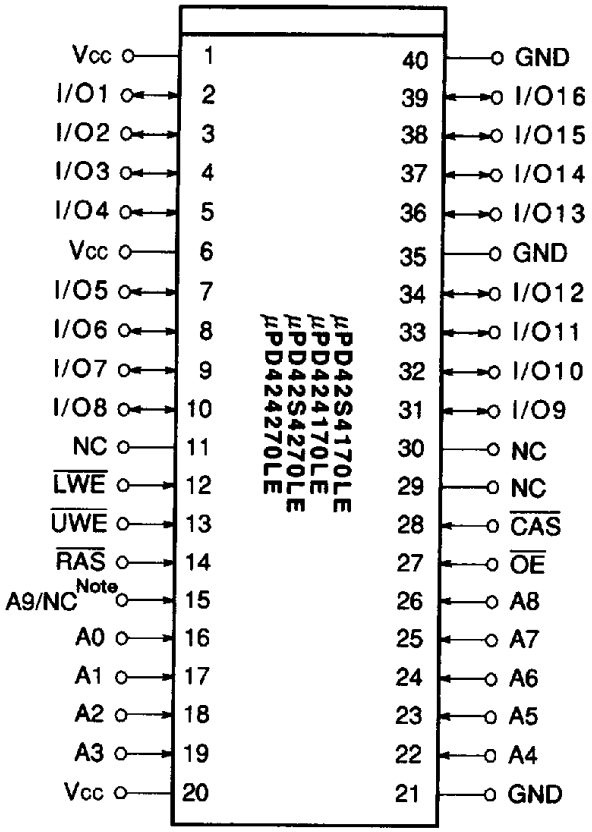
44-pin Plastic TSOP (Reverse bent)
(Marking Side)



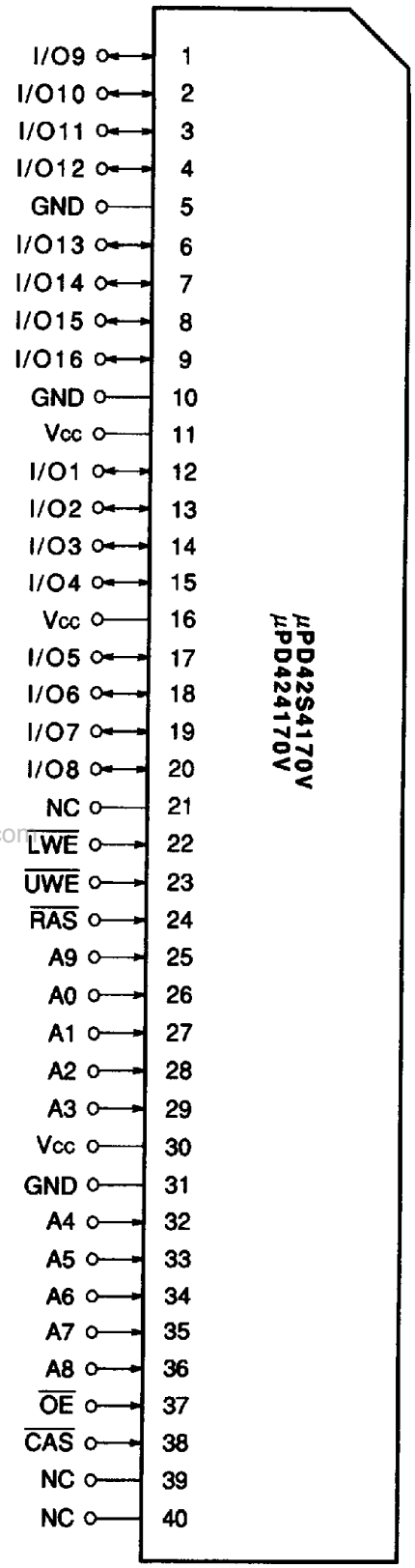
Note A9 ··· μPD42S4170, 424170
NC ··· μPD42S4270, 424270 (No connection)

A0 to A9	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{CAS}$	: Column Address Strobe
$\overline{UWE}$	: Upper Byte Write Enable
$\overline{LWE}$	: Lower Byte Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply (+5.0 V ± 10 %)
GND	: Ground
NC	: No Connection

40-pin Plastic SOJ
(Top View)



40-pin Plastic ZIP (Only for μPD42S4170, 424170)
(Front View)



Note A9 ··· μPD42S4170, 424170
NC ··· μPD42S4270, 424270 (No connection)

A0 to A9	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{CAS}$	: Column Address Strobe
$\overline{UWE}$	: Upper Byte Write Enable
$\overline{LWE}$	: Lower Byte Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply (+5.0 V ± 10 %)
GND	: Ground
NC	: No Connection

ELECTRICAL SPECIFICATIONS NOTE 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTE 2, 3

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O16			7	pF

★ DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

[μPD42S4170, 424170]

PARAMETER		SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTE
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		120	mA	4, 5
				t_{RAC} = 80 ns		105		
Standby current	μPD42S4170	I_{CC2}	$V_{IH(MIN)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2	mA	
			V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.2		
	μPD424170		$V_{IH(MIN)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2		
			V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		1		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $V_{IH(MIN)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		120	mA	4, 5
				t_{RAC} = 80 ns		105		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		100	mA	4, 5
				t_{RAC} = 80 ns		90		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		120	mA	4, 5
				t_{RAC} = 80 ns		105		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1 024 cycles/128 ms, only for μPD42S4170)		I_{CC6}	Standby : V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS} \leqq V_{IH(MAX.)}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 1 024 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ $\overline{WE}$, $\overline{OE}$: V_{IH} Address input : V_{IH} or V_{IL} Output : Hi-Z	$t_{RAS} \leqq$ 200 ns		200	μA	4, 5
				$t_{RAS} \leqq$ 1 μs		300		
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S4170)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$			150	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 5.5 V all other pins except for testing pin = 0 V		–10	+10	μA	
Output leakage current		$I_{O(L)}$	Output is disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.1 mA			0.4	V	

[μPD42S4270, 424270]

PARAMETER		SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTE
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		160	mA	4, 5
				t_{RAC} = 80 ns		145		
				t_{RAC} = 100 ns		120		
Standby current	μPD42S4270	I_{CC2}	$V_{IH(MIN)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2	mA	
			V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.2		
	μPD424270		$V_{IH(MIN)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2		
			V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		1		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $V_{IH(MIN)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		160	mA	4, 5
				t_{RAC} = 80 ns		145		
				t_{RAC} = 100 ns		120		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX)}$ $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		140	mA	4, 5
				t_{RAC} = 80 ns		130		
				t_{RAC} = 100 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		160	mA	4, 5
				t_{RAC} = 80 ns		145		
				t_{RAC} = 100 ns		120		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (512 cycles/128 ms, only for μPD42S4270)		I_{CC6}	Standby : V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS} \leqq V_{IH(MAX)}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 512 cycles/128 ms $\overline{RAS}, \overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$ $\overline{WE}, \overline{OE}$: V_{IH} Address input : V_{IH} or V_{IL} Output : Hi-Z	$t_{RAS} \leqq$ 200 ns		200	μA	4, 5
				$t_{RAS} \leqq$ 1 μs		300		
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S4270)		I_{CC7}	I_O = 0 mA $\overline{RAS}, \overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$			150	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 5.5 V all other pins except for testing pin = 0 V		–10	+10	μA	
Output leakage current		$I_{O(L)}$	Output is disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.1 mA			0.4	V	

★ AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) NOTE 6, 7

[μPD42S4170, 424170] (1/2)

PARAMETER	SYMBOL	tRAC = 70 ns		tRAC = 80 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	130		150		ns	8
Read Modify Write Cycle Time	tRWC	175		200		ns	8
Fast Page Mode Cycle Time	tPC	45		50		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	90		105		ns	8
Access Time from $\overline{RAS}$	tRAC		70		80	ns	9, 10
Access Time from $\overline{CAS}$	tCAC		20		20	ns	9, 10
Access Time from Column Address	tAA		35		40	ns	9, 10
Access Time from $\overline{CAS}$ Precharge	tACP		40		45	ns	10
$\overline{CAS}$ to Output Data Setup Time	tCLZ	0		0		ns	10
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	tOFF	0	15	0	20	ns	11
Transition Time (rise and fall)	tT	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	50		60		ns	
$\overline{RAS}$ Pulse Width	tRAS	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	tRASP	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	tRSH	20		20		ns	
$\overline{CAS}$ Hold Time	tCSH	70		80		ns	
$\overline{CAS}$ Pulse Width	tCAS	20	10 000	20	10 000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	50	20	60	ns	9
$\overline{RAS}$ to Column Address Delay Time	tRAD	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	10		10		ns	12
$\overline{CAS}$ Precharge Time (Fast Page Mode)	tCP	10		10		ns	
Row Address Setup Time	tASR	0		0		ns	
Row Address Hold Time	tRAH	10		10		ns	
Column Address Setup Time	tASC	0		0		ns	
Column Address Hold Time	tCAH	15		15		ns	
$\overline{CAS}$ Precharge Time	tCPN	10		10		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	35		40		ns	
Read Command Setup Time	tRCS	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0		0		ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0		0		ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	tWCH	15		15		ns	14
Write Command Pulse Width	tWP	15		15		ns	14
Write Command Lead Time Referenced to $\overline{RAS}$	tRWL	20		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$	tCWL	15		20		ns	
Data-in Setup Time	tDS	0		0		ns	15
Data-in Hold Time	tDH	15		20		ns	15

(2/2)

PARAMETER		SYMBOL	tRAC = 70 ns		tRAC = 80 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Refresh Time	μPD42S4170	tREF		128		128	ms	17
	μPD424170			16		16	ms	
Write Command Setup Time		tWCS	0		0		ns	16
$\overline{CAS}$ to $\overline{WE}$ Delay Time		tCWD	40		45		ns	16
$\overline{RAS}$ to $\overline{WE}$ Delay Time		tRWD	90		105		ns	16
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		tCPWD	60		70		ns	16
Column Address Delay Time Referenced to $\overline{WE}$		tAWD	55		65		ns	16
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCSR	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCHR	15		15		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		tRPC	10		10		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time		tOES	0		0		ns	
Access Time from $\overline{OE}$		tOEA		20		20	ns	
$\overline{OE}$ Data Delay Time		tOED	15		20		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)		tOEZ	0	15	0	20	ns	11
$\overline{OE}$ Output Data Setup Time		tOLZ	0		0		ns	
$\overline{OE}$ Hold Time		tOEH	0		0		ns	
Masked Byte Write Setup Time		tMCS	0		0		ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$		tMRH	0		0		ns	
Masked Byte Write Hold Time Referenced to $\overline{CAS}$		tMCH	0		0		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$ Precharge		tRHCP	40		45		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRASS	100		100		μs	17
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRPS	130		150		ns	17
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tCHS	−50		−50		ns	17

[μPD42S4270, 424270] (1/2)

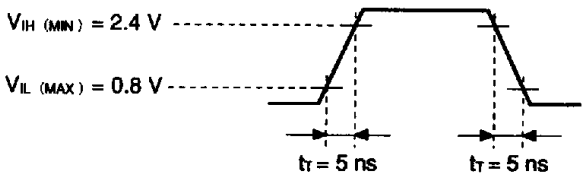
PARAMETER	SYMBOL	tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	130		150		190		ns	8
Read Modify Write Cycle Time	tRWC	175		200		255		ns	8
Fast Page Mode Cycle Time	tPC	45		50		65		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	90		105		125		ns	8
Access Time from $\overline{RAS}$	tRAC		70		80		100	ns	9, 10
Access Time from $\overline{CAS}$	tCAC		20		20		25	ns	9, 10
Access Time from Column Address	tAA		35		40		50	ns	9, 10
Access Time from $\overline{CAS}$ Precharge	tACP		40		45		55	ns	10
$\overline{CAS}$ to Output Data Setup Time	tCLZ	0		0		0		ns	10
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	tOFF	0	15	0	20	0	20	ns	11
Transition Time (rise and fall)	tT	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	50		60		80		ns	
$\overline{RAS}$ Pulse Width	tRAS	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	tRASP	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time	tRSH	20		20		30		ns	
$\overline{CAS}$ Hold Time	tCSH	70		80		100		ns	
$\overline{CAS}$ Pulse Width	tCAS	20	10 000	20	10 000	30	10 000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	50	20	60	25	75	ns	9
$\overline{RAS}$ to Column Address Delay Time	tRAD	15	35	15	40	20	50	ns	9
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	10		10		10		ns	12
$\overline{CAS}$ Precharge Time (Fast Page Mode)	tCP	10		10		10		ns	
Row Address Setup Time	tASR	0		0		0		ns	
Row Address Hold Time	tRAH	10		10		15		ns	
Column Address Setup Time	tASC	0		0		0		ns	
Column Address Hold Time	tCAH	15		15		20		ns	
$\overline{CAS}$ Precharge Time	tCPN	10		10		10		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	35		40		50		ns	
Read Command Setup Time	tRCS	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0		0		0		ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0		0		0		ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	tWCH	15		15		20		ns	14
Write Command Pulse Width	tWP	15		15		20		ns	14
Write Command Lead Time Referenced to $\overline{RAS}$	tRWL	20		25		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$	tCWL	15		20		25		ns	
Data-in Setup Time	tDS	0		0		0		ns	15
Data-in Hold Time	tDH	15		20		20		ns	15

(2/2)

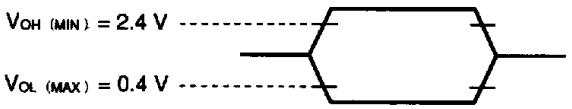
PARAMETER		SYMBOL	tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Refresh Time	μPD42S4270	tREF		128		128		128	ms	17
	μPD424270			8		8		8	ms	
Write Command Setup Time		tWCS	0		0		0		ns	16
$\overline{CAS}$ to $\overline{WE}$ Delay Time		tCWD	40		45		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ Delay Time		tRWD	90		105		135		ns	16
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		tCPWD	60		70		85		ns	16
Column Address Delay Time Referenced to $\overline{WE}$		tAWD	55		65		90		ns	16
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCSR	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCHR	15		15		20		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		tRPC	10		10		10		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time		tOES	0		0		0		ns	
Access Time from $\overline{OE}$		tOEA		20		25		25	ns	
$\overline{OE}$ Data Delay Time		tOED	15		20		25		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)		tOEZ	0	15	0	20	0	20	ns	11
$\overline{OE}$ Output Data Setup Time		tOLZ	0		0		0		ns	
$\overline{OE}$ Hold Time		tOEH	0		0		0		ns	
Masked Write Setup Time		tMCS	0		0		0		ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$		tMRH	0		0		0		ns	
Masked Byte Write Hold Time Referenced to $\overline{CAS}$		tMCH	0		0		0		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$ Precharge		tRHCP	40		45		55		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRASS	100		100		100		μs	17
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRPS	130		150		190		ns	17
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tCHS	−50		−50		−50		ns	17

★ **NOTE** 1. $\overline{WE}$ means $\overline{UWE}$ and $\overline{LWE}$.

2. All voltages are referenced to GND.
3. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
4. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on t_{RC} and t_{PC}. Specified values are obtained with outputs open.
5. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
6. AC measurements assume t_T = 5 ns.
7. AC Characteristics test condition
   (1) Input timing specification



   (2) Output timing specification



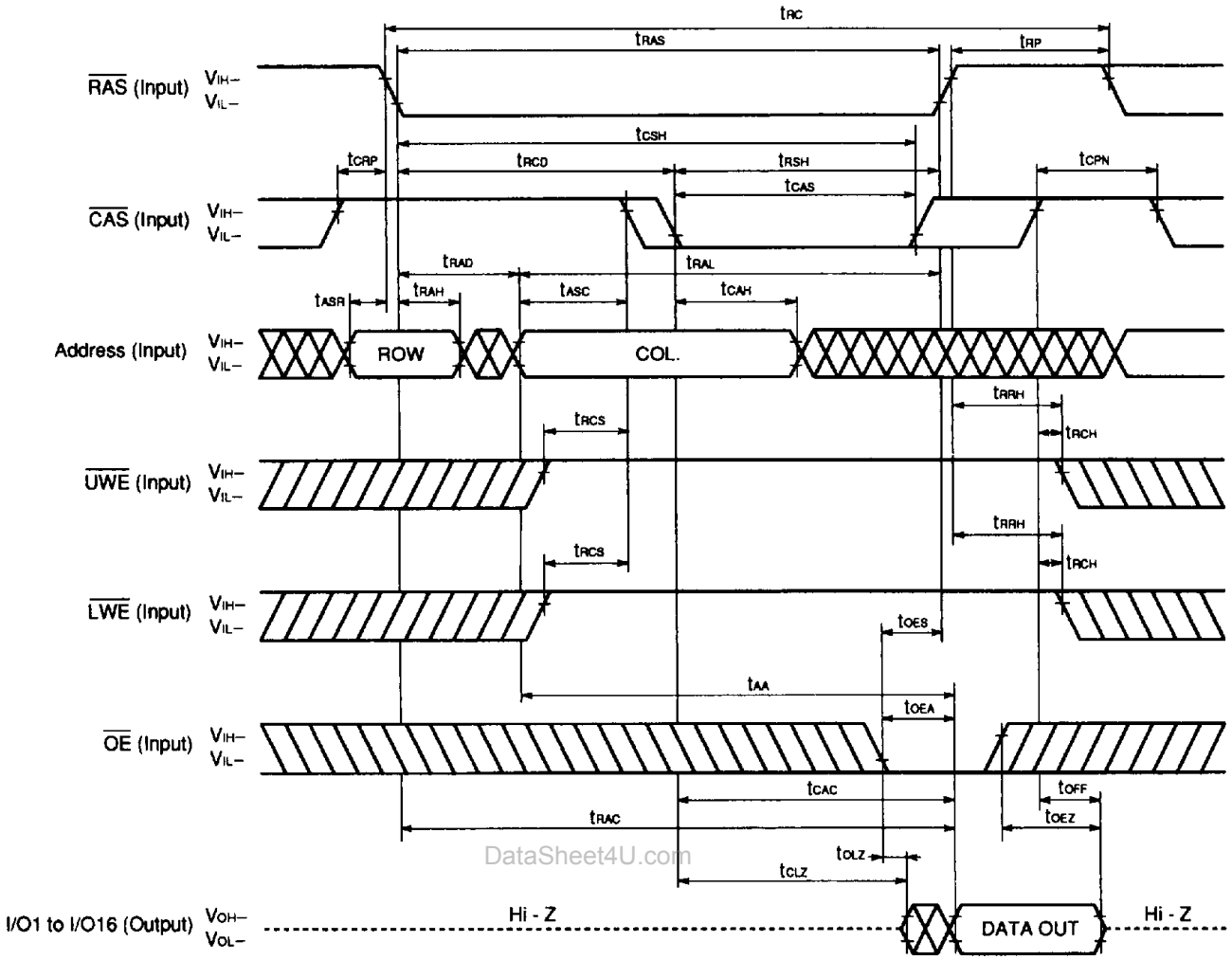
8. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
9. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD\ (MAX.)} \leqq t_{RAD}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$
$t_{RCD\ (MAX.)} \leqq t_{RCD}$	$t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ indicate the points which the access time changes and are not the limits of operation.

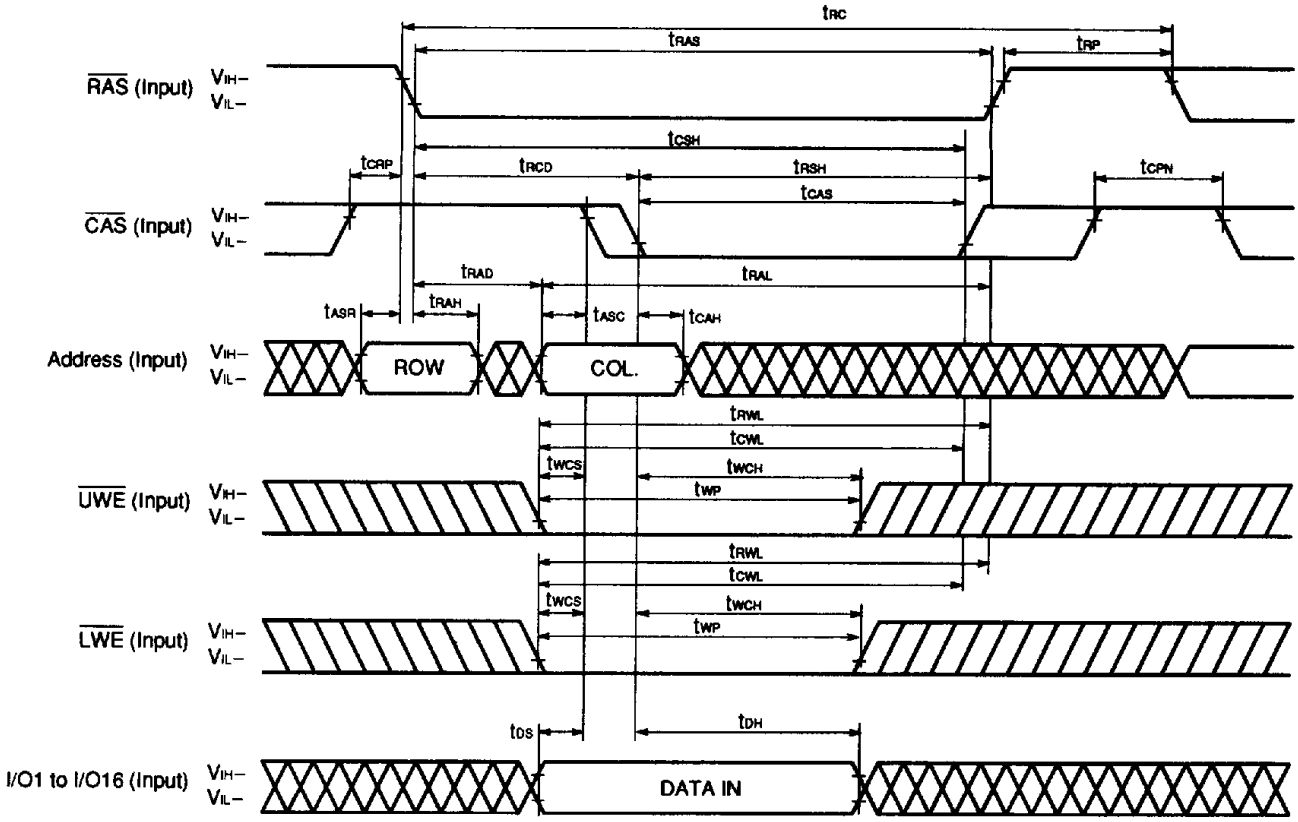
10. Loading conditions are 1TTL and 100 pF.
11. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
12. $t_{CRP(MIN.)}$ requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycles.
13. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ must be satisfied for a read cycle.
14. $t_{WP\ (MIN.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (MIN.)}$ should be satisfied.
15. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters.They are included in the data sheet as electrical characteristics only. If $t_{WCS\ (MIN.)} \leqq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD\ (MIN.)} \leqq t_{RWD}$, $t_{CWD\ (MIN.)} \leqq t_{CWD}$, $t_{AWD\ (MIN.)} \leqq t_{AWD}$, and $t_{CPWD\ (MIN.)} \leqq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.
17. This specification is applicable only for μPD42S4170, 42S4270.

READ CYCLE



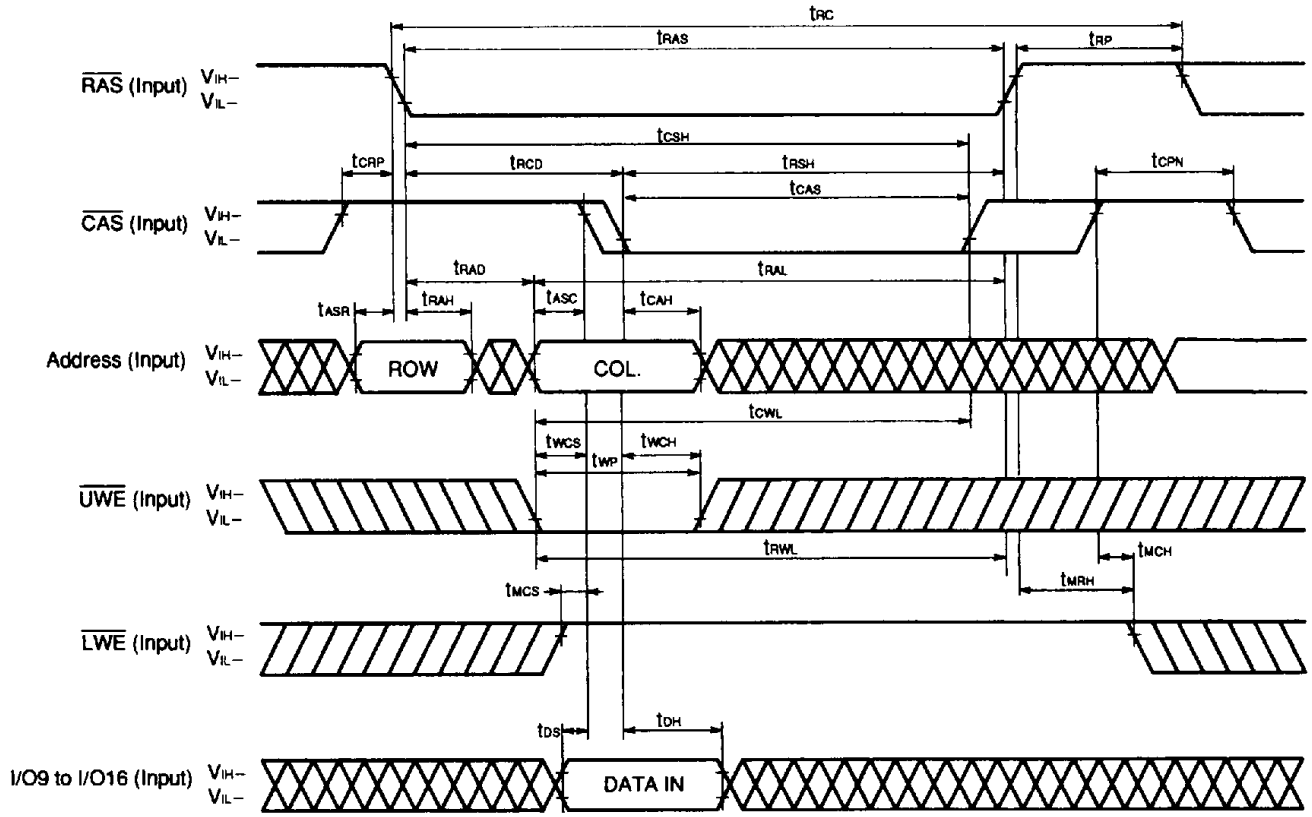
6427525 0041967 895 NECE

EARLY WRITE CYCLE



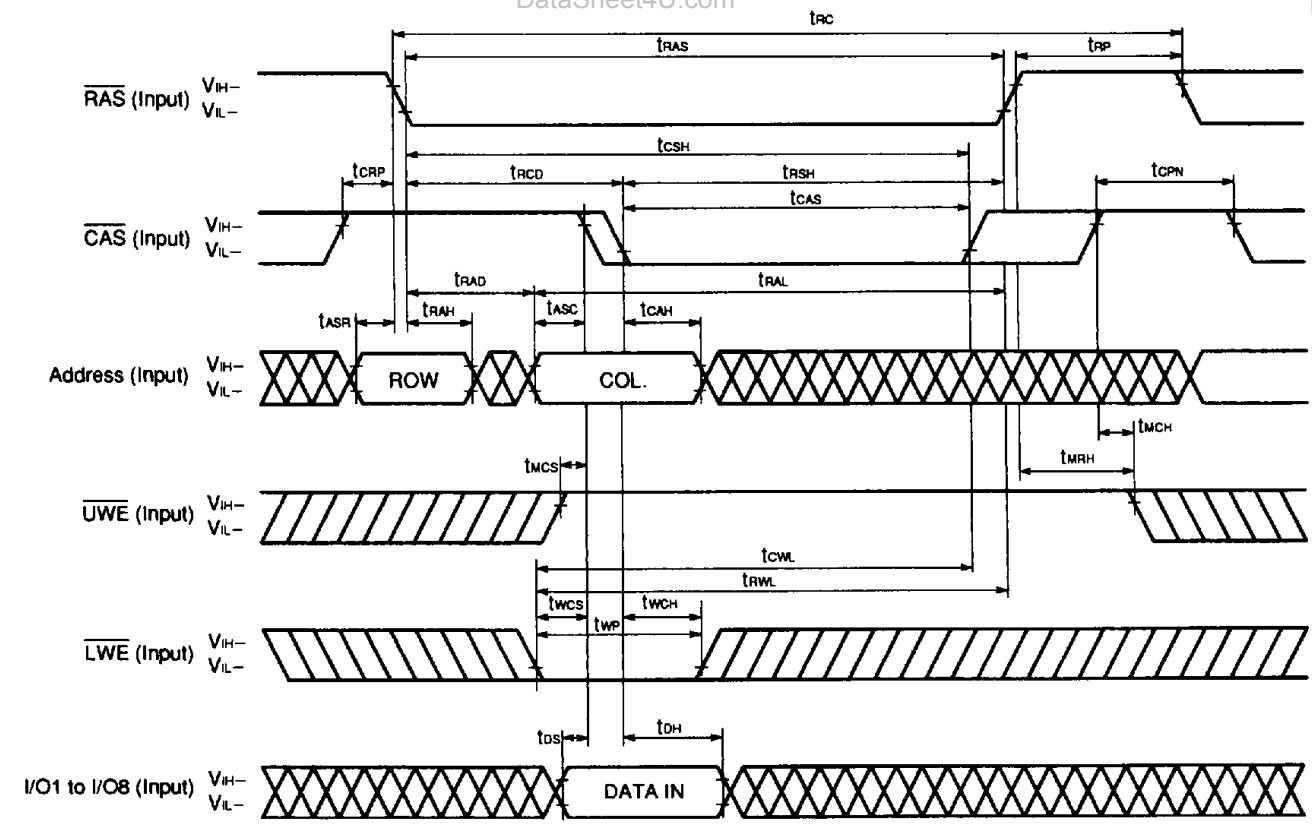
Remark $\overline{OE}$ = Don't care

UPPER BYTE EARLY WRITE CYCLE



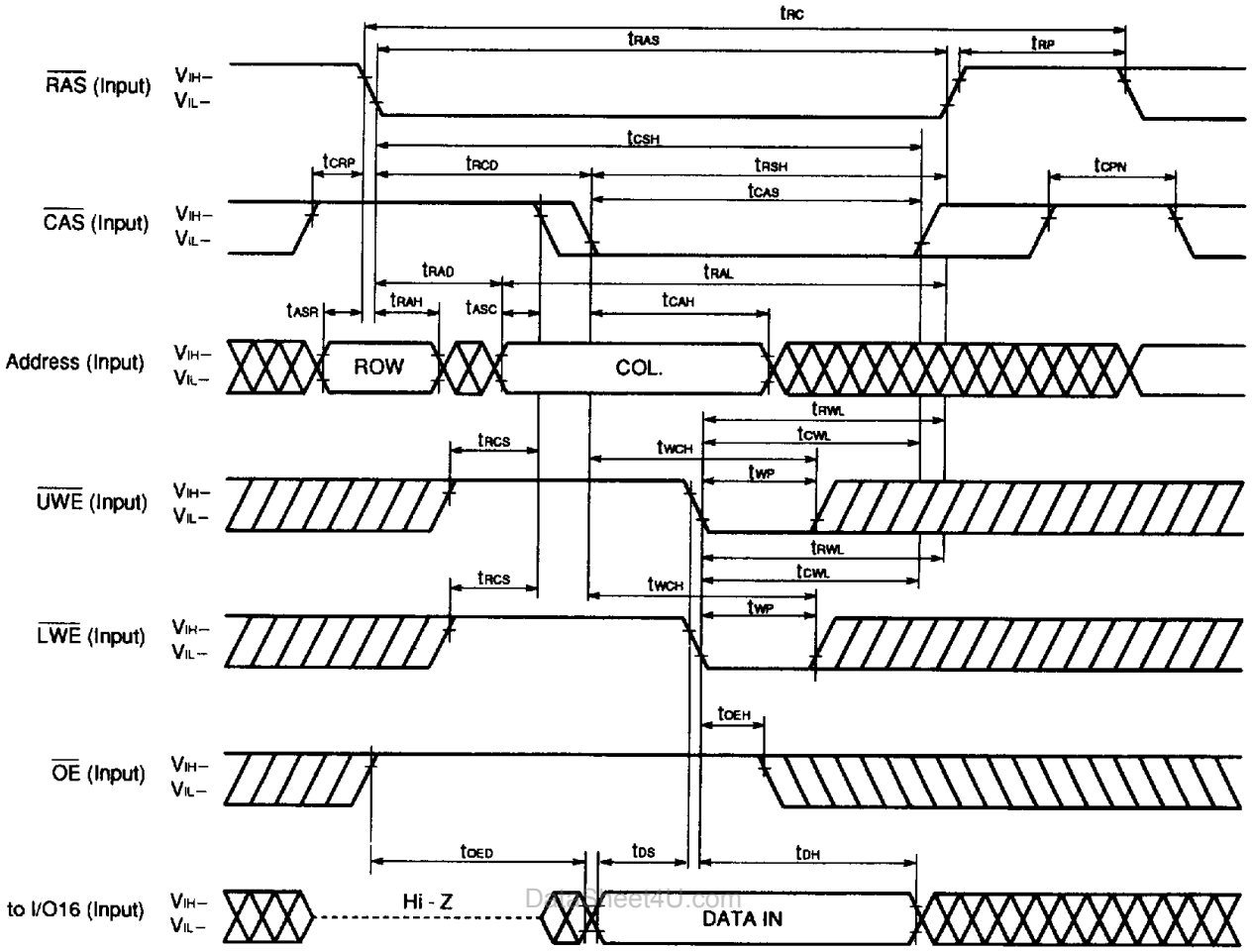
Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

LOWER BYTE EARLY WRITE CYCLE

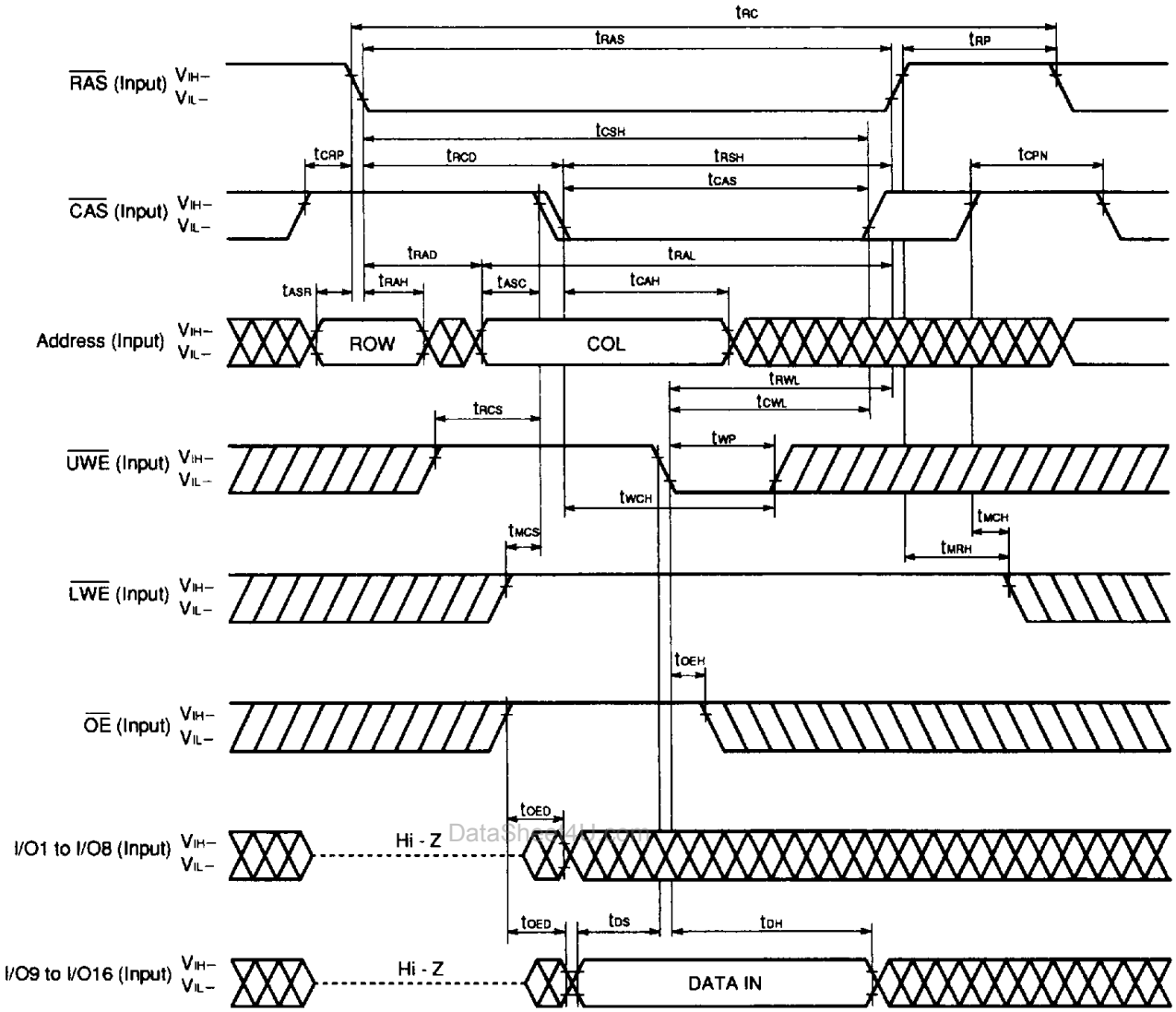


Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

LATE WRITE CYCLE

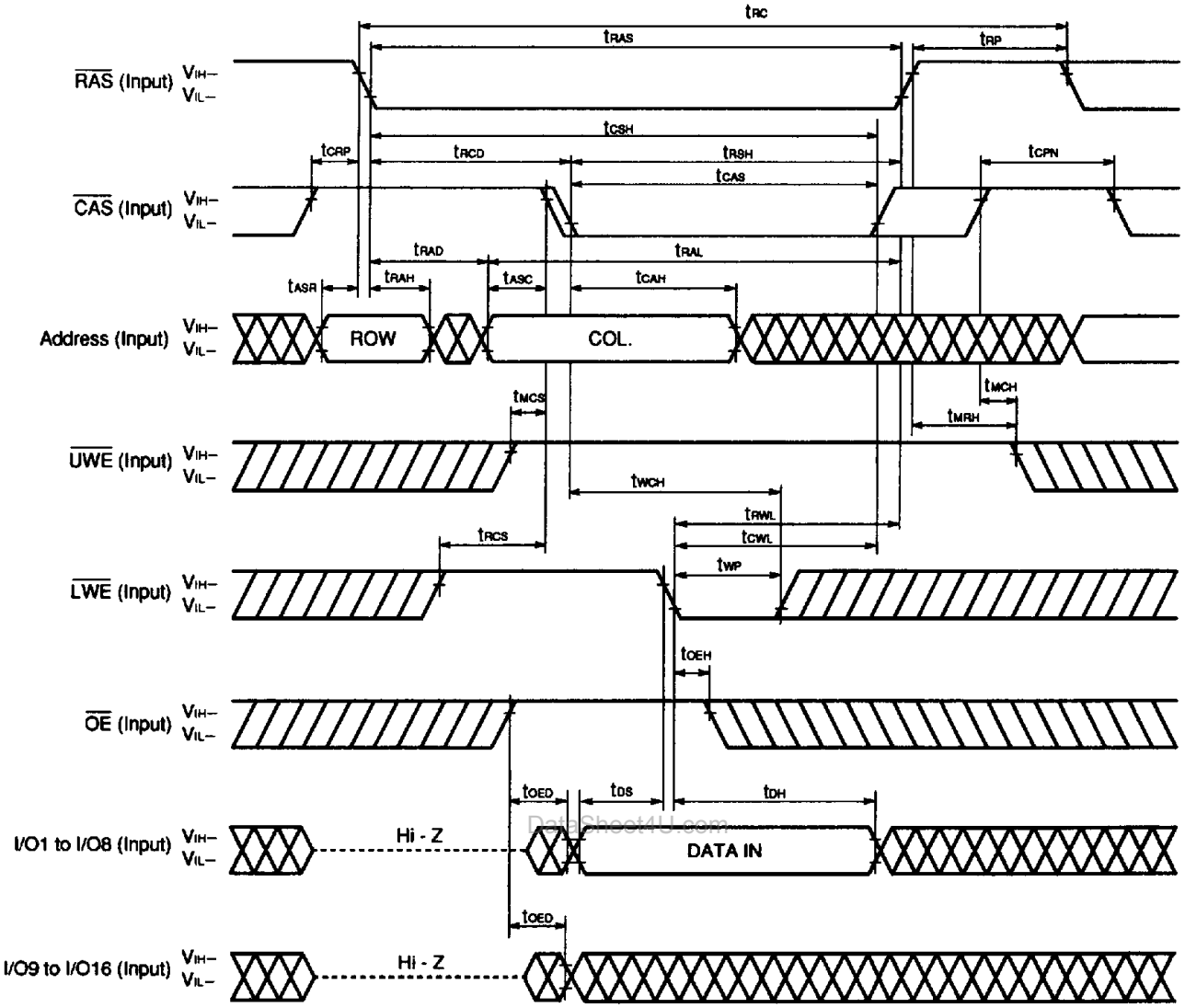


UPPER BYTE LATE WRITE CYCLE

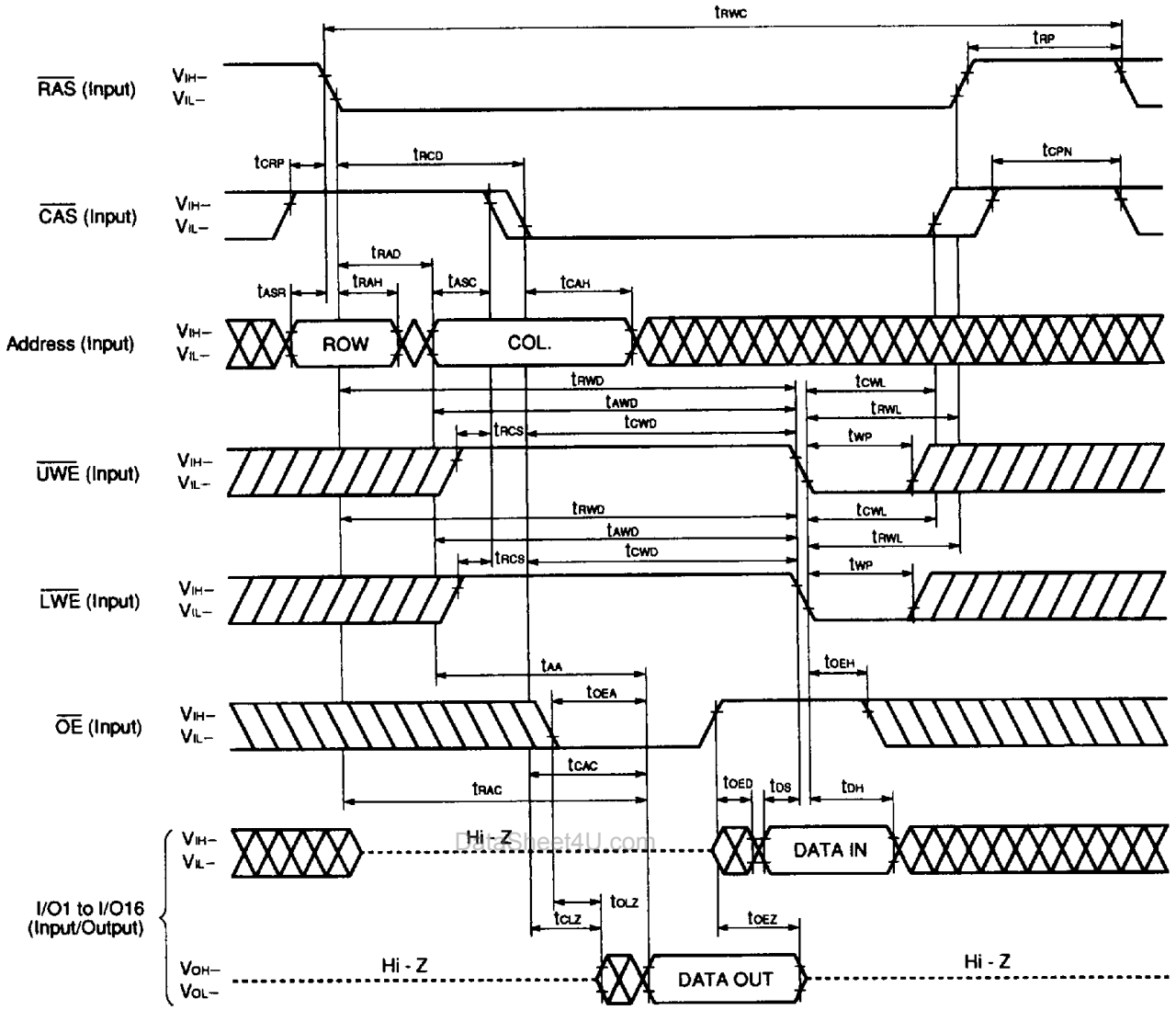


6427525 0041971 216 NECE

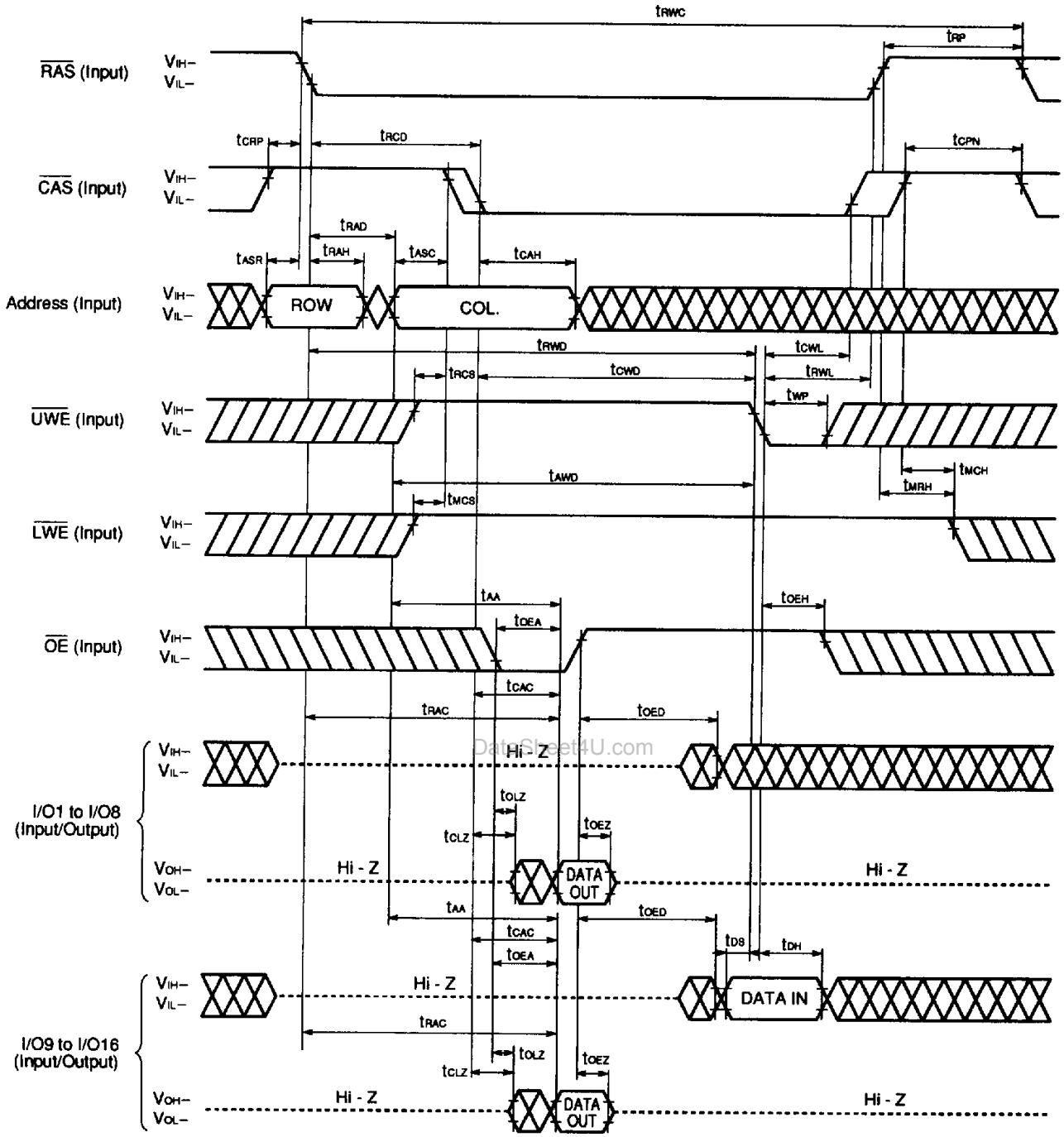
LOWER BYTE LATE WRITE CYCLE



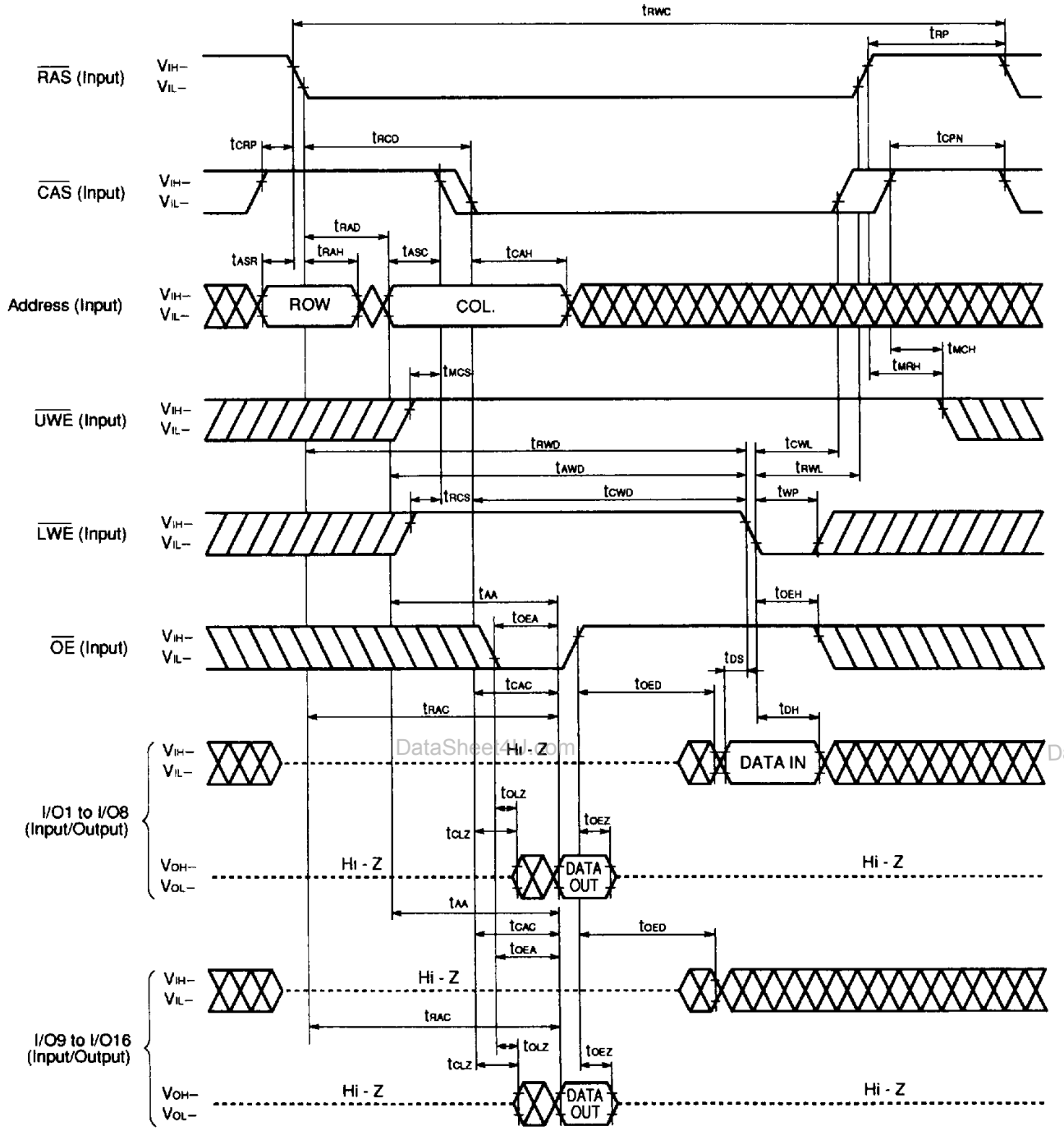
READ MODIFY WRITE CYCLE



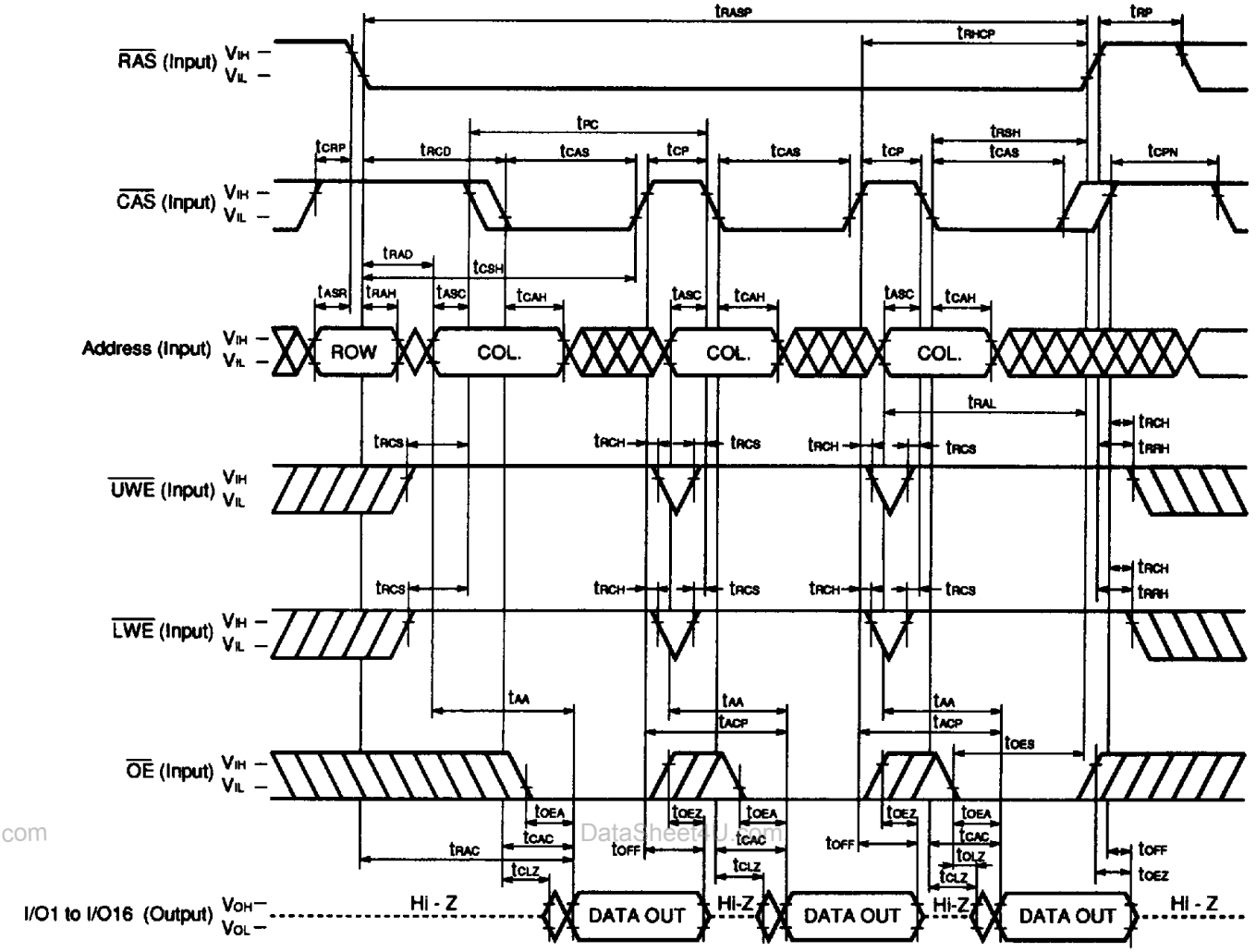
UPPER BYTE READ MODIFY WRITE CYCLE



LOWER BYTE READ MODIFY WRITE CYCLE

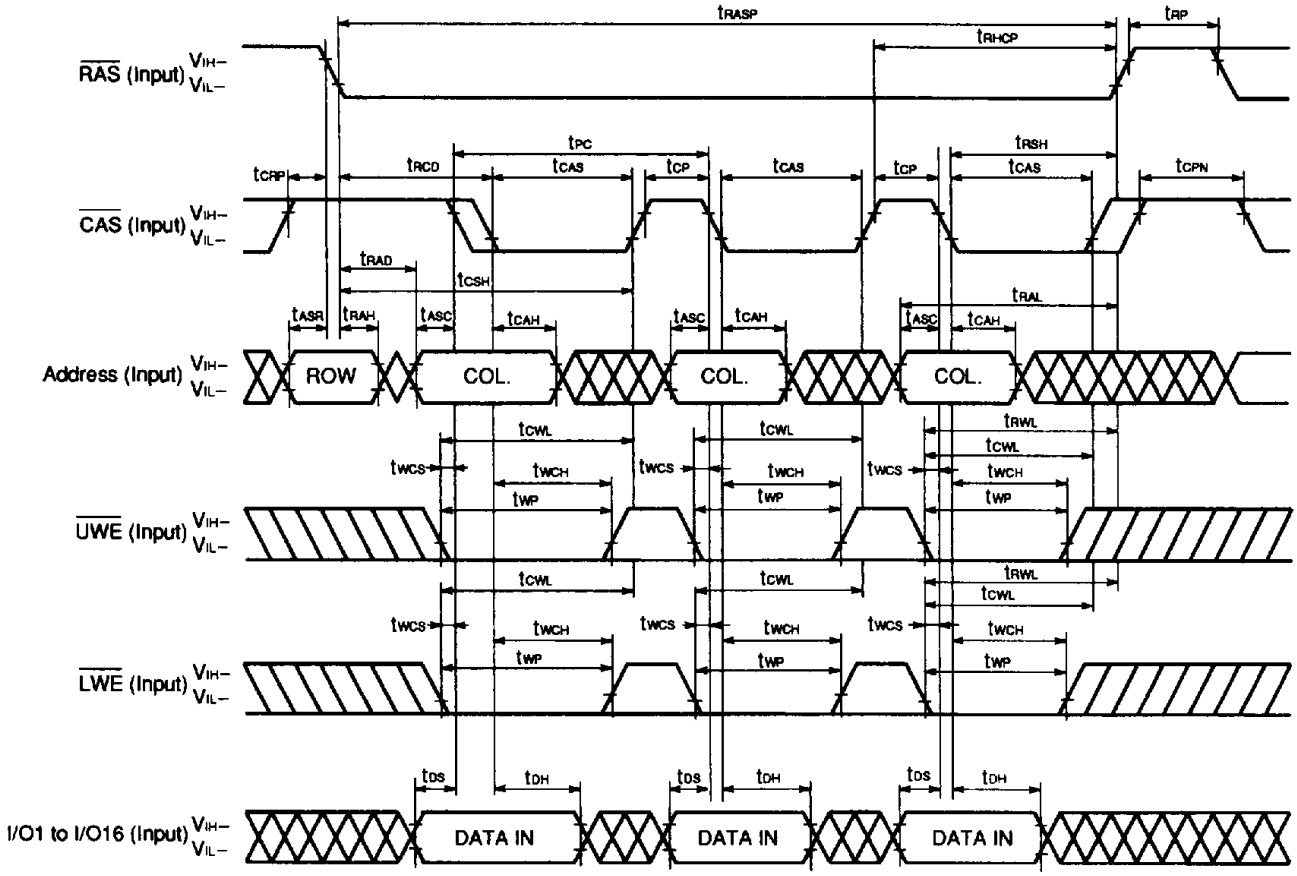


FAST PAGE MODE READ CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

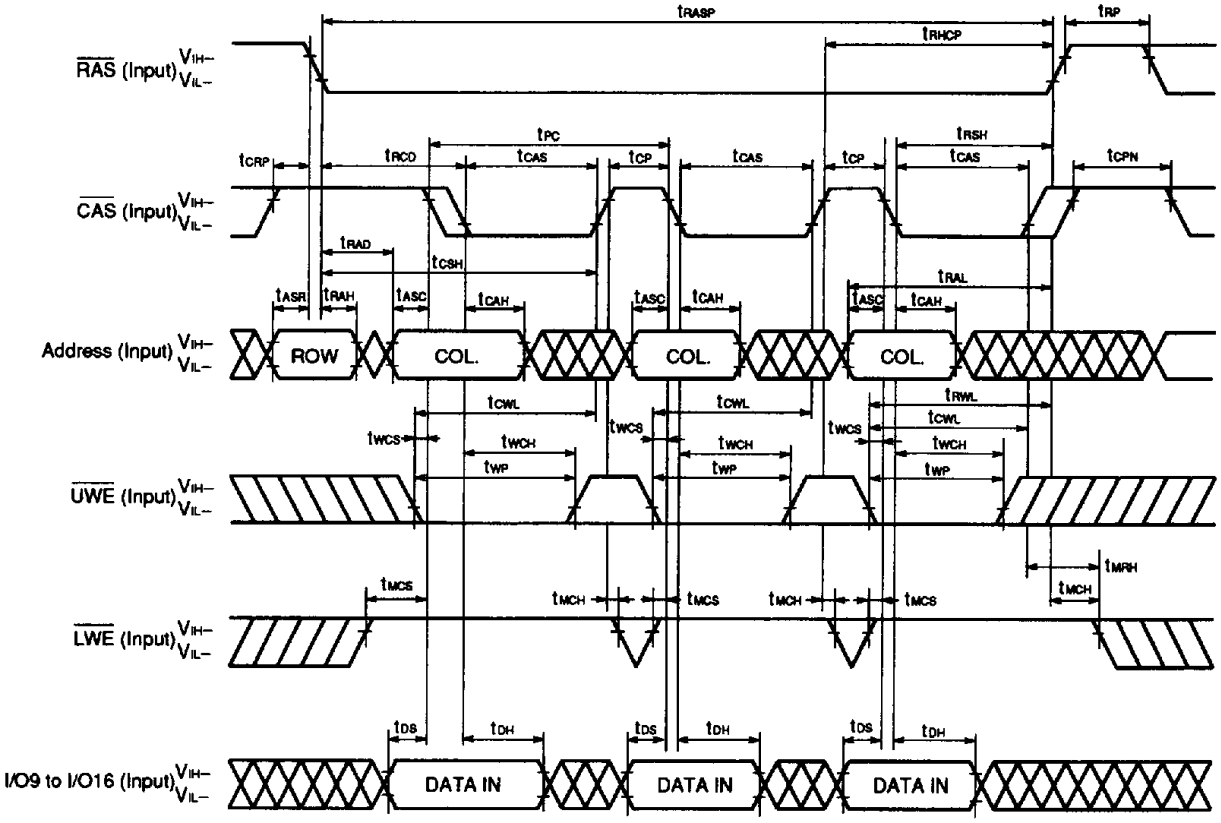
FAST PAGE MODE EARLY WRITE CYCLE



Remark $\overline{OE}$ = Don't care

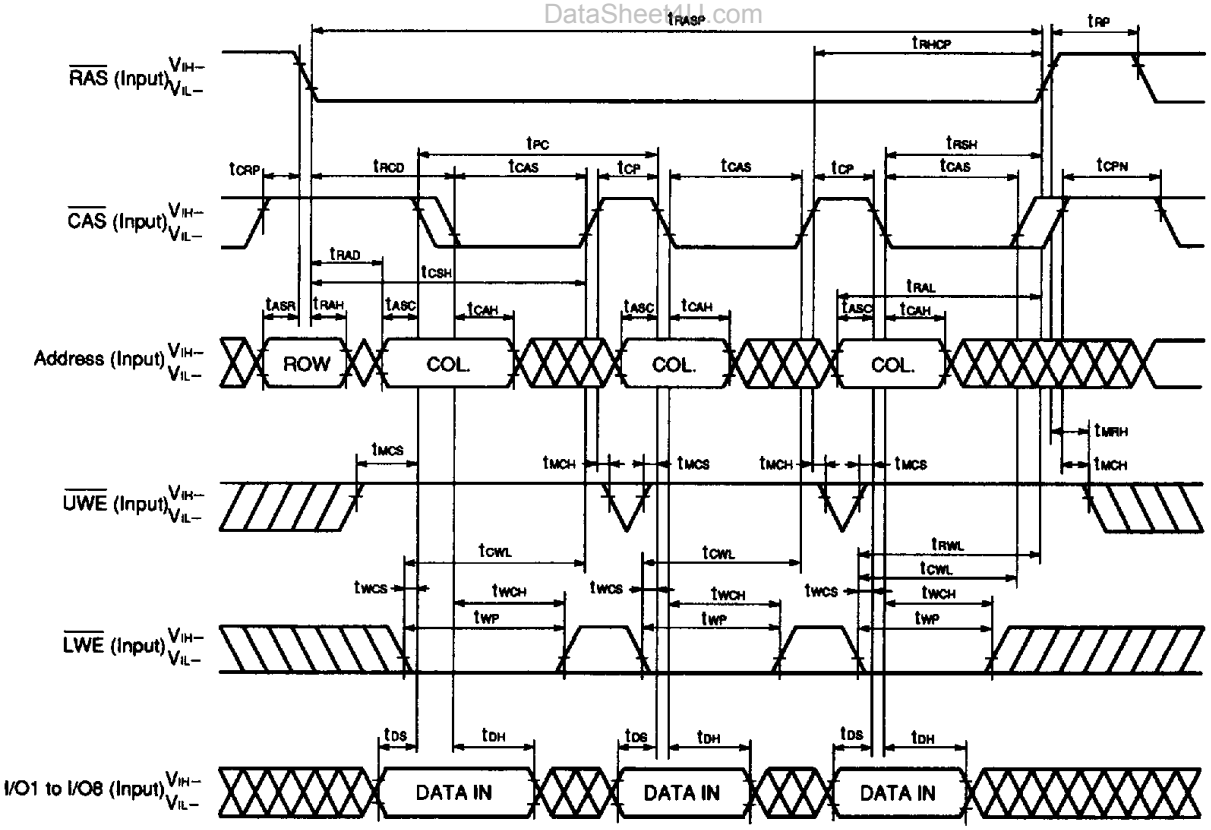
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE EARLY WRITE CYCLE



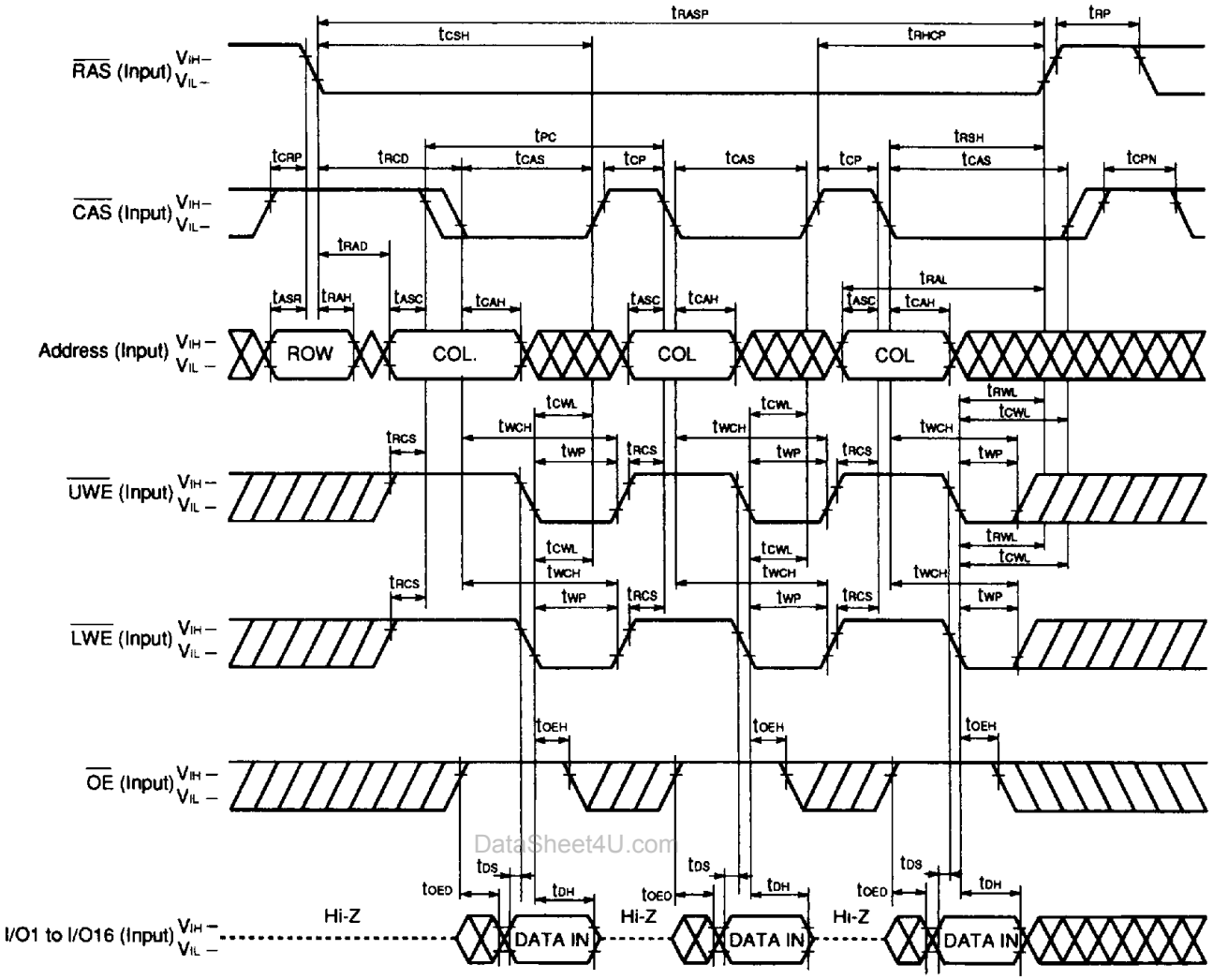
Remark $\overline{OE}$, I/O1 to I/O8 = Don't care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE EARLY WRITE CYCLE



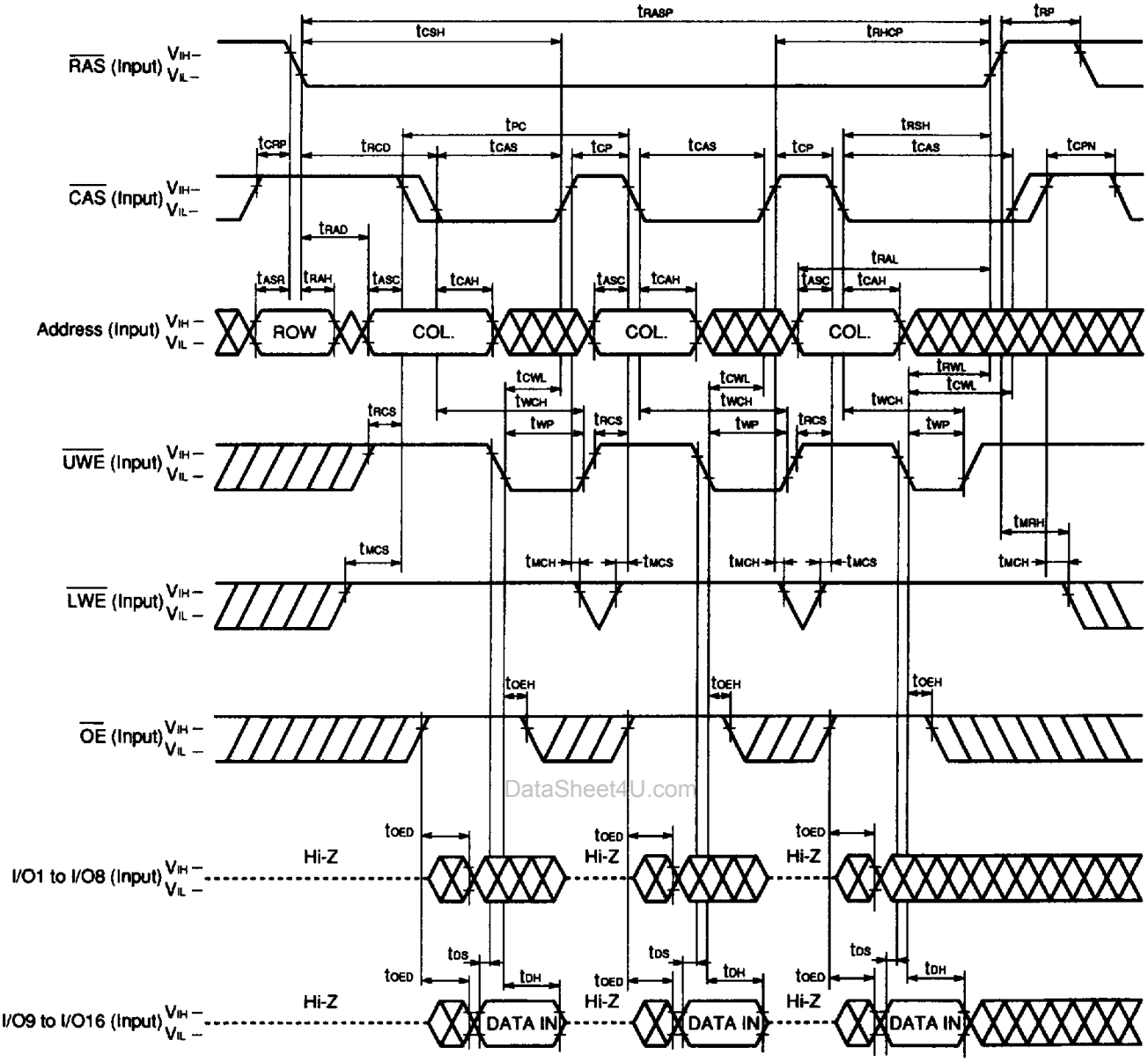
Remark $\overline{OE}$, I/O9 to I/O16 = Don't care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LATE WRITE CYCLE



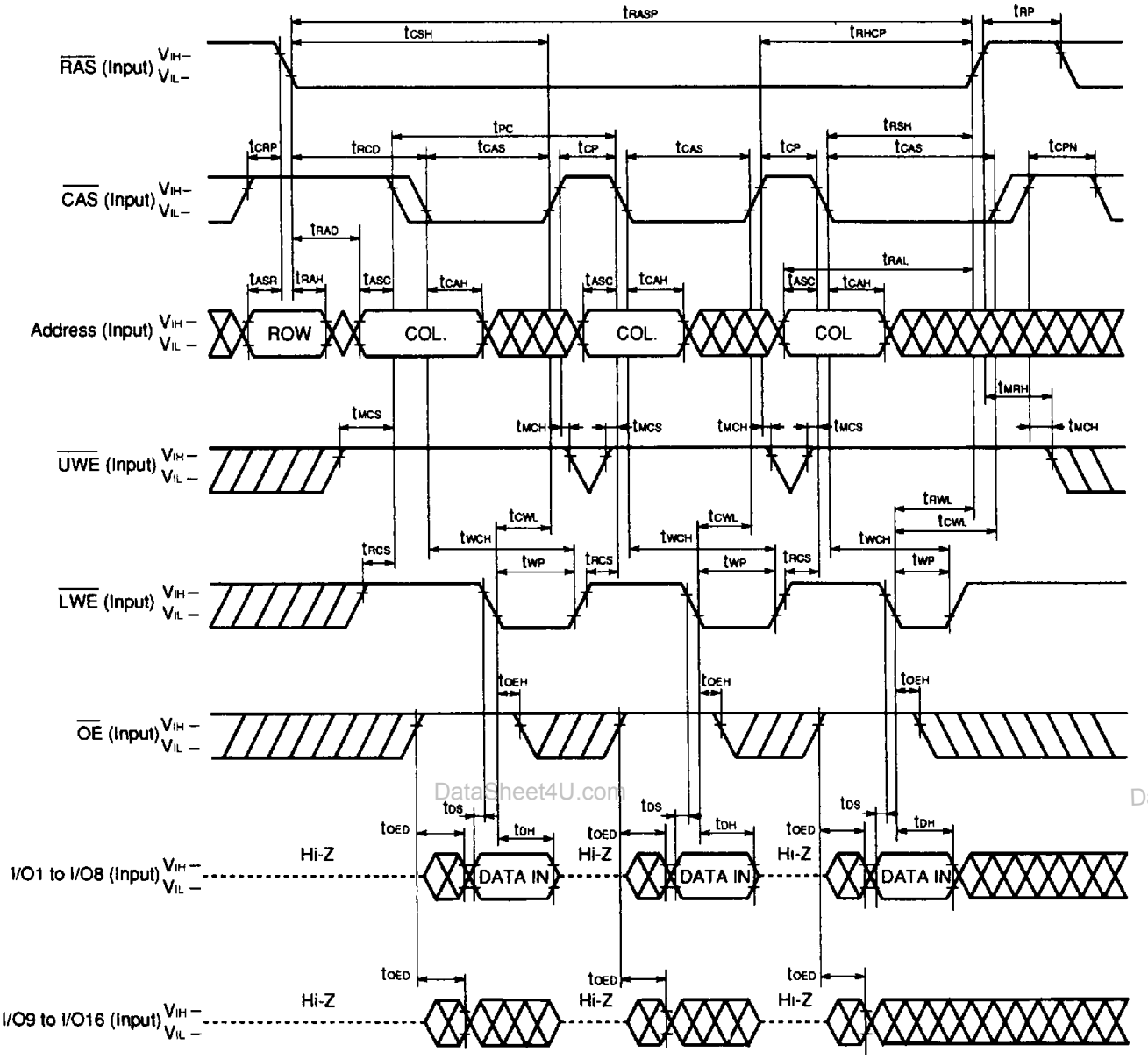
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE LATE WRITE CYCLE



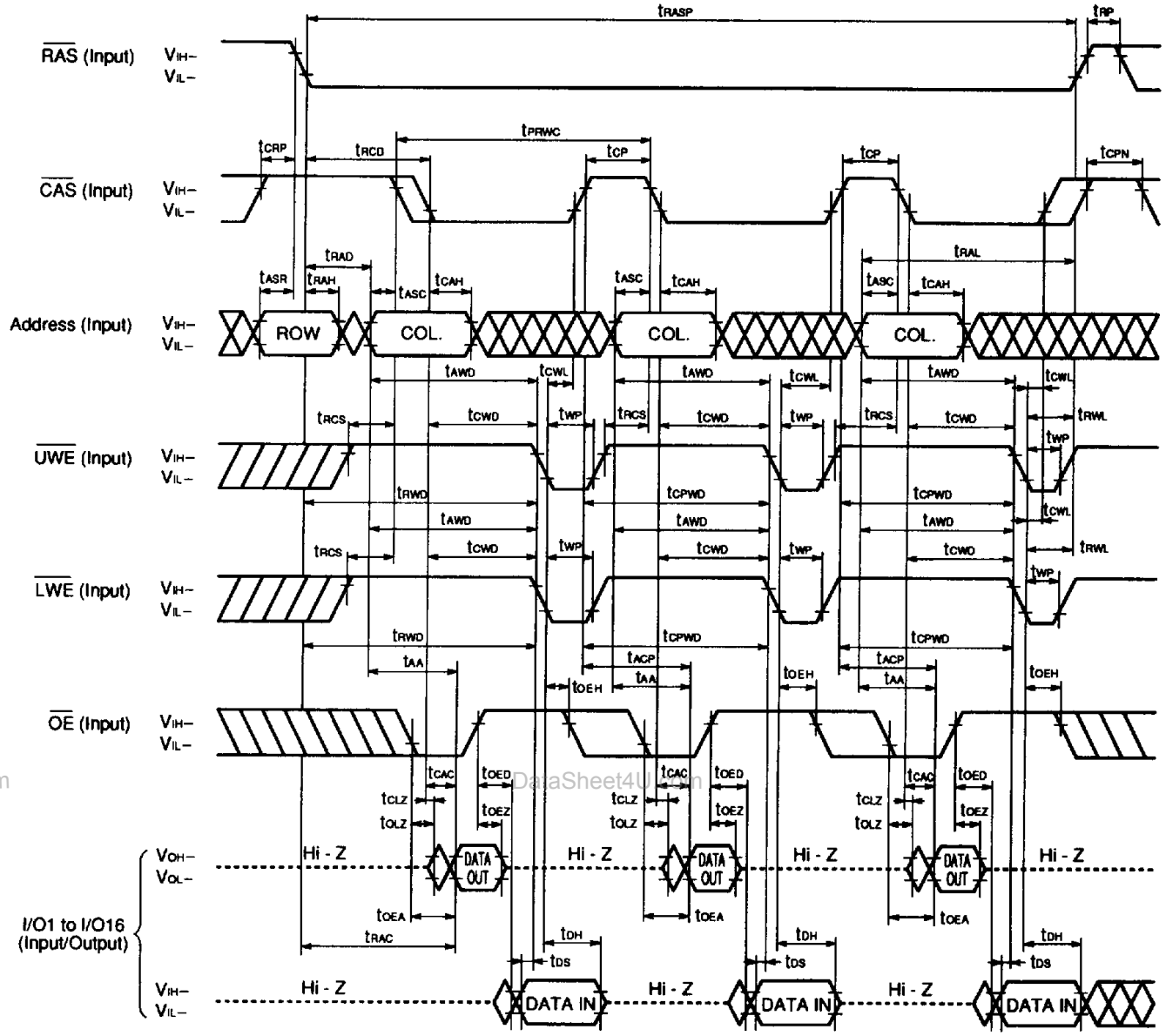
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE LATE WRITE CYCLE



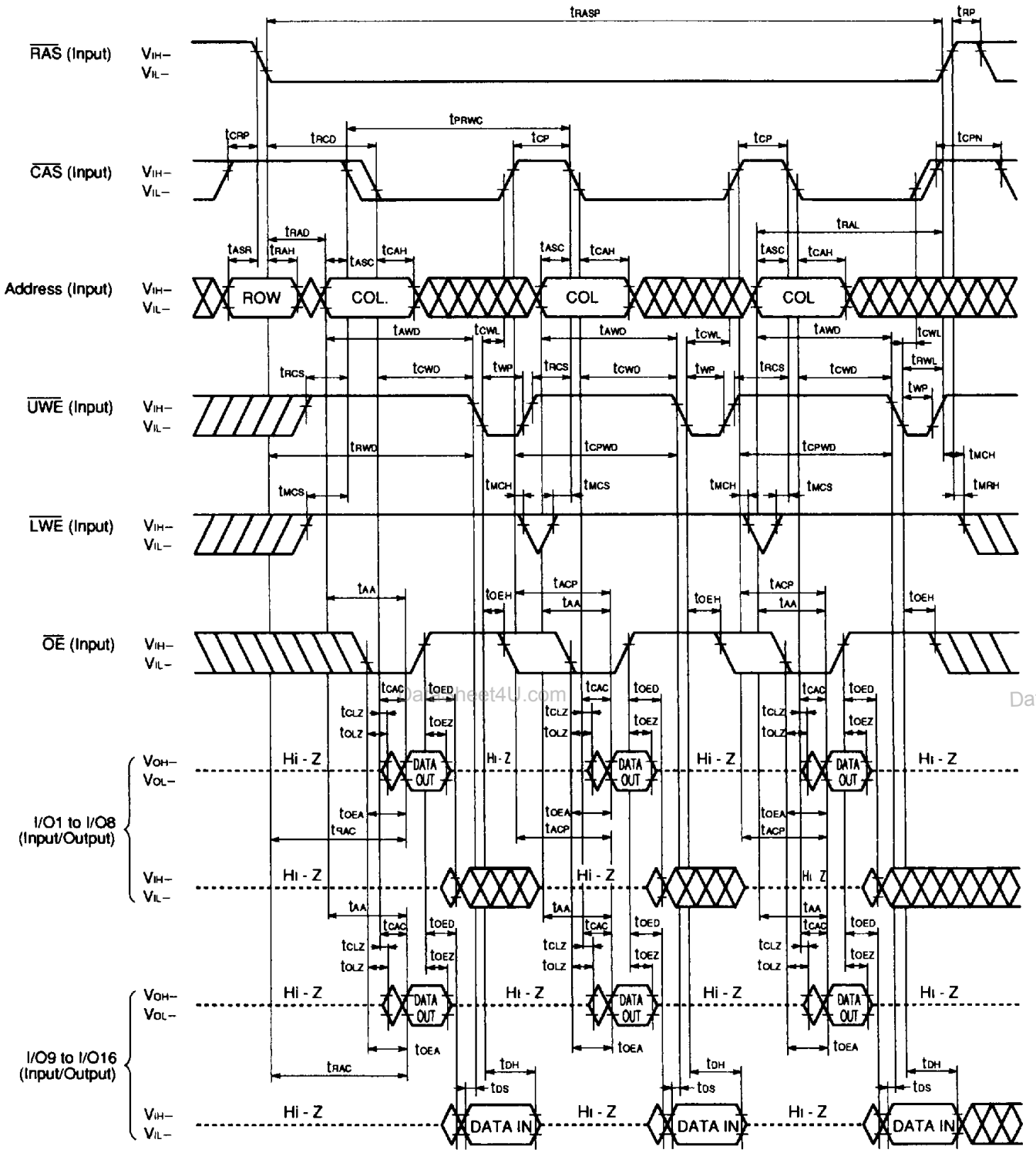
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE READ MODIFY WRITE CYCLE



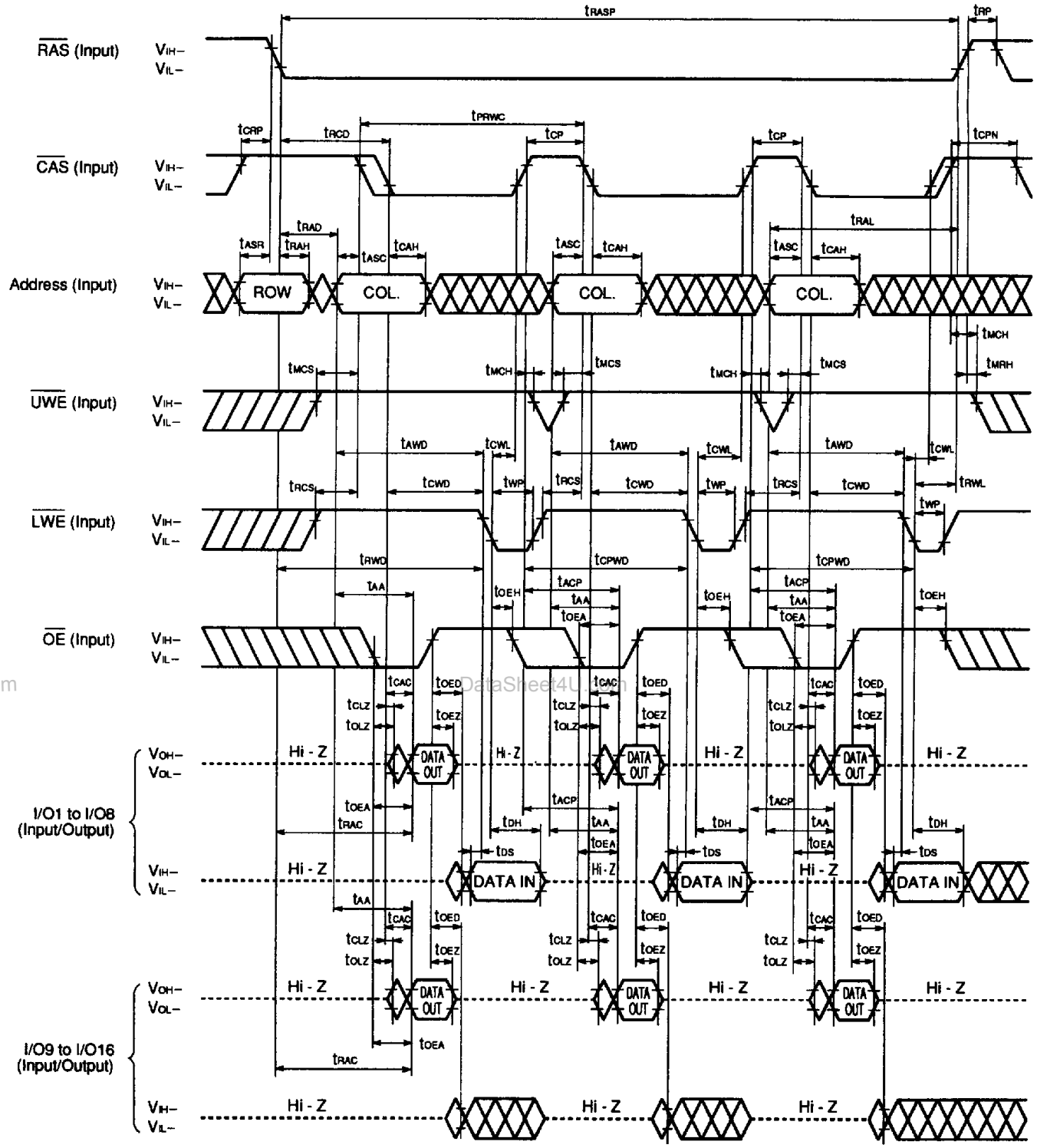
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

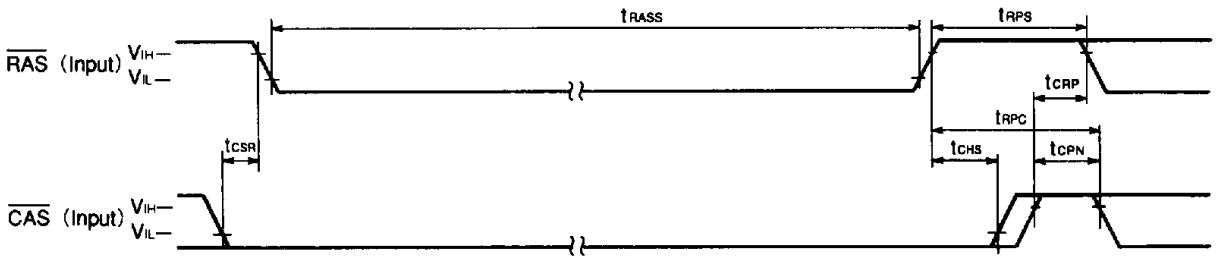
FAST PAGE MODE LOWER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

6427525 0041984 974 NECE

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE (Only for μPD42S4170, 42S4270) ★



Remark Address, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi-Z

How to use the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.

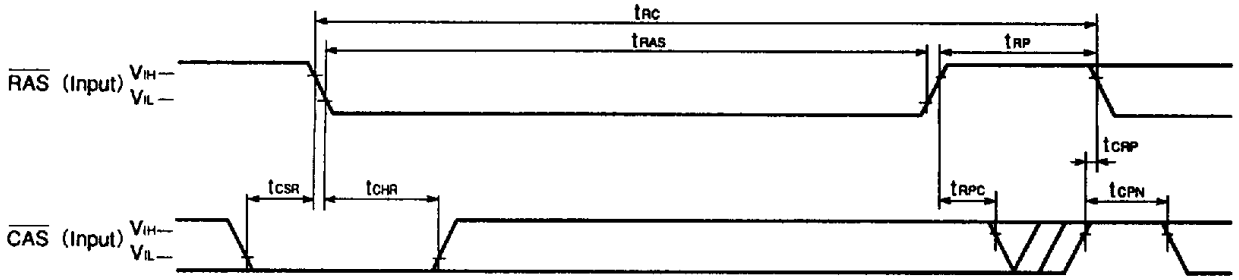
$\overline{CAS}$ before $\overline{RAS}$ self refresh mode can't be used by itself. It must be used with performing one of 3 refreshes below.

- **When using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 1 024 times (μPD42S4170) or 512 times (μPD42S4270) during 128 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

- **When using burst $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 1 024 times (μPD42S4170) during 16 ms or 512 times (μPD42S4270) during 8 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

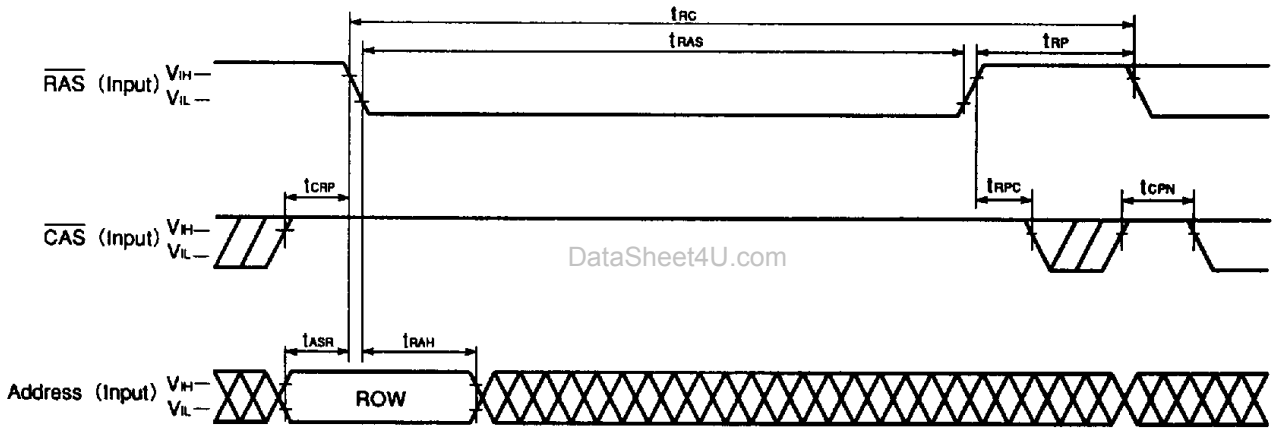
- **When using $\overline{RAS}$ only refresh**
  Refresh all refresh addresses during 16 ms (μPD42S4170) or 8 ms (μPD42S4270) before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



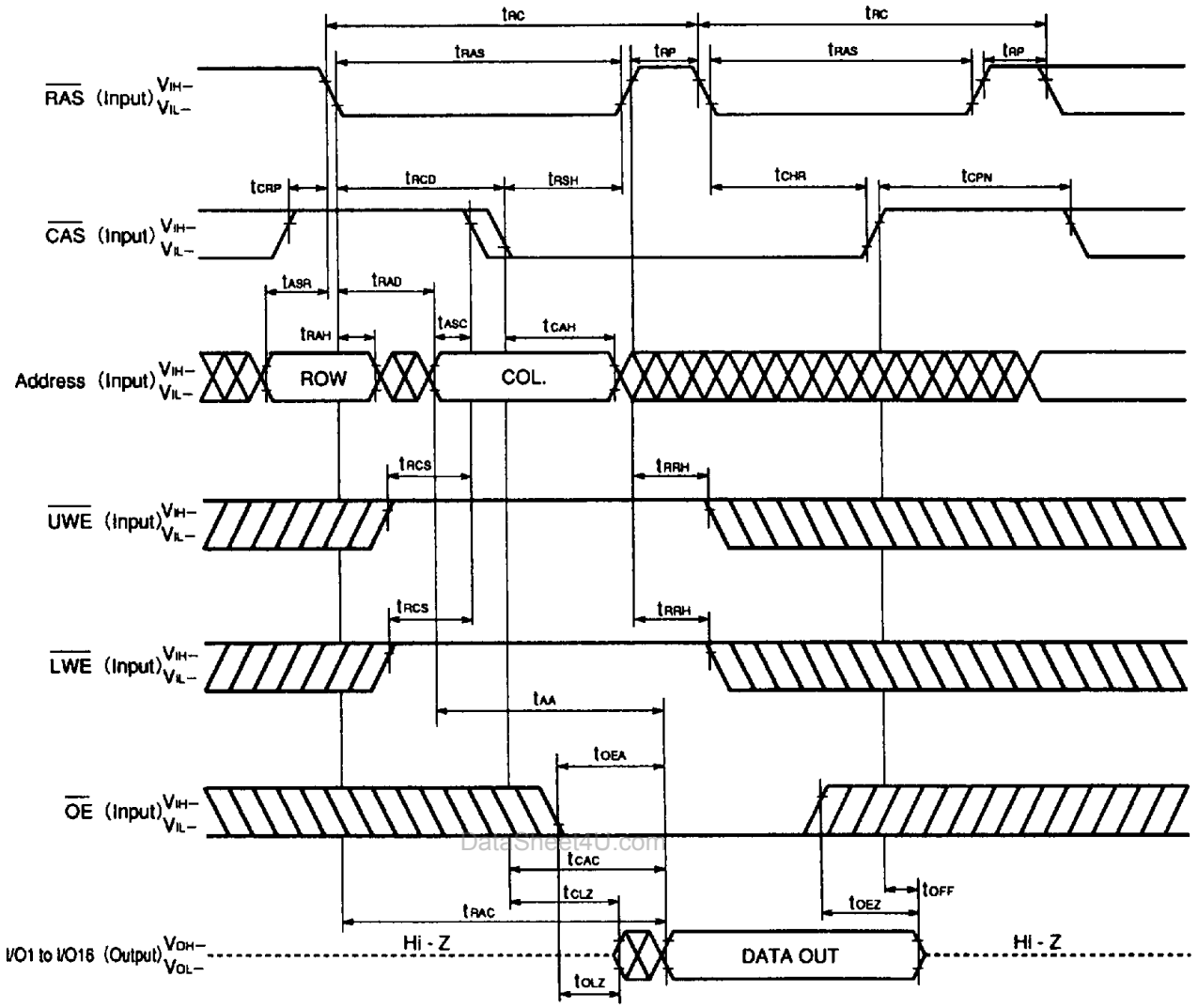
Remark Address, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi-Z

$\overline{RAS}$ ONLY REFRESH CYCLE

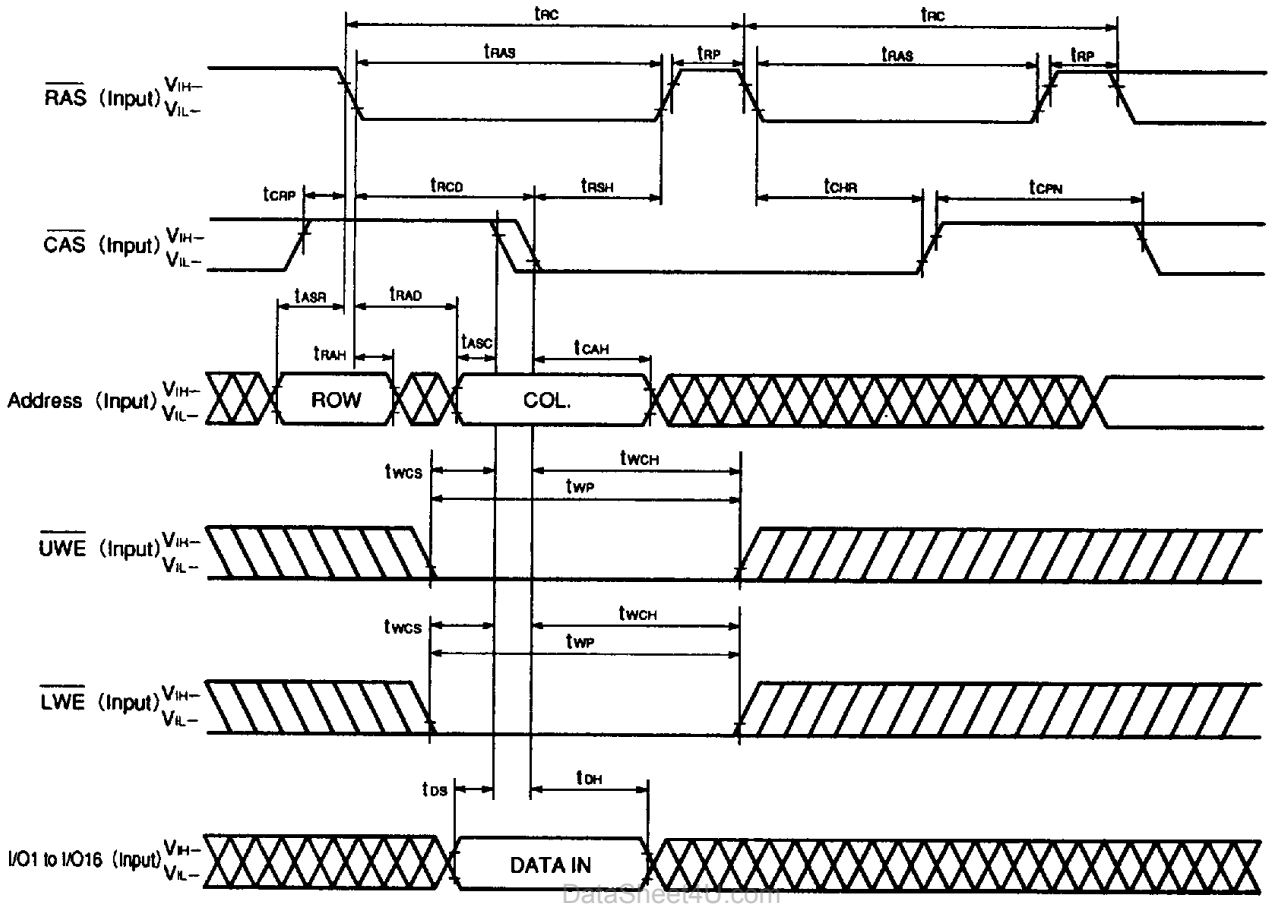


Remark $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ = Don't care
I/O1 to I/O16 = Hi-Z

HIDDEN REFRESH CYCLE (READ)

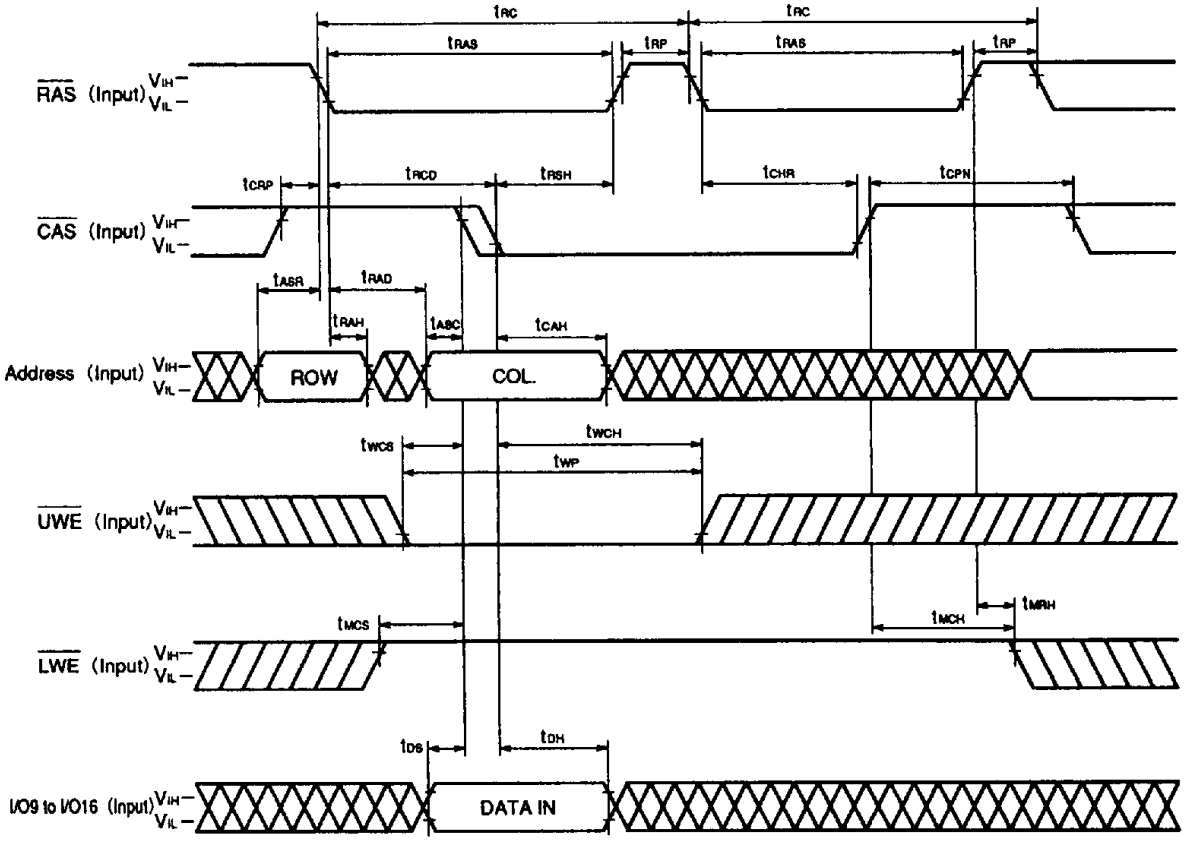


HIDDEN REFRESH CYCLE (WRITE)



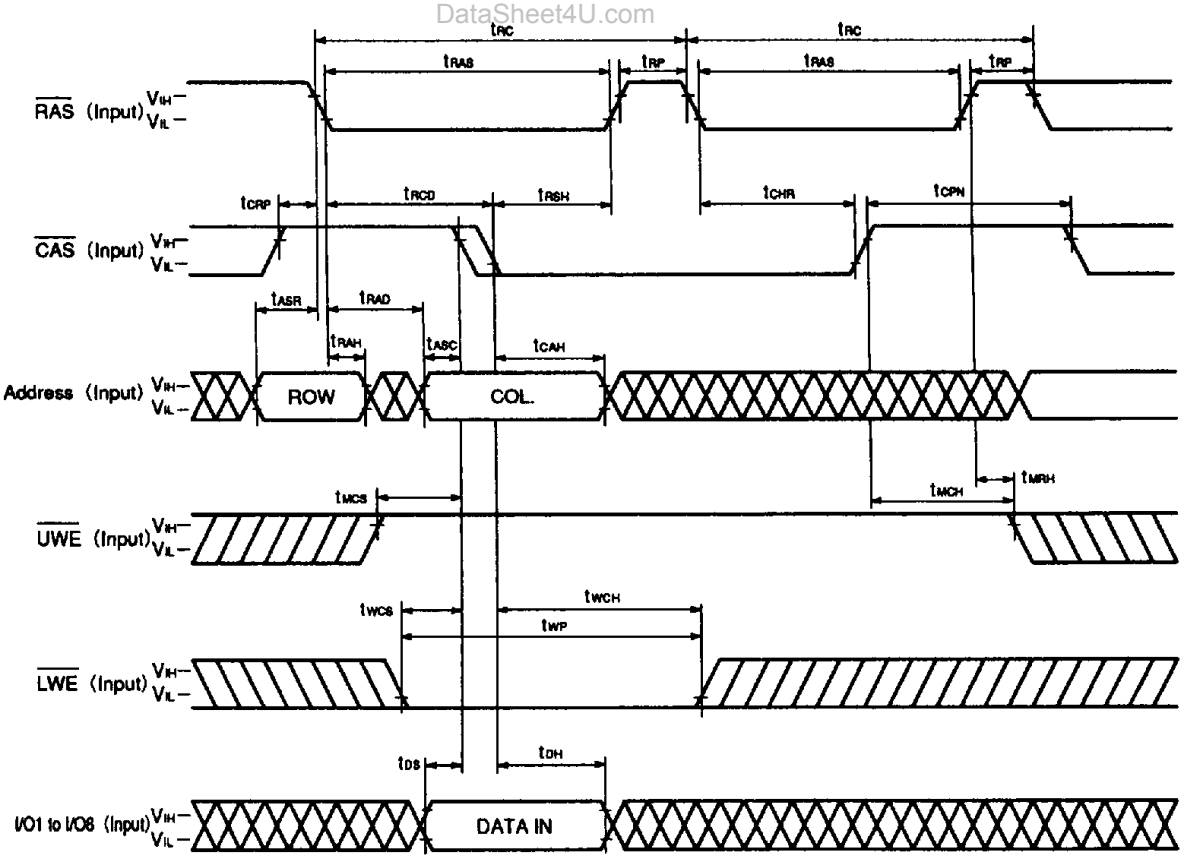
Remark $\overline{OE}$ = Don't care

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

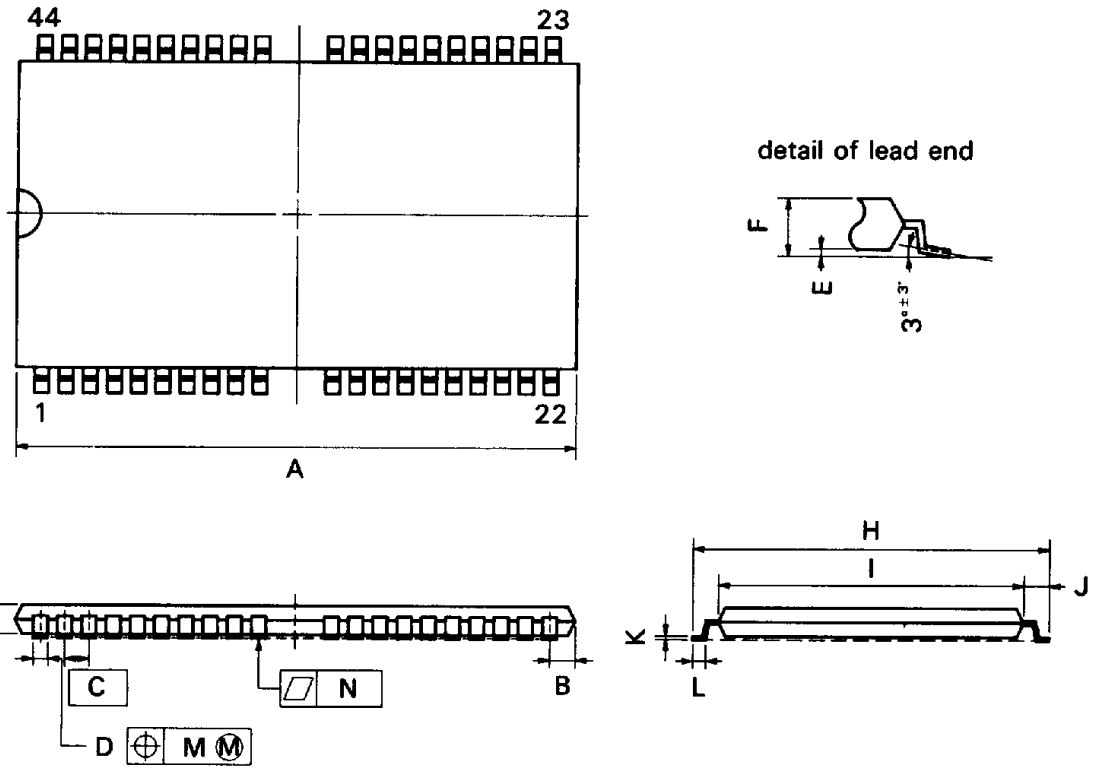
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

PACKAGE INFORMATIONS

44 PIN PLASTIC TSOP (400mil)



S44G5-80-7JF

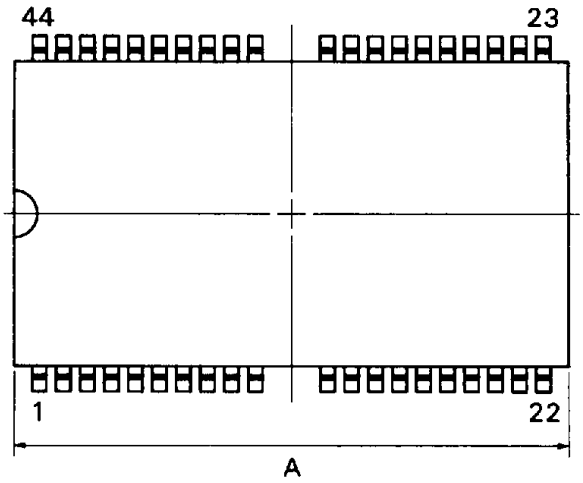
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

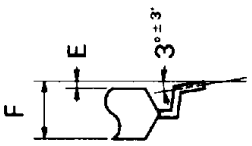
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004

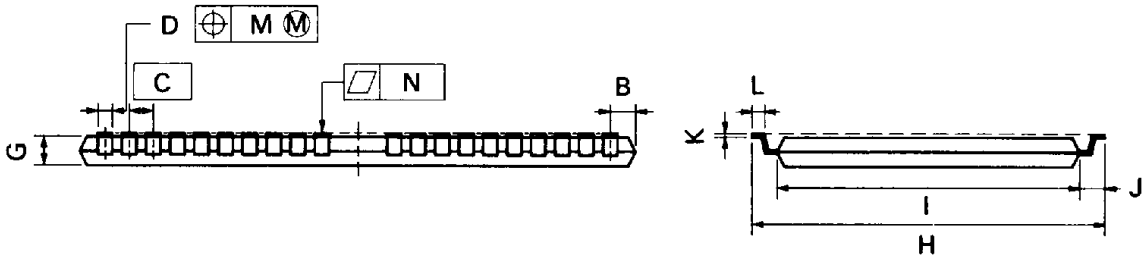
6427525 0041990 178 NECE

44 PIN PLASTIC TSOP (400mil)



detail of lead end





S44G5-80-7KF

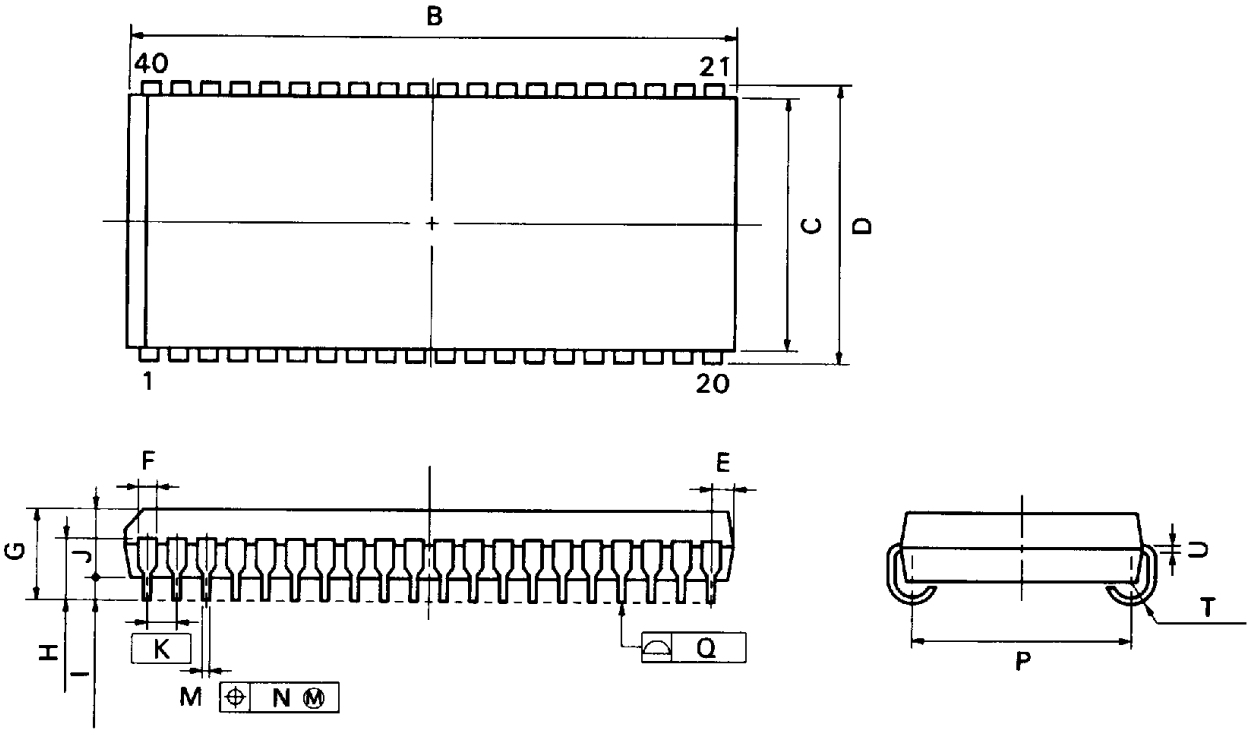
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX
B	1.0 MAX	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
E	$0.05^{+0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.006}$
M	0.13	0.005
N	0.10	0.004

6427525 0041991 004 NECE

40PIN PLASTIC SOJ (400 mil)



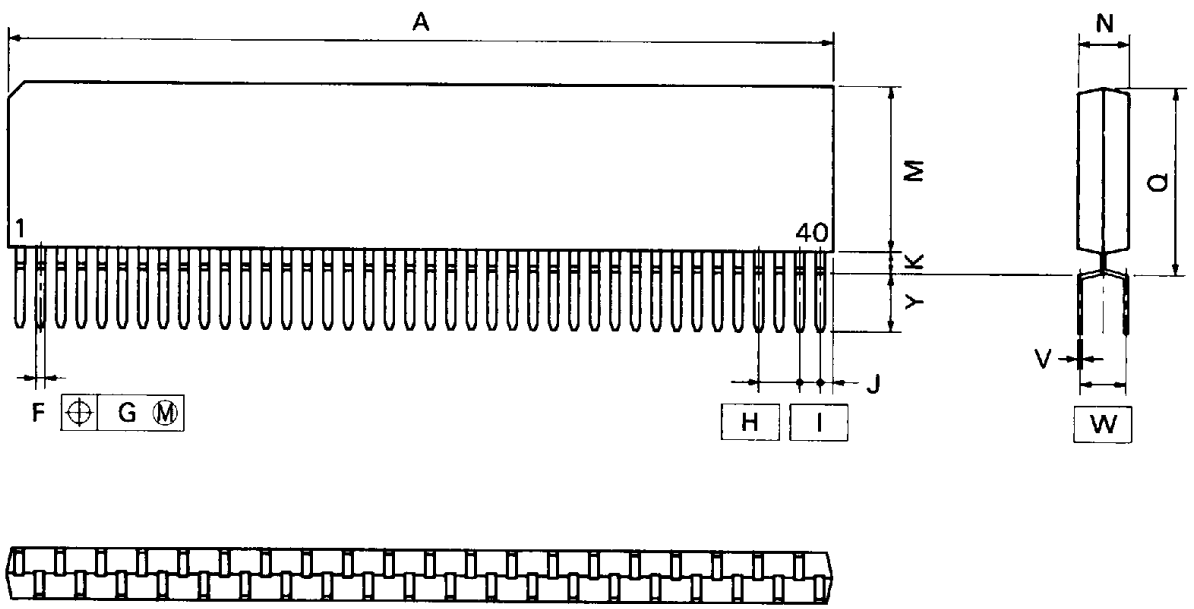
P40LE-400A-1

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	$11.18^{\pm 0.2}$	$0.440^{\pm 0.008}$
E	$1.08^{\pm 0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	$3.5^{\pm 0.2}$	$0.138^{\pm 0.008}$
H	$2.4^{\pm 0.2}$	$0.094^{+0.008}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$9.4^{\pm 0.20}$	$0.370^{\pm 0.008}$
Q	0.15	0.006
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

40 PIN PLASTIC ZIP(475mil)



P40V 100-475A

ITEM	MILLIMETERS	INCHES
A	51 23 MAX.	2.017 MAX.
F	$0\ 50^{\pm 0\ 10}$	$0.020^{+0\ 004}_{-0\ 005}$
G	0.25	0.010
H	2 54 (T.P.)	0.100 (T P.)
I	1.27 (T.P.)	0.050 (T P.)
J	0.85 MAX.	0.034 MAX
K	0.9 MIN.	0 035 MIN
M	10.5 MAX.	0.414 MAX.
N	$2.8^{\pm 0\ 2}$	$0\ 110^{+0\ 009}_{-0\ 008}$
Q	12.07 MAX	0.476 MAX.
V	$0.25^{+0\ 10}_{0\ 05}$	$0\ 010^{+0\ 004}_{-0\ 003}$
W	2.54 (T P)	0.100 (T.P)
Y	$3.25^{\pm 0\ 2}$	$0.128^{\pm 0\ 008}$

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices when soldering μPD42S4170, 424170, 42S4270, 424270.

TYPE OF SURFACE MOUNT DEVICE

μPD42S4170G5, 424170G5, 42S4270G5, 424270G5 (44-pin Plastic TSOP)

μPD42S4170LE, 424170LE, 42S4270LE, 424270LE (40-pin Plastic SOJ)

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD42S4170V, 424170V (40-pin Plastic ZIP)