

### 1M-BIT CMOS STATIC RAM

### 128K-WORD BY 8-BIT

#### Description

The  $\mu$ PD431000A is a high speed, low power, and 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The  $\mu$ PD431000A has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available. In addition to this, A and B versions are low voltage operations.

The  $\mu$ PD431000A is packed in 32-pin plastic DIP, 32-pin plastic SOP and 32-pin plastic TSOP (I).

#### Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation (A version:  $V_{CC} = 3.0$  to 5.5 V, B version:  $V_{CC} = 2.7$  to 5.5 V)
- Low  $V_{CC}$  data retention: 2.0 V (MIN.)
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby $\mu$ A (MAX.)	At data retention $\mu$ A (MAX.) <sup>Note1</sup>
$\mu$ PD431000A-xxL	70, 85	4.5 to 5.5	0 to 70	70	100	15
$\mu$ PD431000A-xxLL					20	
★ $\mu$ PD431000A-Axx	70 <sup>Note2</sup> , 100	3.0 to 5.5		35 <sup>Note3</sup>	13 <sup>Note5</sup>	3
$\mu$ PD431000A-Bxx	70 <sup>Note2</sup> , 100, 120, 150	2.7 to 5.5		30 <sup>Note4</sup>	11 <sup>Note6</sup>	

Notes 1.  $T_A \leq 40$  °C

2.  $V_{CC} = 4.5$  to 5.5 V
3. 70 mA ( $V_{CC} > 3.6$  V)
4. 70 mA ( $V_{CC} > 3.3$  V)
5. 20  $\mu$ A ( $V_{CC} > 3.6$  V)
6. 20  $\mu$ A ( $V_{CC} > 3.3$  V)

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

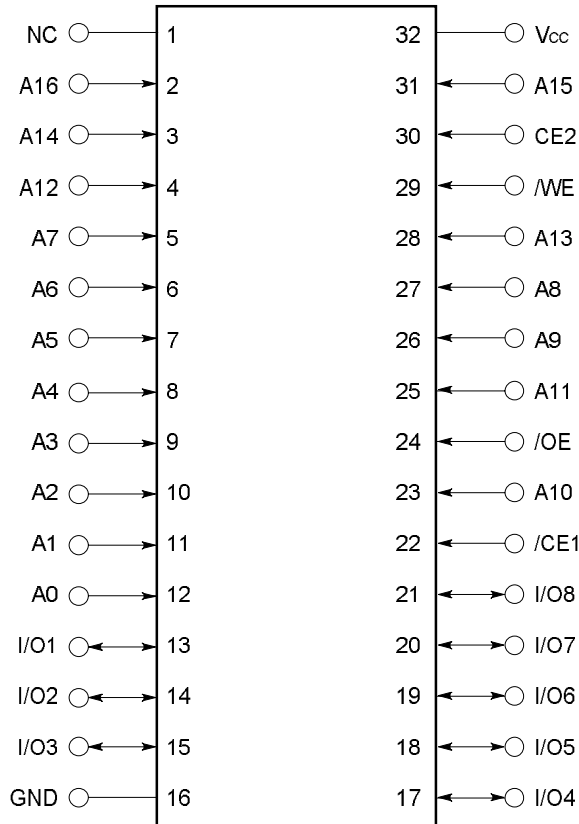
★ Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Remark
μPD431000ACZ-70L	32-pin Plastic DIP (600 mil)	70	4.5 to 5.5	0 to 70	L version
μPD431000ACZ-85L		85			
μPD431000ACZ-70LL		70			LL version
μPD431000ACZ-85LL		85			
μPD431000AGW-70L	32-pin Plastic SOP (13.34 mm (525))	70	4.5 to 5.5		L version
μPD431000AGW-85L		85			
μPD431000AGW-70LL		70			LL version
μPD431000AGW-85LL		85			
μPD431000AGW-A10		100	3.0 to 5.5		A version
μPD431000AGW-B10		100	2.7 to 5.5		B version
μPD431000AGW-B12		120			
μPD431000AGW-B15		150			
μPD431000AGZ-70LL-KJH	32-pin Plastic TSOP (I) (8 × 20) (Normal bent)	70	4.5 to 5.5		LL version
μPD431000AGZ-B10-KJH		100	2.7 to 5.5		B version
μPD431000AGZ-B15-KJH		150			
μPD431000AGZ-70LL-KKH	32-pin Plastic TSOP (I) (8 × 20) (Reverse bent)	70	4.5 to 5.5		LL version
μPD431000AGZ-B10-KKH		100	2.7 to 5.5		B version
μPD431000AGZ-B15-KKH		150			
μPD431000AGU-B10-9JH	32-pin Plastic TSOP (I) (8 × 13.4) (Normal bent)	100	2.7 to 5.5		B version
μPD431000AGU-B15-9JH		150			
μPD431000AGU-B10-9KH	32-pin Plastic TSOP (I) (8 × 13.4) (Reverse bent)	100	2.7 to 5.5		B version

Pin Configurations (Marking Side)

/xxx indicates active low signal.

32-pin Plastic DIP (600 mil)  
 [ μPD431000ACZ-xxL ]  
 [ μPD431000ACZ-xxLL ]



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- A0 - A16 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

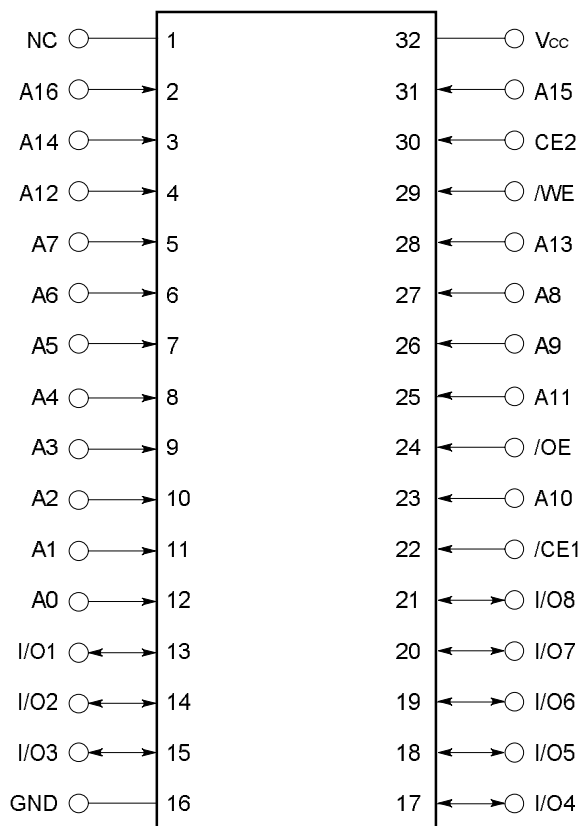
32-pin Plastic SOP [ 13.34 mm (525) ]

[ μPD431000AGW-xxL ]

[ μPD431000AGW -xxLL ]

[ μPD431000AGW -Axx ]

[ μPD431000AGW -Bxx ]



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- A0 - A16 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8x20) (Normal bent)

[ μPD431000AGZ-xxLL-KJH ]

[ μPD431000AGZ-Bxx-KJH ]



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32-pin Plastic TSOP (I) (8x20) (Reverse bent)

[ μPD431000AGZ-xxLL-KKH ]

[ μPD431000AGZ-Bxx-KKH ]



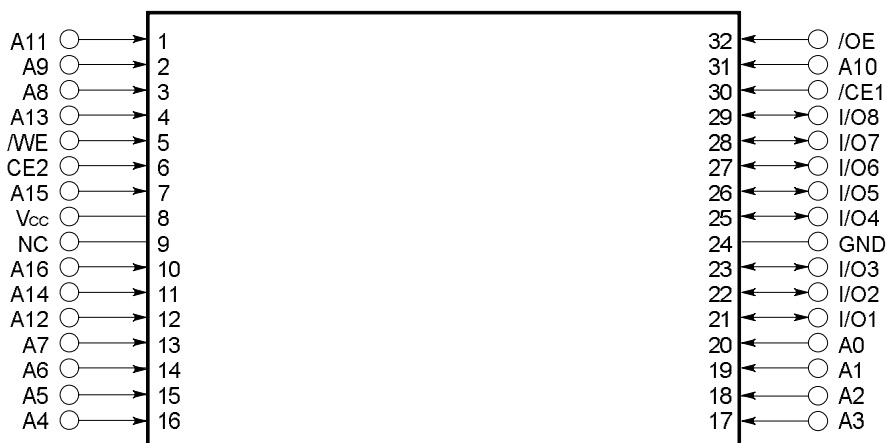
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- Vcc : Power supply
- GND : Ground
- NC : No connection

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8x13.4) (Normal bent)

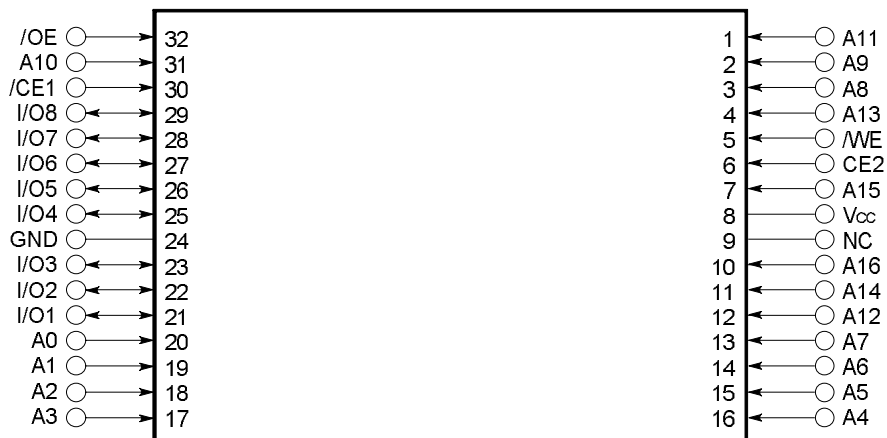
[ μPD431000AGU-Bxx-9JH ]



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32-pin Plastic TSOP (I) (8x13.4) (Reverse bent)

[ μPD431000AGU-Bxx-9KH ]

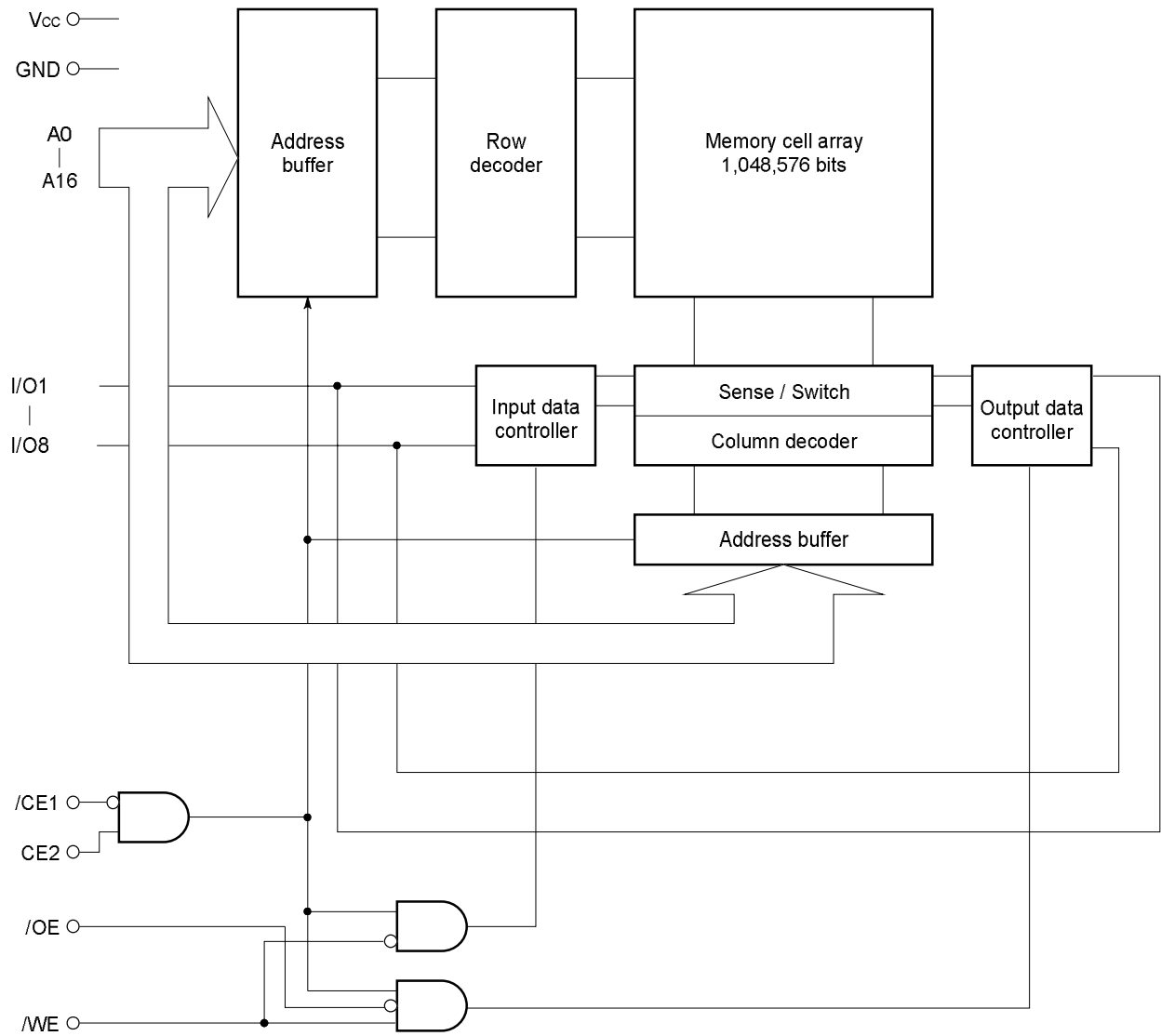


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- A0 - A16 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

**Block Diagram**



**Truth Table**

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	x	x	x	Not selected	High impedance	I <sub>SB</sub>
x	L	x	x			
L	H	H	H	Output disable		I <sub>CCA</sub>
L	H	L	H	Read	D <sub>OUT</sub>	
L	H	x	L	Write	D <sub>IN</sub>	

**Remark** x : Don't care

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.5 <sup>Note</sup> to +7.0	V
Input / Output voltage	V <sub>I</sub>		-0.5 <sup>Note</sup> to V <sub>CC</sub> + 0.5	V
Operating ambient temperature	T <sub>A</sub>		0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Note** -3.0 V (MIN.) (Pulse width: 30 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	μPD431000A-xxL		μPD431000A-Axx		μPD431000A-Bxx		Unit
			μPD431000A-xxLL		MIN.	MAX.	MIN.	MAX.	
			MIN.	MAX.					
Supply voltage	V <sub>CC</sub>		4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> +0.5	2.2	V <sub>CC</sub> +0.5	2.2	V <sub>CC</sub> +0.5	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>	+0.8	-0.3 <sup>Note</sup>	+0.5	-0.3 <sup>Note</sup>	+0.5	V
Operating ambient temperature	T <sub>A</sub>		0	70	0	70	0	70	°C

**Note** -3.0 V (MIN.) (Pulse width: 30 ns)

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			6	pF
Input / Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			10	pF

- Remarks**
1. V<sub>IN</sub> : Input voltage  
V<sub>I/O</sub> : Input / Output voltage
  2. These parameters are periodically sampled and not 100% tested.



DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition	μPD431000A-xxL			μPD431000A-xxLL			μPD431000A-Axx			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I <sub>I</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current	I <sub>LO</sub>	V <sub>I/O</sub> = 0 V to V <sub>CC</sub> , /CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or /WE = V <sub>IL</sub> or /OE = V <sub>IH</sub>	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I <sub>CCA1</sub>	/CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA		40	70		40	70		40	70	mA
		Minimum cycle time V <sub>CC</sub> ≤ 3.6 V			-			-			35	
	I <sub>CCA2</sub>	/CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA			15			15			15	
		V <sub>CC</sub> ≤ 3.6 V			-			-			8	
I <sub>CCA3</sub>	/CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V, Cycle = 1 MHz, I <sub>I/O</sub> = 0 mA, V <sub>IL</sub> ≤ 0.2 V, V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V			10			10			10		
	V <sub>CC</sub> ≤ 3.6 V			-			-			8		
Standby supply current	I <sub>SB</sub>	/CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>			3			3			3	mA
		V <sub>CC</sub> ≤ 3.6 V			-			-			2	
	I <sub>SB1</sub>	/CE1 ≥ V <sub>CC</sub> - 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V		2	100		1	20		1	20	μA
		V <sub>CC</sub> ≤ 3.6 V			-			-		0.5	13	
I <sub>SB2</sub>	CE2 ≤ 0.2 V		2	100		1	20		1	20		
	V <sub>CC</sub> ≤ 3.6 V			-			-		0.5	13		
High level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 4.5 V	2.4			2.4			2.4			V
		I <sub>OH</sub> = -0.5 mA	-			-			2.4			
	V <sub>OH2</sub>	I <sub>OH</sub> = -0.02 mA	-			-			V <sub>CC</sub> -0.1			
Low level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 4.5 V			0.4			0.4			0.4	V
		I <sub>OL</sub> = 1.0 mA			-			-			0.4	
	V <sub>OL2</sub>	I <sub>OL</sub> = 0.02 mA			-			-			0.1	

Remarks 1. V<sub>IN</sub> : Input voltage

V<sub>I/O</sub> : Input / Output voltage

2. These DC characteristics are in common regardless of package types and access time.

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)**

Parameter	Symbol	Test condition	μPD431000A-Bxx			Unit
			MIN.	TYP.	MAX.	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-1.0		+1.0	μA
I/O leakage current	I <sub>LO</sub>	V <sub>I/O</sub> = 0 V to V <sub>CC</sub> , /CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or /WE = V <sub>IL</sub> or /OE = V <sub>IH</sub>	-1.0		+1.0	μA
Operating supply current	I <sub>CCA1</sub>	/CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA Minimum cycle time	V <sub>CC</sub> ≤ 3.3 V	40	70	mA
					30	
	I <sub>CCA2</sub>	/CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA	V <sub>CC</sub> ≤ 3.3 V		15	
					7	
I <sub>CCA3</sub>	/CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V, Cycle = 1 MHz, I <sub>I/O</sub> = 0 mA, V <sub>IL</sub> ≤ 0.2 V, V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V	V <sub>CC</sub> ≤ 3.3 V		10		
				7		
Standby supply current	I <sub>SB</sub>	/CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	V <sub>CC</sub> ≤ 3.3 V		3	mA
					2	
	I <sub>SB1</sub>	/CE1 ≥ V <sub>CC</sub> - 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V	V <sub>CC</sub> ≤ 3.3 V	1	20	μA
				0.5	11	
I <sub>SB2</sub>	CE2 ≤ 0.2 V	V <sub>CC</sub> ≤ 3.3 V	1	20		
			0.5	11		
High level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 4.5 V		2.4		V
			I <sub>OH</sub> = -0.5 mA		2.4	
	V <sub>OH2</sub>	I <sub>OH</sub> = -0.02 mA	V <sub>CC</sub> -0.1			
Low level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 4.5 V			0.4	V
			I <sub>OL</sub> = 1.0 mA			
	V <sub>OL2</sub>	I <sub>OL</sub> = 0.02 mA			0.1	

**Remarks 1.** V<sub>IN</sub> : Input voltage

V<sub>I/O</sub> : Input / Output voltage

**2.** These DC characteristics are in common regardless of package types and access time.

**AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

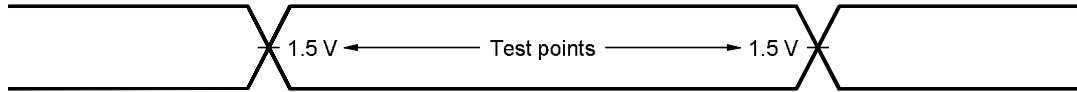
**AC Test Conditions**

**Input Waveform (Rise and Fall Time ≤ 5 ns)**

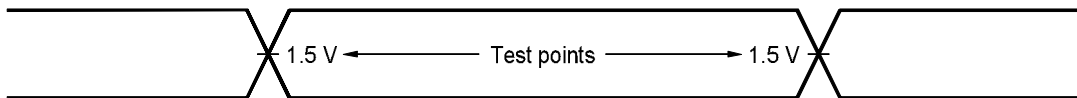
Input pulse levels

0.8 V to 2.2 V : μPD431000A-xxL, 431000A-xxLL

0.5 V to 2.2 V : μPD431000A-Axx, 431000A-Bxx



**Output Waveform**



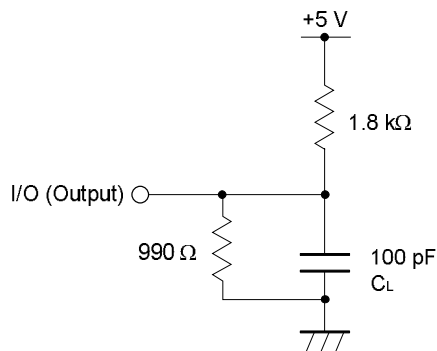
**Output Load**

AC characteristics should be measured with the following output load conditions.

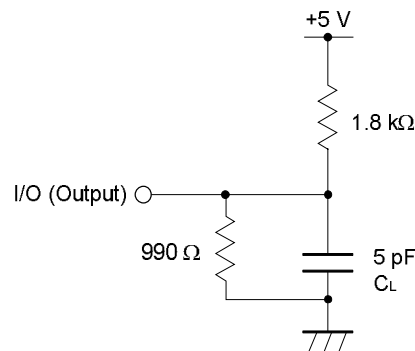
Part number	Output load condition	
	tAA, tCO1, tCO2, tOE, tOH	tLZ1, tLZ2, tOLZ, tHZ1, tHZ2, tOHZ, tWHZ, tOW
μPD431000A-A10 μPD431000A-B10, 431000A-B12	1TTL + 50 pF	1TTL + 5 pF
μPD431000A-B15	1TTL + 100 pF	1TTL + 5 pF
μPD431000A-70L, 431000A-85L μPD431000A-70LL, 431000A-85LL	See Figure 1	See Figure 2

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**Figure 1**



**Figure 2**



**Remark** C<sub>L</sub> includes capacitance of the probe and jig, and stray capacitance.

★ Read Cycle (1/2)

Parameter	Symbol	V <sub>CC</sub> ≥ 4.5 V				V <sub>CC</sub> ≥ 3.0 V		Unit	Condition
		μPD431000A-70 μPD431000A-Axx μPD431000A-Bxx		μPD431000A-85		μPD431000A-A10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t <sub>RC</sub>	70		85		100		ns	
Address access time	t <sub>AA</sub>		70		85		100	ns	Note
/CE1 access time	t <sub>CO1</sub>		70		85		100	ns	
CE2 access time	t <sub>CO2</sub>		70		85		100	ns	
/OE to output valid	t <sub>OE</sub>		35		45		50	ns	
Output hold from address change	t <sub>OH</sub>	10		10		10		ns	
/CE1 to output in low impedance	t <sub>LZ1</sub>	10		10		10		ns	
CE2 to output in low impedance	t <sub>LZ2</sub>	10		10		10		ns	
/OE to output in low impedance	t <sub>OLZ</sub>	5		5		5		ns	
/CE1 to output in high impedance	t <sub>HZ1</sub>		25		30		35	ns	
CE2 to output in high impedance	t <sub>HZ2</sub>		25		30		35	ns	
/OE to output in high impedance	t <sub>OHZ</sub>		25		30		35	ns	

Note See the output load.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

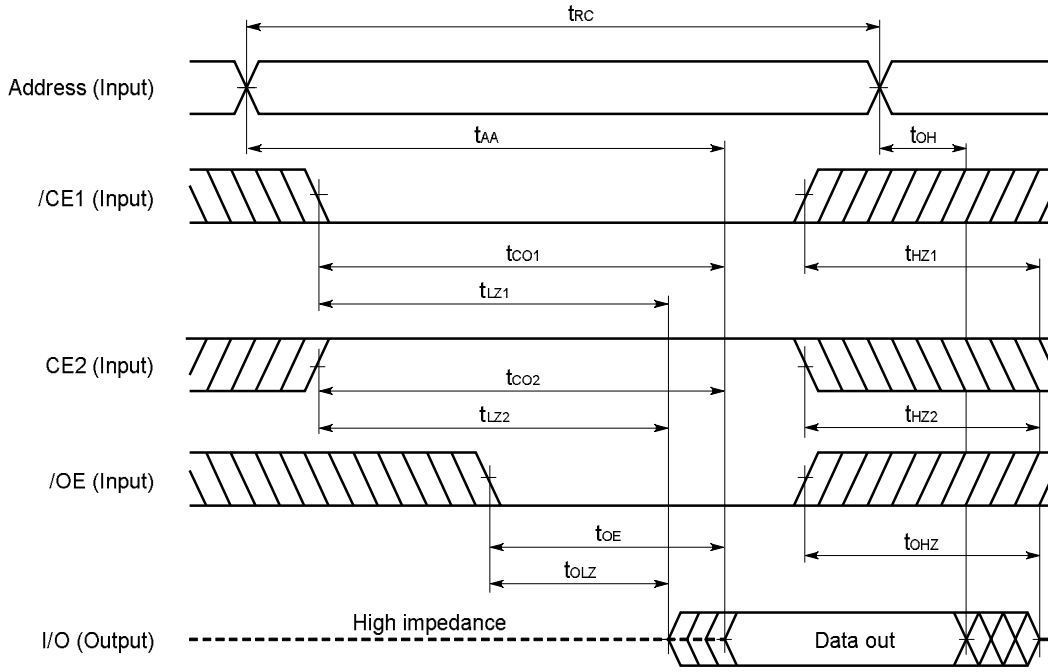
Read Cycle (2/2)

Parameter	Symbol	V <sub>CC</sub> ≥ 2.7 V						Unit	Condition
		μPD431000A-B10		μPD431000A-B12		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t <sub>RC</sub>	100		120		150		ns	
Address access time	t <sub>AA</sub>		100		120		150	ns	Note
/CE1 access time	t <sub>CO1</sub>		100		120		150	ns	
CE2 access time	t <sub>CO2</sub>		100		120		150	ns	
/OE to output valid	t <sub>OE</sub>		50		60		70	ns	
Output hold from address change	t <sub>OH</sub>	10		10		10		ns	
/CE1 to output in low impedance	t <sub>LZ1</sub>	10		10		10		ns	
CE2 to output in low impedance	t <sub>LZ2</sub>	10		10		10		ns	
/OE to output in low impedance	t <sub>OLZ</sub>	5		5		5		ns	
/CE1 to output in high impedance	t <sub>HZ1</sub>		35		40		50	ns	
CE2 to output in high impedance	t <sub>HZ2</sub>		35		40		50	ns	
/OE to output in high impedance	t <sub>OHZ</sub>		35		40		50	ns	

Note See the output load.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



**Remark** In read cycle,  $\overline{WE}$  should be fixed to high level.

★ Write Cycle (1/2)

Parameter	Symbol	V <sub>CC</sub> ≥ 4.5 V				V <sub>CC</sub> ≥ 3.0 V		Unit	Condition
		μPD431000A-70 μPD431000A-Axx μPD431000A-Bxx		μPD431000A-85		μPD431000A-A10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t <sub>WC</sub>	70		85		100		ns	
/CE1 to end of write	t <sub>CW1</sub>	55		70		80		ns	
CE2 to end of write	t <sub>CW2</sub>	55		70		80		ns	
Address valid to end of write	t <sub>AW</sub>	55		70		80		ns	
Address setup time	t <sub>AS</sub>	0		0		0		ns	
Write pulse width	t <sub>WP</sub>	50		60		60		ns	
Write recovery time	t <sub>WR</sub>	5		5		0		ns	
Data valid to end of write	t <sub>DW</sub>	35		35		60		ns	
Data hold time	t <sub>DH</sub>	0		0		0		ns	
/WE to output in high impedance	t <sub>WHZ</sub>		25		30		35	ns	Note
Output active from end of write	t <sub>OW</sub>	5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

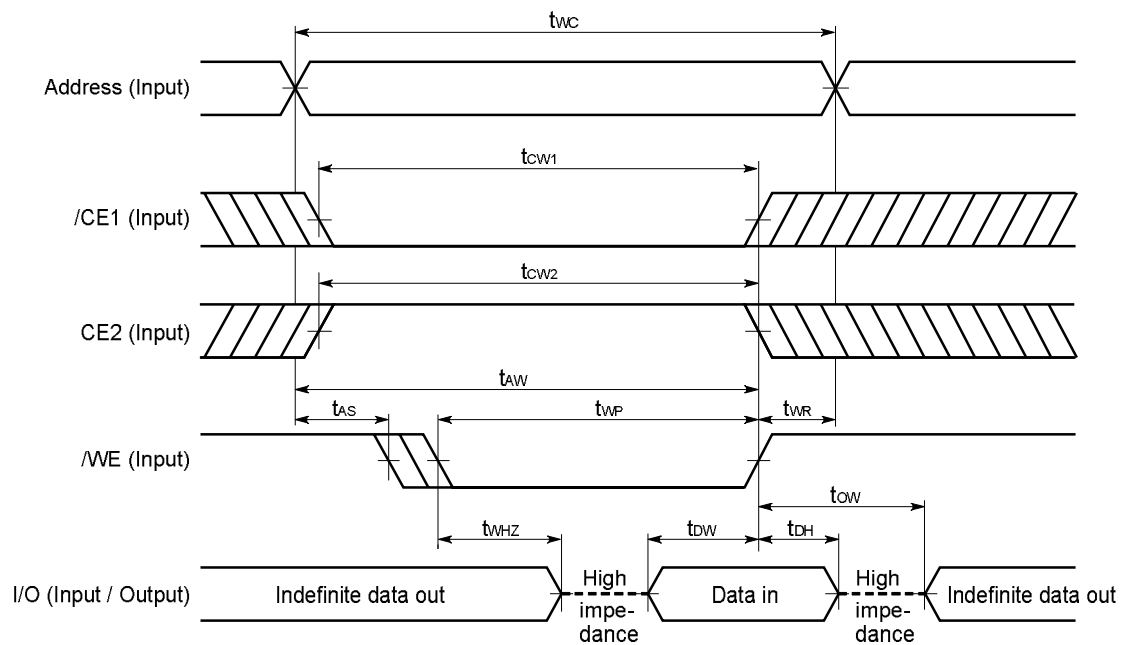
Write Cycle (2/2)

Parameter	Symbol	V <sub>CC</sub> ≥ 2.7 V						Unit	Condition
		μPD431000A-B10		μPD431000A-B12		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t <sub>WC</sub>	100		120		150		ns	
/CE1 to end of write	t <sub>CW1</sub>	80		100		120		ns	
CE2 to end of write	t <sub>CW2</sub>	80		100		120		ns	
Address valid to end of write	t <sub>AW</sub>	80		100		120		ns	
Address setup time	t <sub>AS</sub>	0		0		0		ns	
Write pulse width	t <sub>WP</sub>	60		85		100		ns	
Write recovery time	t <sub>WR</sub>	0		0		0		ns	
Data valid to end of write	t <sub>DW</sub>	60		60		80		ns	
Data hold time	t <sub>DH</sub>	0		0		0		ns	
/WE to output in high impedance	t <sub>WHZ</sub>		35		40		50	ns	Note
Output active from end of write	t <sub>OW</sub>	5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

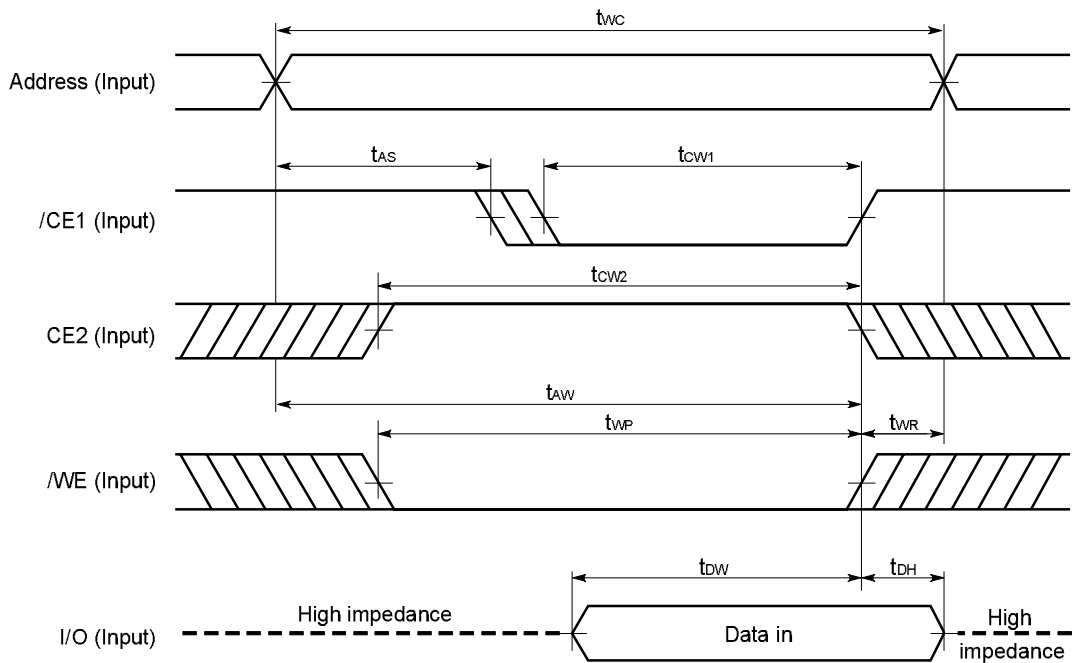
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

- Remarks**
1. Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.
  2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
  3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

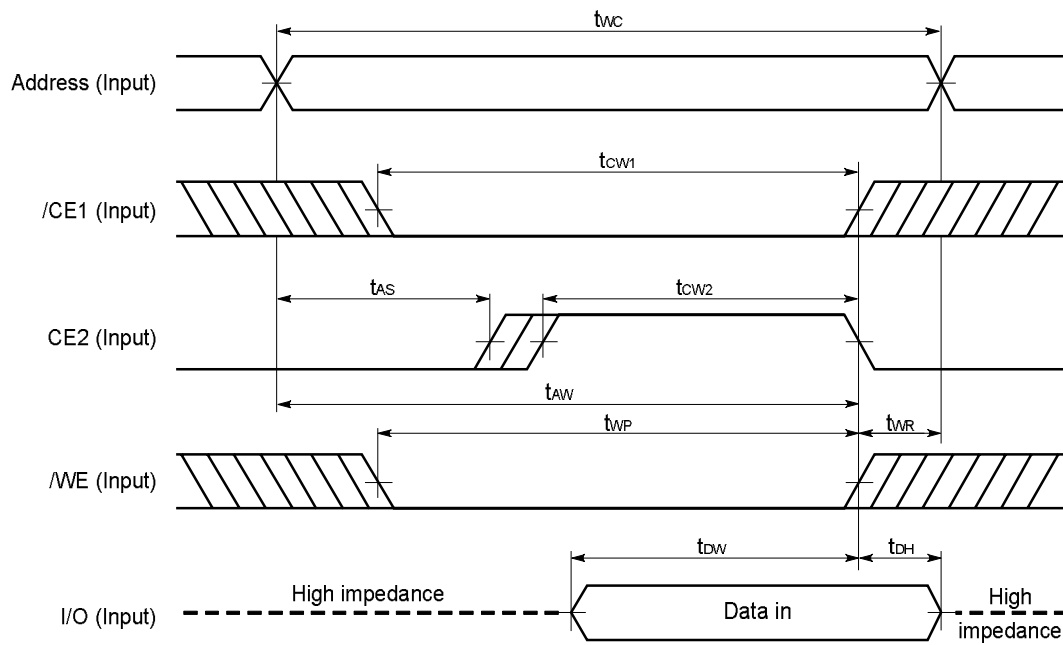


- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.



**Write Cycle Timing Chart 3 (CE2 Controlled)**



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Low Vcc Data Retention Characteristics (T<sub>A</sub> = 0 to 70 °C)

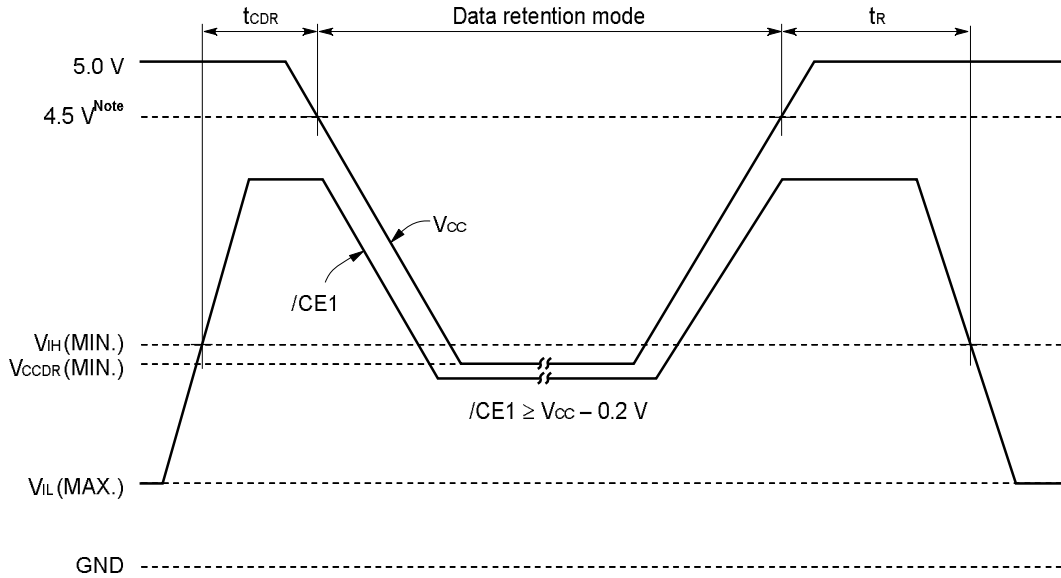
Parameter	Symbol	Test Condition	μPD431000A-xxL			μPD431000A-xxLL μPD431000A-Axx μPD431000A-Bxx			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V <sub>CCDR1</sub>	/CE1 ≥ V <sub>CC</sub> - 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V	2.0		5.5	2.0		5.5	V
	V <sub>CCDR2</sub>	CE2 ≤ 0.2 V	2.0		5.5	2.0		5.5	
Data retention supply current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3.0 V, /CE1 ≥ V <sub>CC</sub> - 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V or CE2 ≤ 0.2 V		1	50 <sup>Note1</sup>		0.5	10 <sup>Note2</sup>	μA
	I <sub>CCDR2</sub>	V <sub>CC</sub> = 3.0 V, CE2 ≤ 0.2 V		1	50 <sup>Note1</sup>		0.5	10 <sup>Note2</sup>	
Chip deselection to data retention mode	t <sub>CDR</sub>		0			0			ns
Operation recovery time	t <sub>R</sub>		5			5			ms

Notes 1. 15 μA (T<sub>A</sub> ≤ 40 °C)

2. 3 μA (T<sub>A</sub> ≤ 40 °C)

**Data Retention Timing Chart**

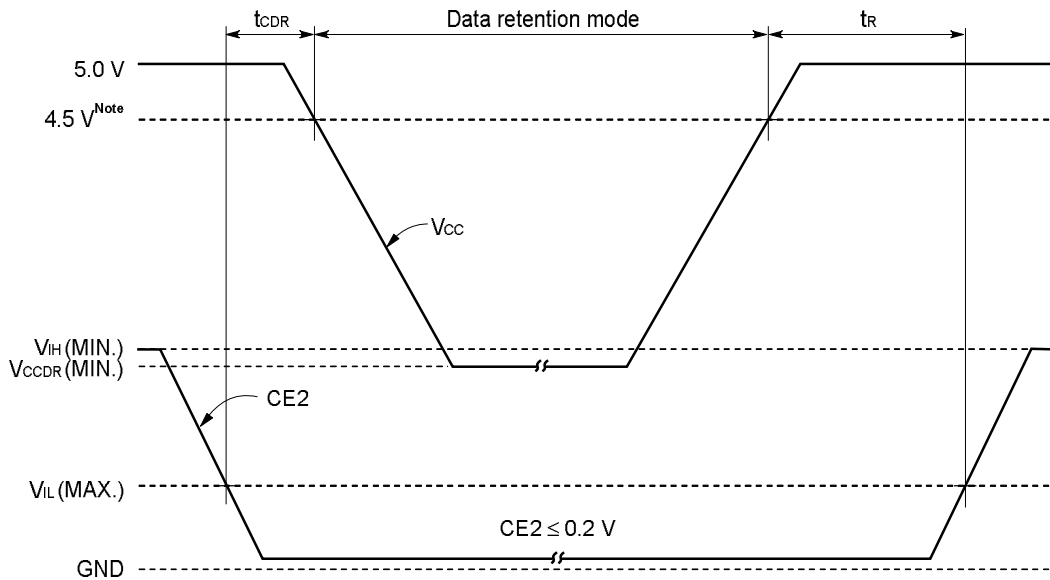
**(1) /CE1 Controlled**



**Note** A version : 3.0 V, B version : 2.7 V

**Remark** On the data retention mode by controlling /CE1, the input level of CE2 must be  $CE2 \geq V_{cc} - 0.2 V$  or  $CE2 \leq 0.2 V$ . The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

**(2) CE2 Controlled**

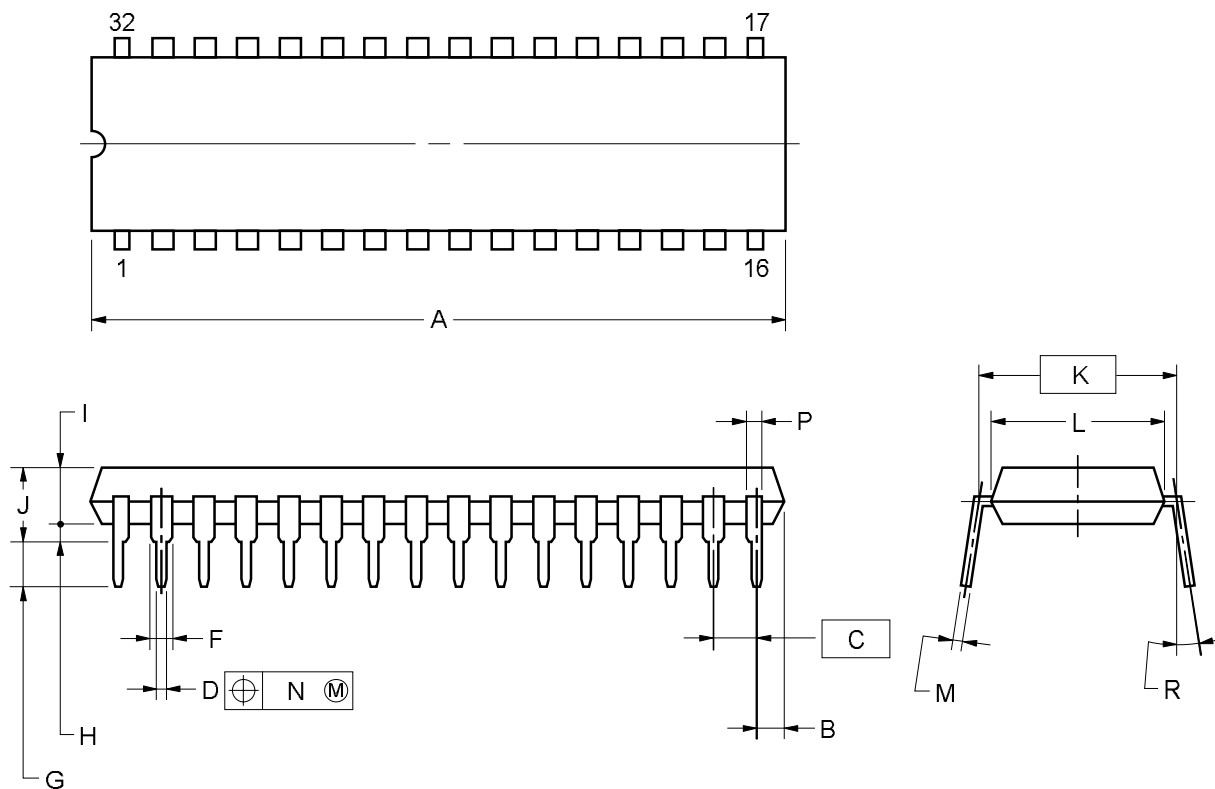


**Note** A version : 3.0 V, B version : 2.7 V

**Remark** The other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

32PIN PLASTIC DIP (600 mil)



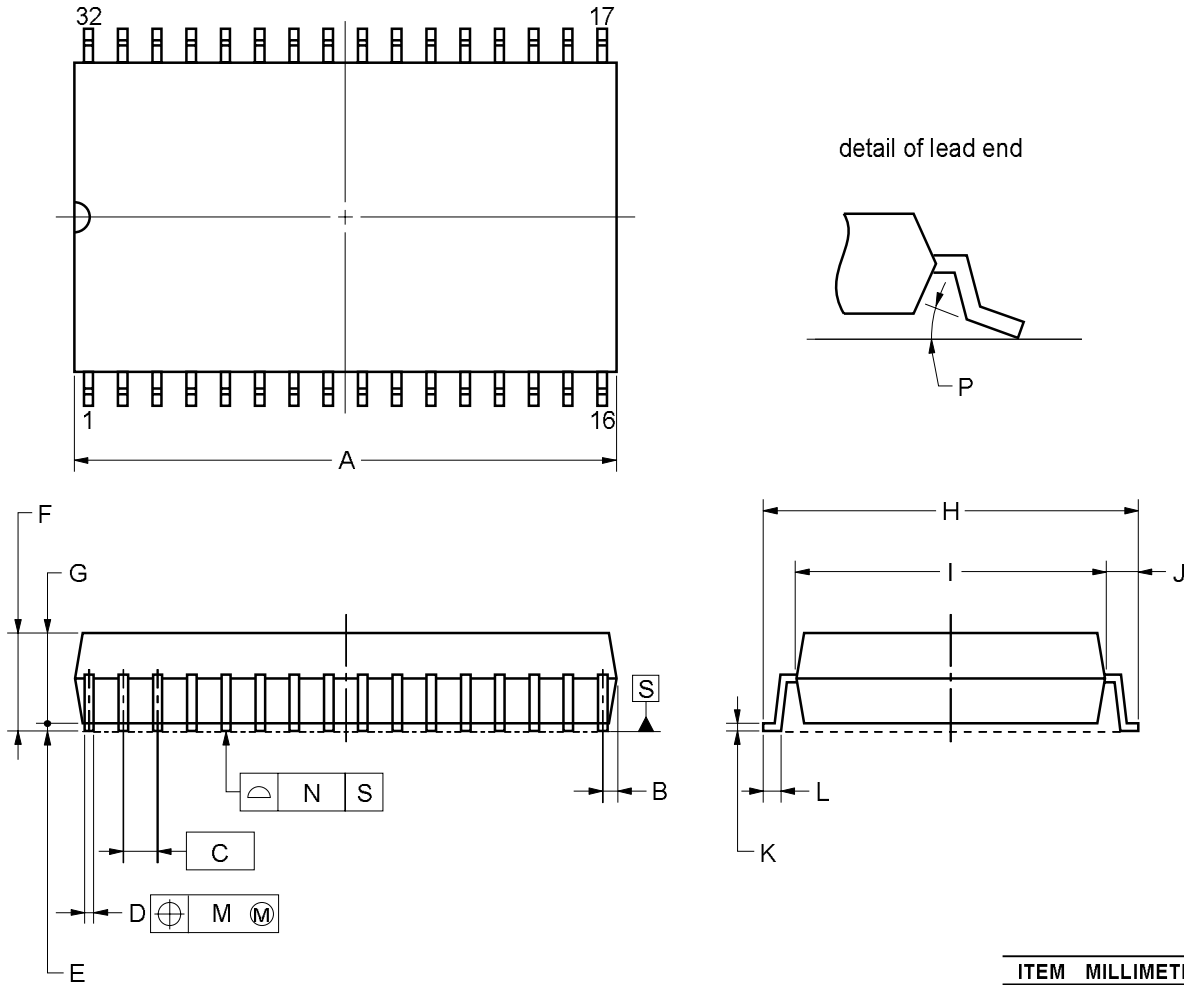
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	40.64 MAX.	1.600 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	1.1 MIN.	0.043 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P32C-100-600A-1

★ 32-PIN PLASTIC SOP (13.34 mm (525))



**NOTE**  
 Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	20.61 MAX.
B	0.78 MAX.
C	1.27 (T.P.)
D	0.40 <sup>+0.10</sup> <sub>-0.05</sub>
E	0.15±0.05
F	2.95 MAX.
G	2.7
H	14.1±0.3
I	11.3
J	1.4±0.2
K	0.20 <sup>+0.10</sup> <sub>-0.05</sub>
L	0.8±0.2
M	0.12
N	0.10
P	3° <sup>+7°</sup> <sub>-3°</sub>

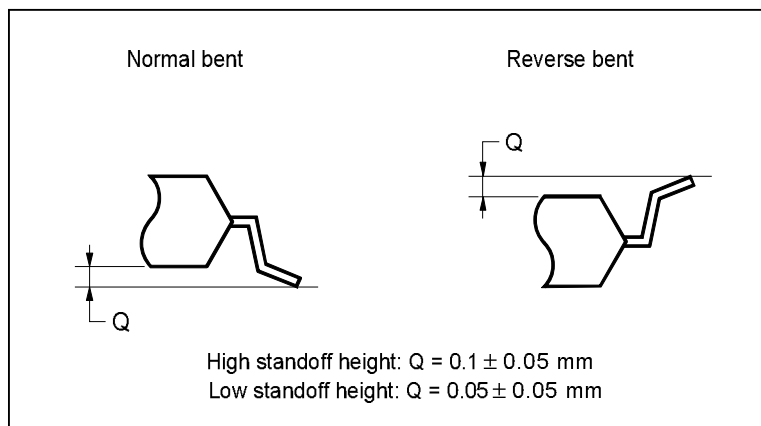
P32GW-50-525A-1

**Notice of change in 32-pin plastic TSOP (I) (8 × 20) standoff height**

We are changing the 32-pin plastic TSOP (I) (8 × 20) standoff height  $0.05 \pm 0.05$  mm (low standoff height) to  $0.1 \pm 0.05$  mm (high standoff height). Each lot version is identified by the fifth character of the lot number.

**Difference between high standoff height and low standoff height.**

**Detail of lead end**

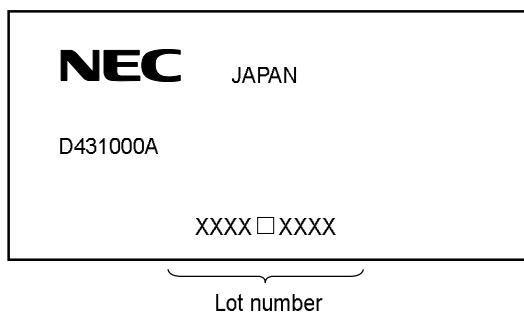


**Identification of each lot version**

Each lot version is identified by the fifth character of the lot number.

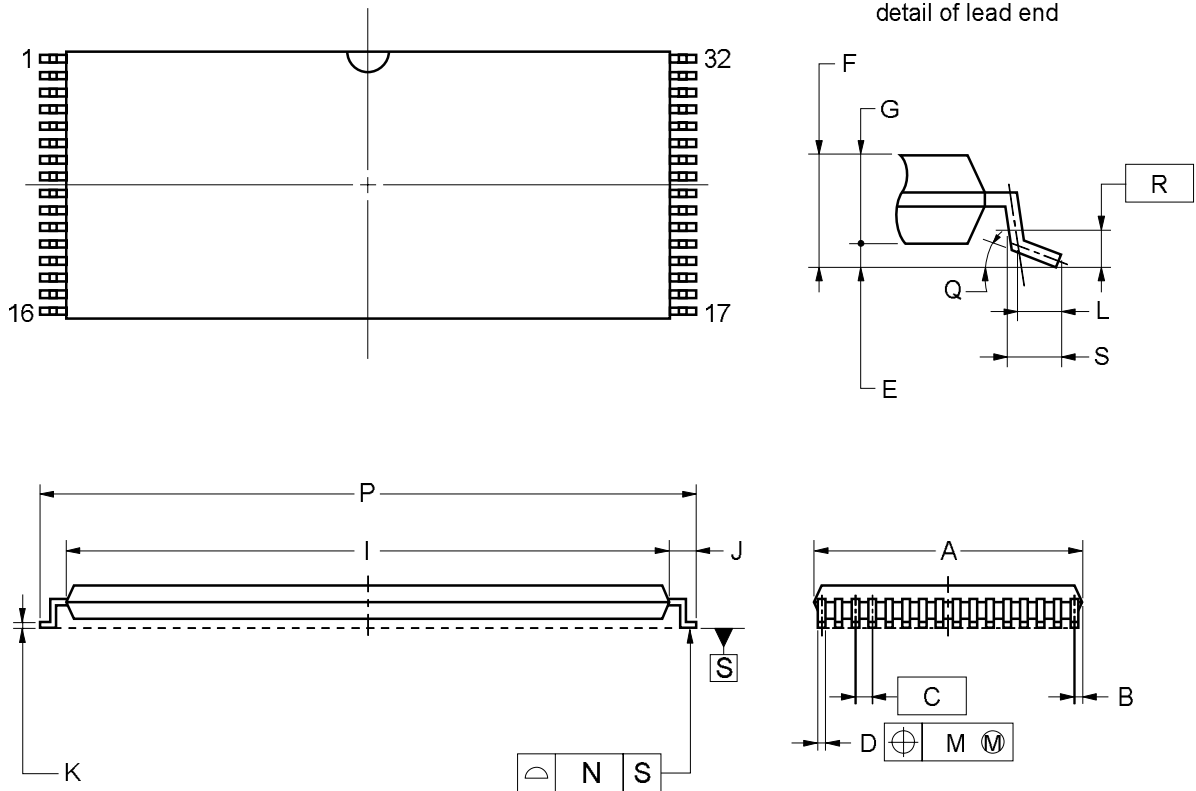
Fifth character of the lot number	Lot version	Standoff height
R	R version	$0.1 \pm 0.05$ mm (High standoff height)
H	H version	$0.05 \pm 0.05$ mm (Low standoff height)

**Marking Example**



High standoff height

★ 32-PIN PLASTIC TSOP(I) (8x20)



NOTES

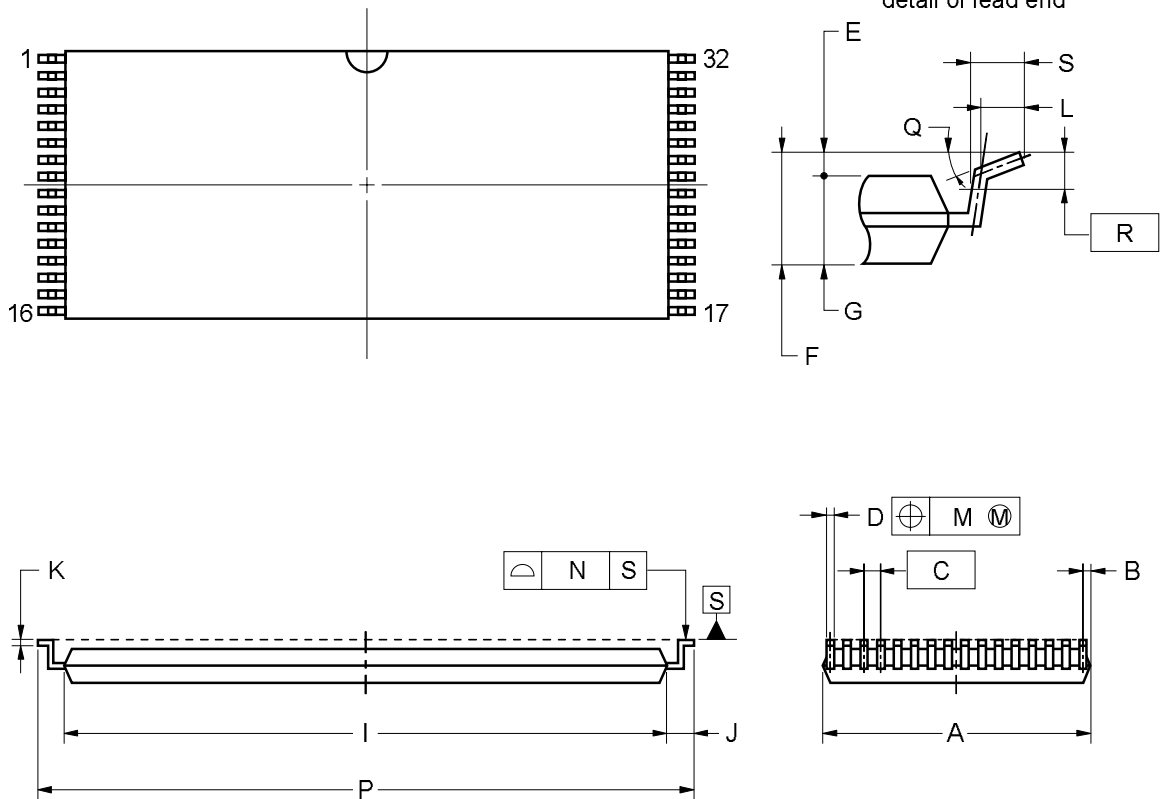
1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	3 <sup>+5°</sup> <sub>-3°</sub>
R	0.25
S	0.60±0.15

S32GZ-50-KJH1-1

High standoff height

★ 32-PIN PLASTIC TSOP(I) (8x20)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

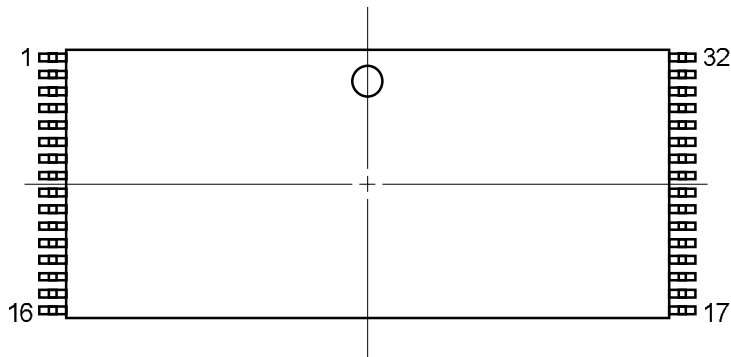
ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	3° <sup>+5°</sup> <sub>-3°</sub>
R	0.25
S	0.60±0.15

S32GZ-50-KKH1-1

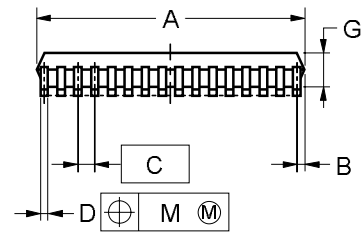
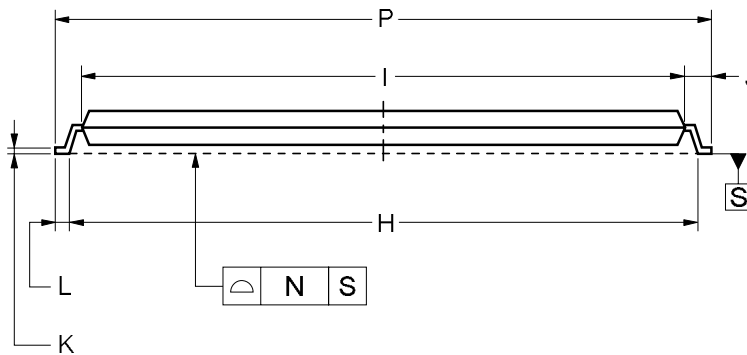
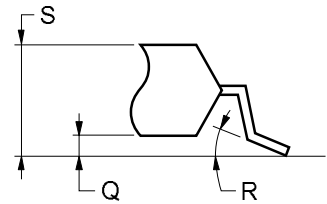


Low standoff height

★ 32-PIN PLASTIC TSOP (I) (8x20)



detail of lead end



NOTES

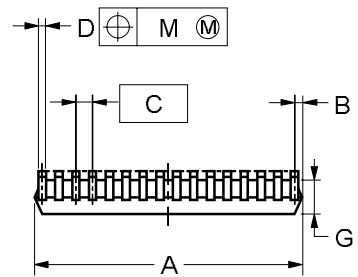
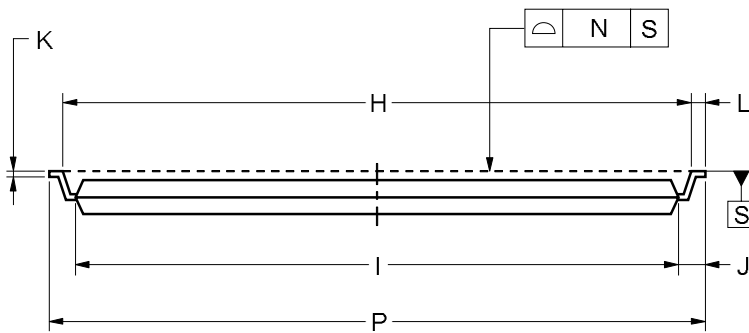
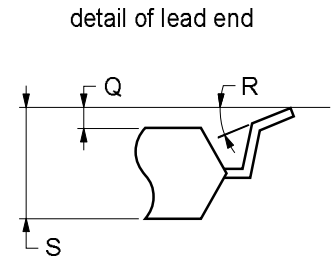
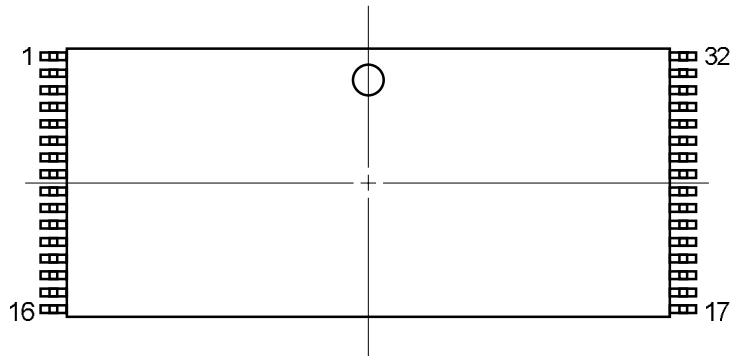
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.20±0.10
G	1.02 MAX.
H	19.0±0.2
I	18.4±0.2
J	0.8±0.2
K	0.125 <sup>+0.10</sup> <sub>-0.05</sub>
L	0.5±0.1
M	0.08
N	0.10
P	20.0±0.2
Q	0.05±0.05
R	5°±5°
S	1.1 MAX.

S32GZ-50-KJH-4

Low standoff height

★ 32-PIN PLASTIC TSOP (I) (8x20)



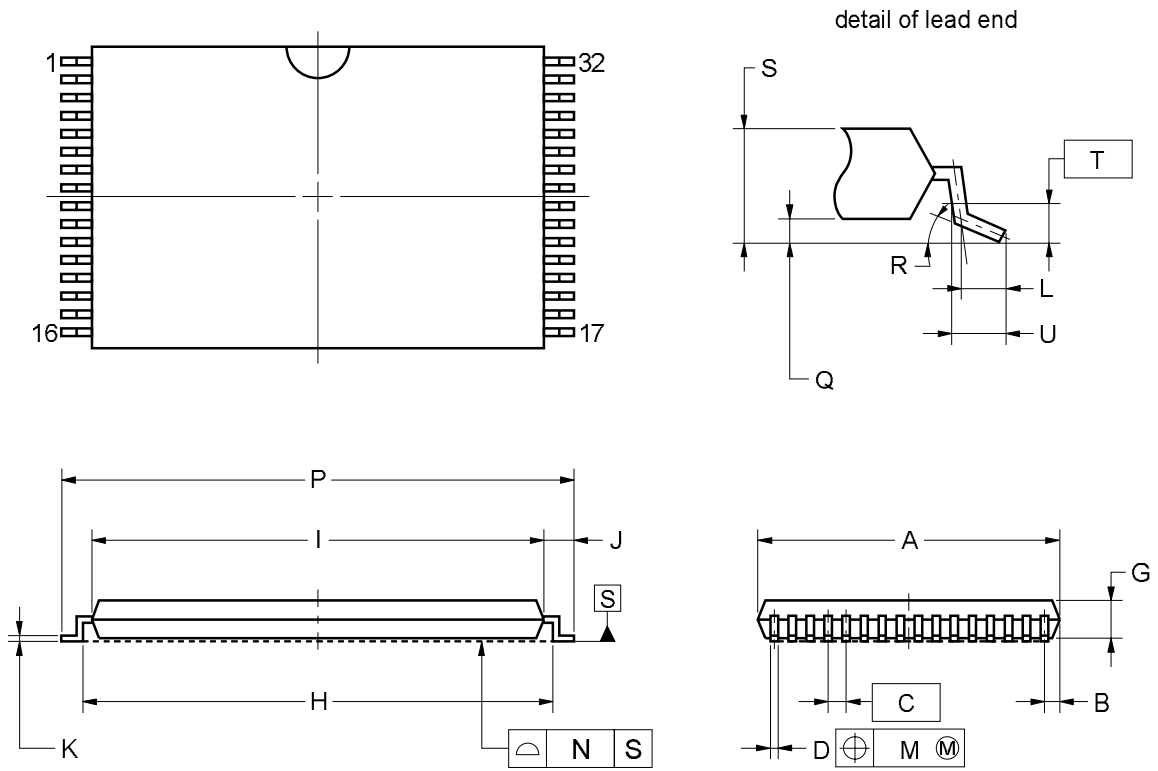
NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.20±0.10
G	1.02 MAX.
H	19.0±0.2
I	18.4±0.2
J	0.8±0.2
K	0.125 <sup>+0.10</sup> <sub>-0.05</sub>
L	0.5±0.1
M	0.08
N	0.10
P	20.0±0.2
Q	0.05±0.05
R	5°±5°
S	1.1 MAX.

S32GZ-50-KKH-4

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



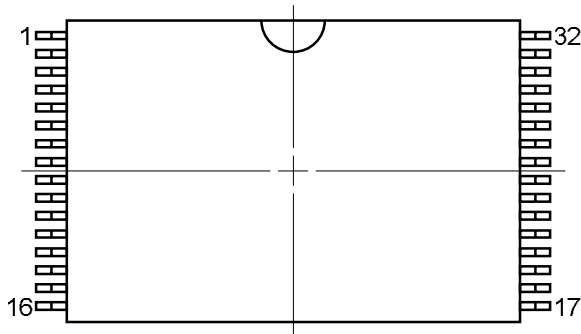
NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

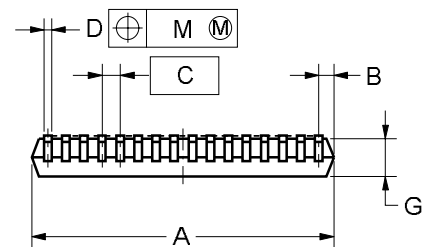
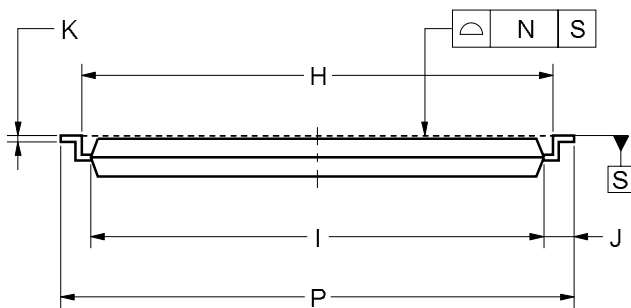
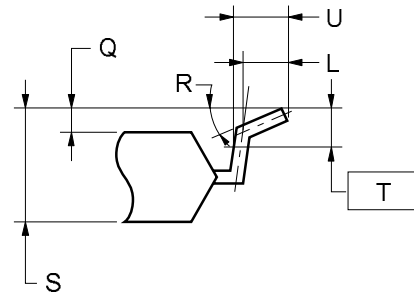
ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	3° <sup>+5°</sup> <sub>-3°</sub>
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9JH-2

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



detail of lead end



NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	3° <sup>+5°</sup> <sub>-3°</sub>
S	1.2 MAX.
T	0.25
U	0.6±0.15
P32GU-50-9KH-2	

**Recommended Soldering Conditions**

The following conditions must be met when soldering conditions of the μPD431000A.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

**Types of Surface Mount Device**

- μPD431000AGW-xxL: 32-pin Plastic SOP (13.34 mm (525))
- μPD431000AGW-xxLL: 32-pin Plastic SOP (13.34 mm (525))
- μPD431000AGW-Axx: 32-pin Plastic SOP (13.34 mm (525))
- μPD431000AGW-Bxx: 32-pin Plastic SOP (13.34 mm (525))
- μPD431000AGZ-xxLL-KJH: 32-pin Plastic TSOP (I) (8 × 20) (Normal bent)
- μPD431000AGZ-xxLL-KKH: 32-pin Plastic TSOP (I) (8 × 20) (Reverse bent)
- μPD431000AGZ-Bxx-KJH: 32-pin Plastic TSOP (I) (8 × 20) (Normal bent)
- μPD431000AGZ-Bxx-KKH: 32-pin Plastic TSOP (I) (8 × 20) (Reverse bent)
- μPD431000AGU-Bxx-9JH: 32-pin Plastic TSOP (I) (8 × 13.4) (Normal bent)
- μPD431000AGU-Bxx-9KH: 32-pin Plastic TSOP (I) (8 × 13.4) (Reverse bent)

Please consult with our sales offices.

**Types of Through Hole Mount Device**

- μPD431000ACZ-xxL: 32-pin Plastic DIP (600 mil)
- μPD431000ACZ-xxLL: 32-pin Plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature : 300 °C or below, Time: 3 seconds or below (Per one lead)

**Caution Do not jet molten solder on the surface of package.**

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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  - NEC devices are classified into the following three quality grades:  
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    - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
    - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
    - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
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