NEC

MOS INTEGRATED CIRCUIT

μPD431232AL

1M-BIT CMOS SYNCHRONOUS FAST SRAM
32K-WORD BY 32-BIT

Description

The μPD431232AL is a 32,768-word by 32-bit synchronous static RAM fabricated with advanced CMOS technology using N-channel memory cell.

The μPD431232AL integrates unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core.

All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD431232AL is suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as cache and buffer memory.

ZZ pin has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State ("Sleep"). In the "Sleep" state, the SRAM internal state is preserved. When ZZ pin is set LOW again, the SRAM resumes normal operation.

The μPD431232AL is packaged in 100-pin plastic TQFP with a 1.4 mm package thickness (LQFP in EIAJ) for high density and low capacitive loading.

Features

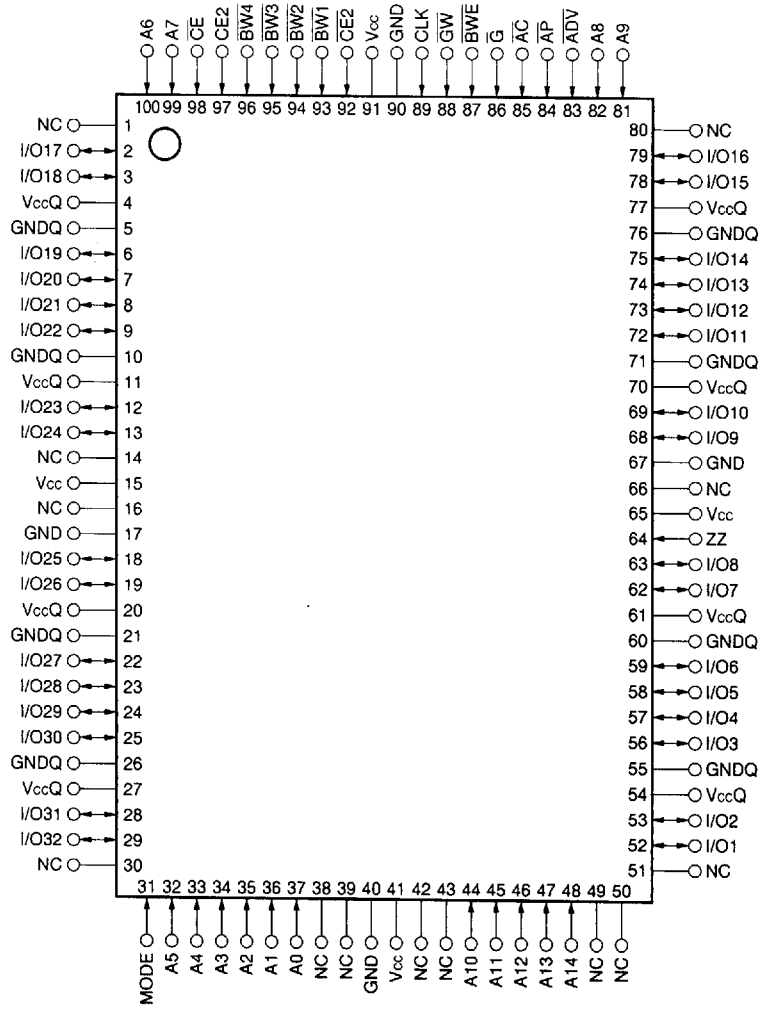
- Single 3.3 V power supply
- Synchronous operation
- Burst Read/Write: Interleaved burst and Linear burst sequence
- Fully registered inputs and outputs for Pipelined operation
- LVTTL compatible: All inputs and outputs
- Fast clock access time: 7ns/83 MHz, 8 ns/66 MHz, 10 ns/60 MHz, 12 ns/50 MHz
- Asynchronous output enable: $\overline{G}$
- Burst sequence selectable: MODE
- Power down (Sleep) mode: ZZ (ZZ = Open or Low: Normal operation)
- Separate byte write enable: $\overline{BW1}$-$\overline{BW4}$, $\overline{BWE}$ and global write enable: $\overline{GW}$
- Three chip enables for easy depth expansion
- Common I/O using three state outputs
- 5 V - tolerant inputs (except I/O pins)

Ordering Information

Part number	Access time ns (MAX.)	Clock frequency MHz	Burst sequence	Operation	Package
μPD431232ALGF-A7	7	83	Interleaved and linear	Pipelined operation	100-pin plastic TQFP (14 × 20 mm)
μPD431232ALGF-A8	8	66			
μPD431232ALGF-A10	10	60			
μPD431232ALGF-A12	12	50			

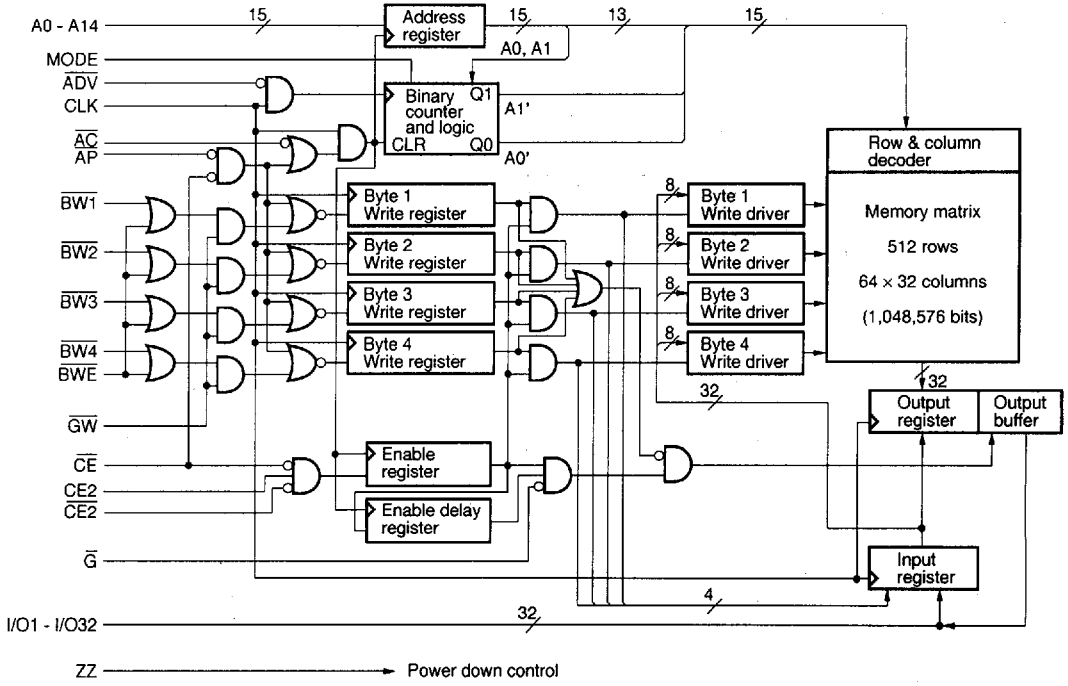
Pin Configuration (Marking Side)

100-pin plastic TQFP (14 × 20 mm)



A0 - A14	:	Address inputs	CLK	:	System clock input
I/O1 - I/O32	:	Data inputs/outputs	MODE	:	Burst sequence select input
$\overline{ADV}$	:	Burst address advance	ZZ	:	Power down state input
$\overline{AC}$	:	Controller address status	Vcc	:	Power supply (3.3 V)
$\overline{AP}$	:	Processor address status	GND	:	Ground
$\overline{CE}$, $\overline{CE2}$, CE2	:	Chip enable	VccQ	:	Power for outputs (3.3 V)
$\overline{BW1}$ - $\overline{BW4}$, $\overline{BWE}$	:	Byte write enable	GNDQ	:	Ground for outputs
$\overline{GW}$	:	Global write	NC	:	No connection
$\overline{G}$	:	Asynchronous output enable			

Block Diagram



Burst Sequence Table

Burst sequence is controlled by MODE input pin. MODE pin has to be tied to Vcc or GND during normal operation.

1. Interleaved burst sequence [MODE = Vcc]

External Address	A14 - A2, A1, A0
1st Burst Address	A14 - A2, A1, $\overline{A0}$
2nd Burst Address	A14 - A2, $\overline{A1}$, A0
3rd Burst Address	A14 - A2, $\overline{A1}$, $\overline{A0}$

Remark The burst sequence wraps around to its initial state upon completion.

2. Linear burst sequence [MODE = GND]

External Address	A14 - A2, 0, 0	A14 - A2, 0, 1	A14 - A2, 1, 0	A14 - A2, 1, 1
1st Burst Address	A14 - A2, 0, 1	A14 - A2, 1, 0	A14 - A2, 1, 1	A14 - A2, 0, 0
2nd Burst Address	A14 - A2, 1, 0	A14 - A2, 1, 1	A14 - A2, 0, 0	A14 - A2, 0, 1
3rd Burst Address	A14 - A2, 1, 1	A14 - A2, 0, 0	A14 - A2, 0, 1	A14 - A2, 1, 0

Remark The burst sequence wraps around to its initial state upon completion.

Asynchronous Truth Table

Operation	$\overline{G}$	I/O
Read Cycle	L	D_{OUT}
	H	Hi-Z
Write Cycle	×	Hi-Z, D_{IN}
Deselected	×	Hi-Z

Remark × means "Don't care".

Synchronous Truth Table

Operation	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{AP}$	$\overline{AC}$	$\overline{ADV}$	$\overline{WRITE}$ Note 2	CLK	Address
Deselected Note 1	H	×	×	×	L	×	×	L-H	N/A
Deselected Note 1	L	×	L	L	×	×	×	L-H	N/A
Deselected Note 1	L	H	×	L	×	×	×	L-H	N/A
Deselected Note 1	L	×	L	H	L	×	×	L-H	N/A
Deselected Note 1	L	H	×	H	L	×	×	L-H	N/A
Read cycle/Begin burst	L	L	H	L	×	×	×	L-H	External
Read cycle/Begin burst	L	L	H	H	L	×	H	L-H	External
Read cycle/Continue burst	×	×	×	H	H	L	H	L-H	Next
Read cycle/Continue burst	H	×	×	×	H	L	H	L-H	Next
Read cycle/Suspend burst	×	×	×	H	H	H	H	L-H	Current
Read cycle/Suspend burst	H	×	×	×	H	H	H	L-H	Current
Write cycle/Begin burst	L	L	H	H	L	×	L	L-H	External
Write cycle/Continue burst	×	×	×	H	H	L	L	L-H	Next
Write cycle/Continue burst	H	×	×	×	H	L	L	L-H	Next
Write cycle/Suspend burst	×	×	×	H	H	H	L	L-H	Current
Write cycle/Suspend burst	H	×	×	×	H	H	L	L-H	Current

Notes 1. Deselected status is held until new "Begin Burst" entry.

2. $\overline{WRITE}$ = L means any one or more byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, or $\overline{BW4}$) and $\overline{BWE}$ are low or $\overline{GW}$ is low.

$\overline{WRITE}$ = H means all byte write enables are high.

Remark × means "Don't care".

Partial Truth Table for Write Enables

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read cycle	H	H	×	×	×	×
	H	L	H	H	H	H
Write cycle/Byte1 only	H	L	L	H	H	H
Write cycle/All bytes	H	L	L	L	L	L
	L	×	×	×	×	×

Note × means "Don't care".

Pass-through Truth Table

Previous cycle				Present cycle						Next cycle
Operation	Address	$\overline{\text{WRITE}}$ Note1	I/O	Operation	Address	$\overline{\text{CEs}}$ Note2	$\overline{\text{WRITE}}$ Note1	$\overline{\text{G}}$	I/O	Operation
Write cycle	Ak	L	Dn(Ak)	Read cycle (Begin burst)	Am	L	H	L	Q1(Ak)	Read Q1 (Am)
				Deselected	–	H	×	×	Hi-Z	No carryover from previous cycle

Notes 1. $\overline{\text{WRITE}}$ = L means any one or more byte write enables ($\overline{\text{BW1}}$, $\overline{\text{BW2}}$, $\overline{\text{BW3}}$, or $\overline{\text{BW4}}$) and $\overline{\text{BWE}}$ are low or $\overline{\text{GW}}$ is low.

$\overline{\text{WRITE}}$ = H means all byte write enables are high.

2. $\overline{\text{CEs}}$ = L means $\overline{\text{CE}}$ is low, $\overline{\text{CE2}}$ is low and CE2 is high.

$\overline{\text{CEs}}$ = H means $\overline{\text{CE}}$ is high or $\overline{\text{CE2}}$ is high or CE2 is low.

Remark × means "Don't care".

ZZ (Sleep) Truth Table

ZZ	Chip status
≤ 0.2 V	Active
Open	Active
≥ V_{CC} −0.2 V	Sleep

Electrical Characteristics

- The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the tables.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +4.6	V
Output supply voltage	V_{CCQ}	−0.5 to V_{CC}	V
Input voltage	V_{IN}	−0.5[Note] to +6.0	V
Input/Output voltage	$V_{I/O}$	−0.5[Note] to V_{CCQ} + 0.5	V
Operating ambient temperature	T_A	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note −2.5 V (MIN.) (Pulse width: 3 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	3.1	3.3	3.6	V
Output supply voltage	V_{CCQ}	3.1	3.3	3.6	V
High level input voltage-Input pins	$V_{IH(IN)}$	2.0		5.5	V
High level input voltage-I/O pins	$V_{IH(I/O)}$	2.0		V_{CCQ} + 0.3	V
Low level input voltage	V_{IL}	−0.5[Note]		+0.8	V
Operating ambient temperature	T_A	0		+70	°C

Note −2.5 V (MIN.) (Pulse width: 3 ns)

Capacitance (T_A = +25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			4	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			7	pF
Clock input capacitance	C_{clk}	V_{clk} = 0 V			4	pF

Remarks 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

DC Characteristics (Recommended operating conditions unless otherwise noted)

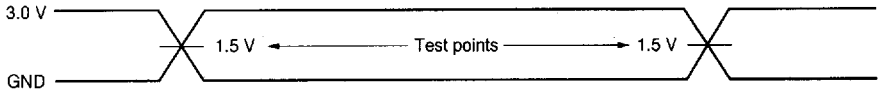
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} (except ZZ and MODE) = 0 V to V_{CC}, ZZ, MODE = 0 V or V_{CC}	−2		+2	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, Output is disabled	−2		+2	μA
Operating supply current	I_{CC}	Device selected, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA, Freq. = MAX.			250	mA
	I_{CC1}	Suspend read cycle, $\overline{AC}$, $\overline{AP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BWs} \geq V_{IH}$, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA, Freq. = MAX.			45	
Standby supply current	I_{SB}	Device deselected, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, Cycle = 0 MHz, All inputs are static			20	mA
	I_{SB1}	Device deselected, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V, Cycle = 0 MHz, All inputs are static			2	
	I_{SB2}	Device deselected, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, Freq. = MAX.			50	
Power down supply current	I_{SBZZ}	ZZ ≥ V_{CC} − 0.2 V		0.2	1	mA
High level output voltage	V_{OH}	I_{OH} = −4 mA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 8 mA			0.4	V

Remark V_{IN}: Input voltage

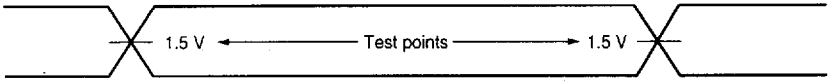
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/fall time ≤ 3 ns)



Output waveform



Output load

Fig. 1

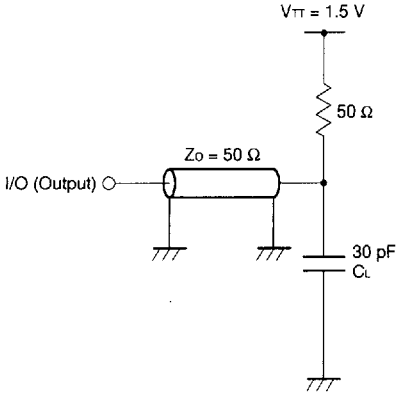
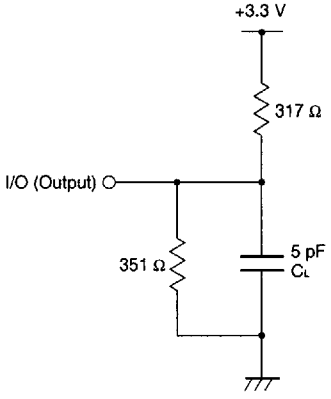


Fig. 2
(For TDC1, TDC2, TOLZ, TOHZ, TCZ)



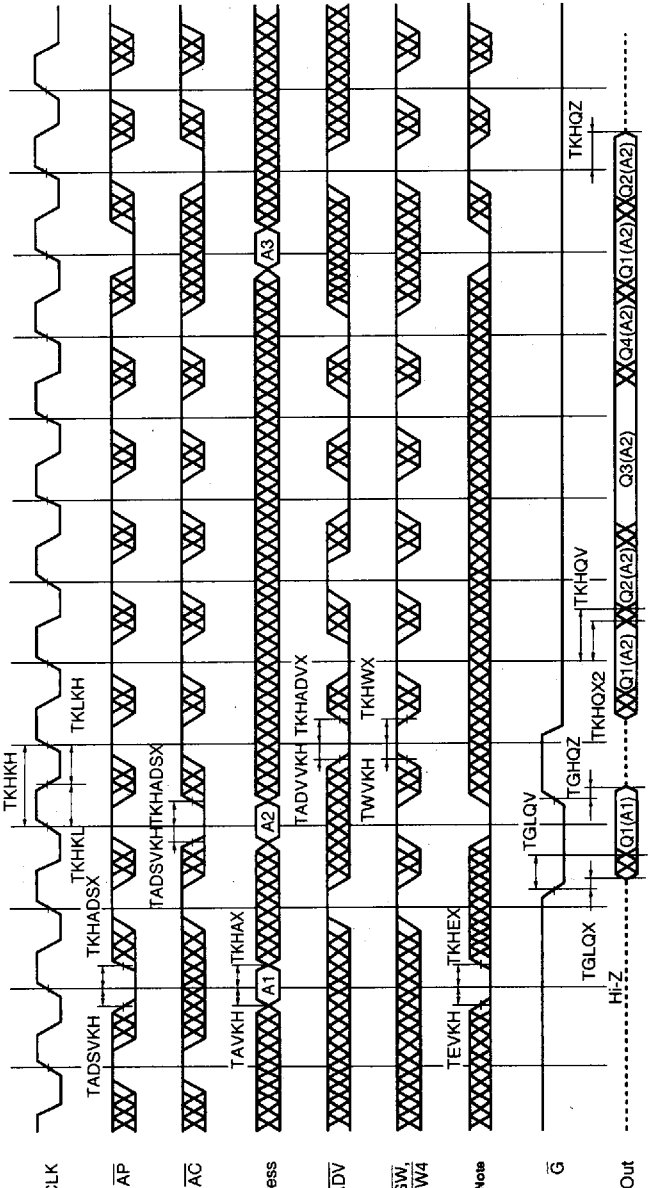
Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

Parameter		Symbol		-A7 (83 MHz)		-A8 (66 MHz)		-A10 (60 MHz)		-A12 (50 MHz)		Unit	Note
		Standard	Alternate	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Cycle time		TKHKH	TCYC	12	–	15	–	16.7	–	20	–	ns	
Clock access time		TKHQV	TCD	–	7	–	8	–	10	–	12	ns	
Output Enable to output valid		TGLQV	TOE	–	5	–	5	–	5	–	6	ns	
Clock high to output active		TKHQX1	TDC1	2	–	2	–	2	–	2	–	ns	
Clock high to output change		TKHQX2	TDC2	3	–	3	–	3	–	3	–	ns	
Output Enable to output active		TGLQX	TOLZ	2	–	2	–	2	–	2	–	ns	
Output disable to output Hi-Z		TGHQZ	TOHZ	2	5	2	5	2	5	2	6	ns	
Clock high to output Hi-Z		TKHQZ	TCZ	2	5	2	5	2	5	2	6	ns	
Clock high pulse width		TKHKL	TCH	4.5	–	5	–	5	–	6	–	ns	
Clock low pulse width		TKLKH	TCL	4.5	–	5	–	5	–	6	–	ns	
Setup times	Address	TAVKH	TAS	2.5	–	2.5	–	3	–	3	–	ns	
	Address status	TADSVKH	TSS										
	Data In	TDVKH	TDS										
	Write Enable	TWVKH	TWS										
	Address advance	TADVVKH	–										
	Chip Enable	TEVKH	–										
Hold times	Address	TKHAX	TAH	0.5	–	0.5	–	0.5	–	0.5	–	ns	
	Address status	TKHADSX	TSH										
	Data In	TKHDX	TDH										
	Write Enable	TKHWX	TWH										
	Address advance	TKHADVX	–										
	Chip Enable	TKHEX	–										
Power down entry setup		TZZES	TZZES	8	–	8	–	8	–	8	–	ns	1
Power down entry hold		TZZEH	TZZEH	0	–	0	–	0	–	0	–	ns	1
Power down recovery setup		TZZRS	TZZRS	8	–	8	–	8	–	8	–	ns	1
Power down recovery hold		TZZRH	TZZRH	0	–	0	–	0	–	0	–	ns	1

Note 1. Although ZZ signal input is asynchronous, the signal must meet specified setup and hold times in order to be recognized.

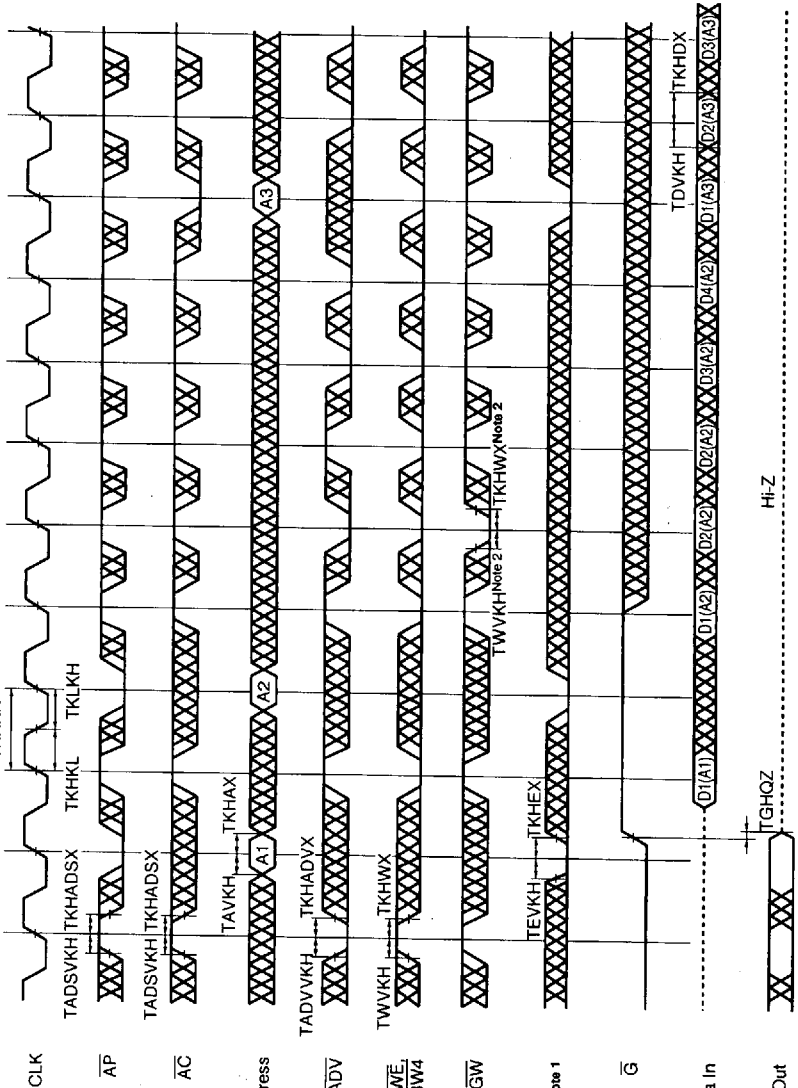
Read Cycle



Note $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

Remark Qn(A2) refers to output from address A2. Q1 - Q4 refers to outputs according to burst sequence.

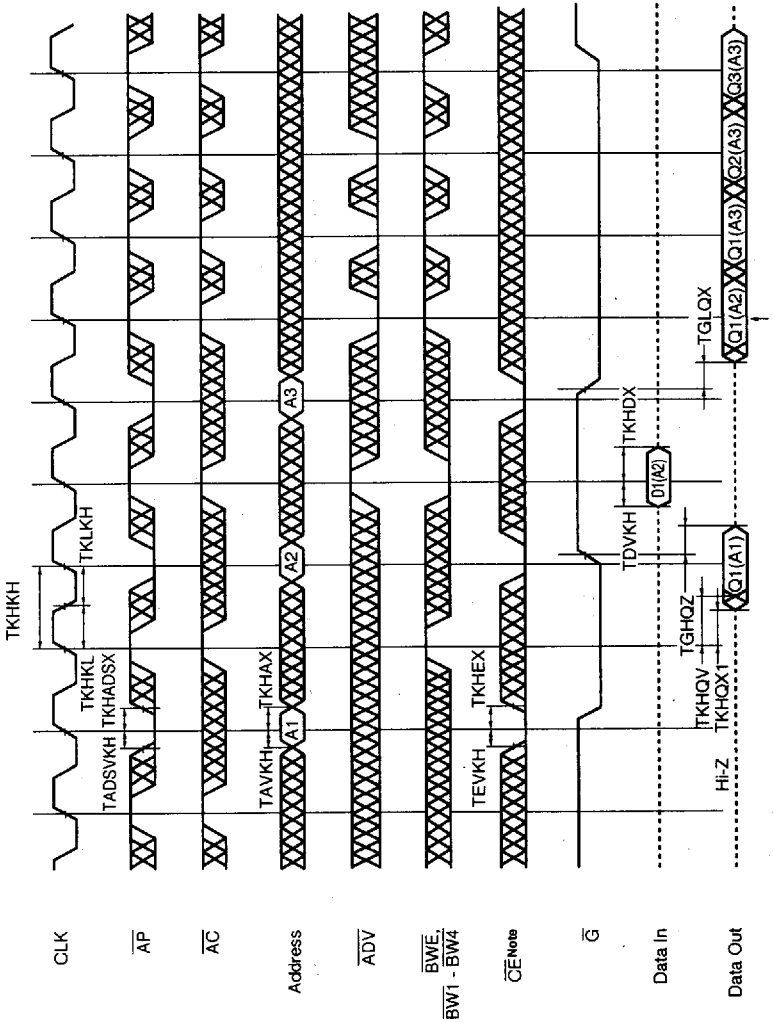
Write Cycle



Notes 1. $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

2. All bytes WRITE can be initiated by $\overline{GW}$ low or $\overline{GW}$ high and $\overline{BWE}$, $\overline{BW1}$-$\overline{BW4}$ low.

Read/Write Cycle

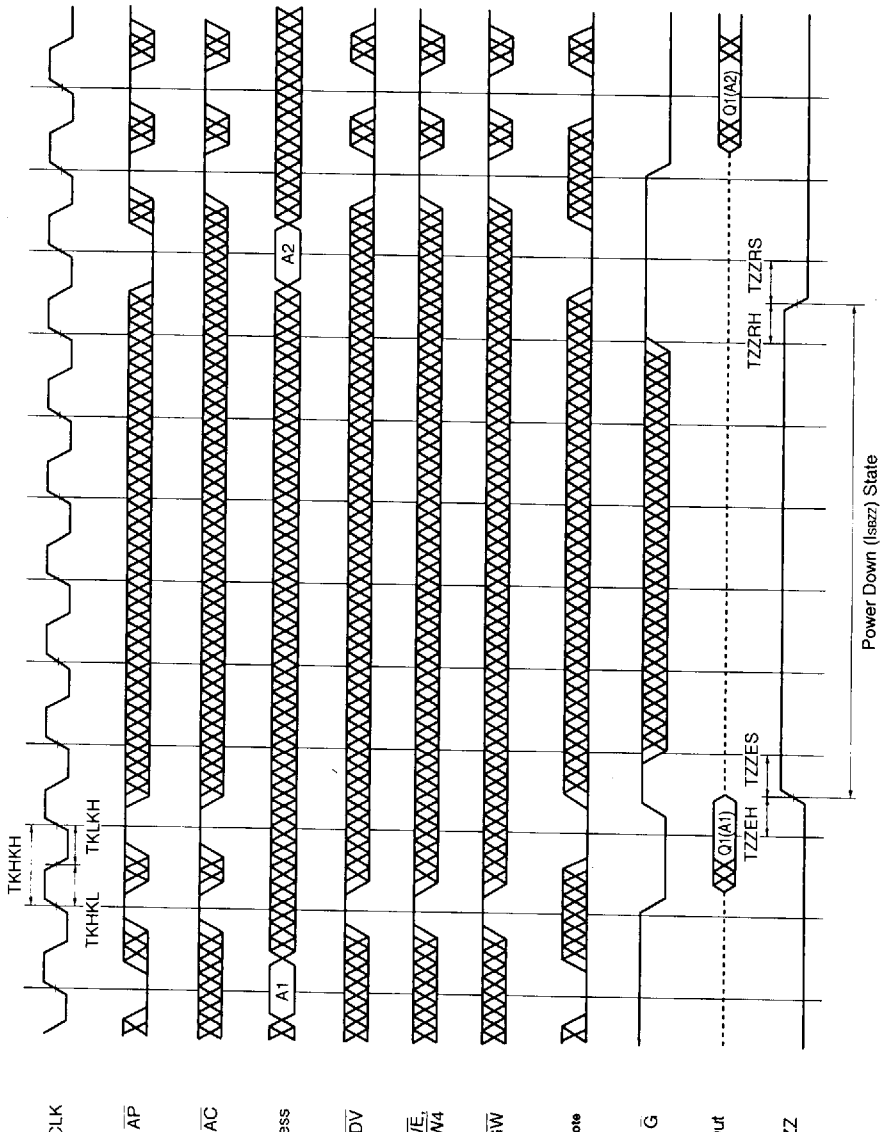


Note $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

Remarks 1. $\overline{GW}$ is high.

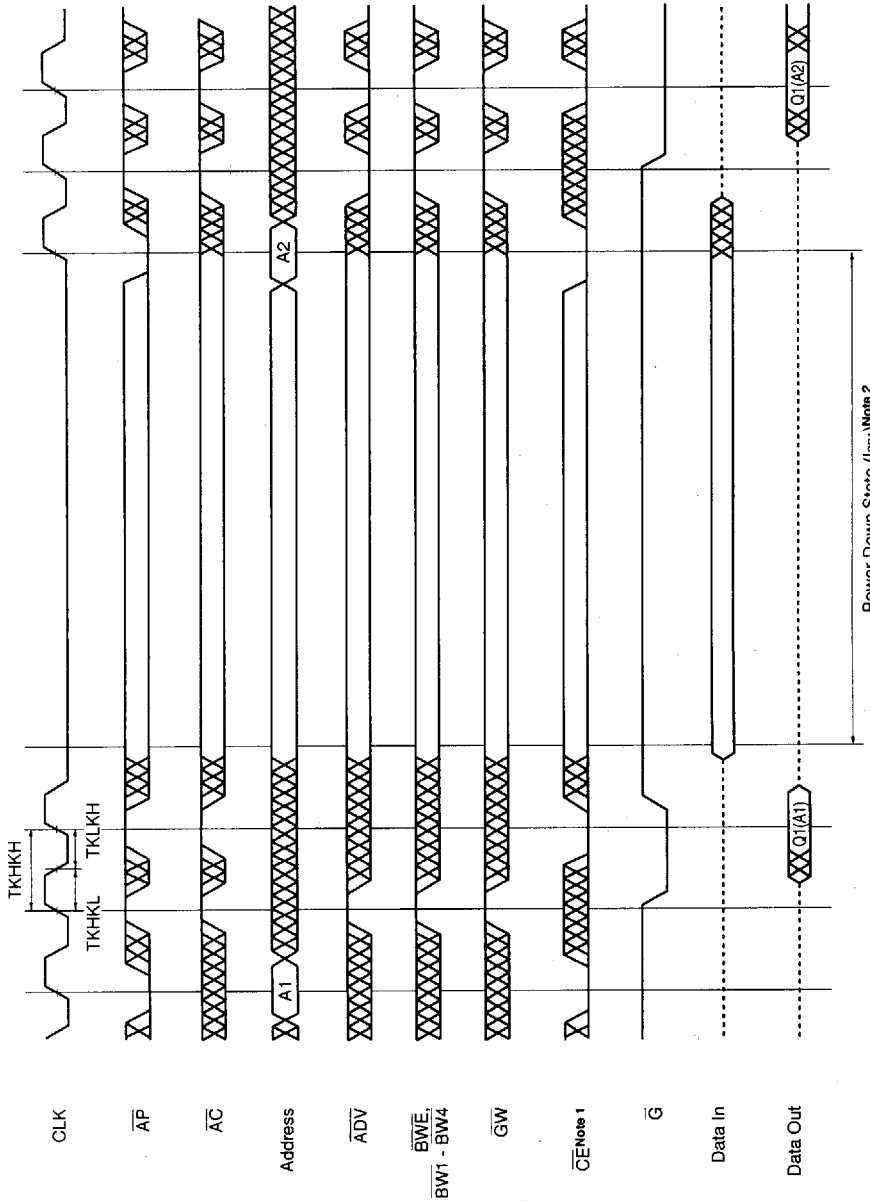
2. The data out remains in Hi-Z following a WRITE cycle unless an $\overline{AP}$, $\overline{AC}$ or $\overline{ADV}$ cycle is performed.

Power Down (ZZ) Cycle



Note $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

Stop Clock Cycle

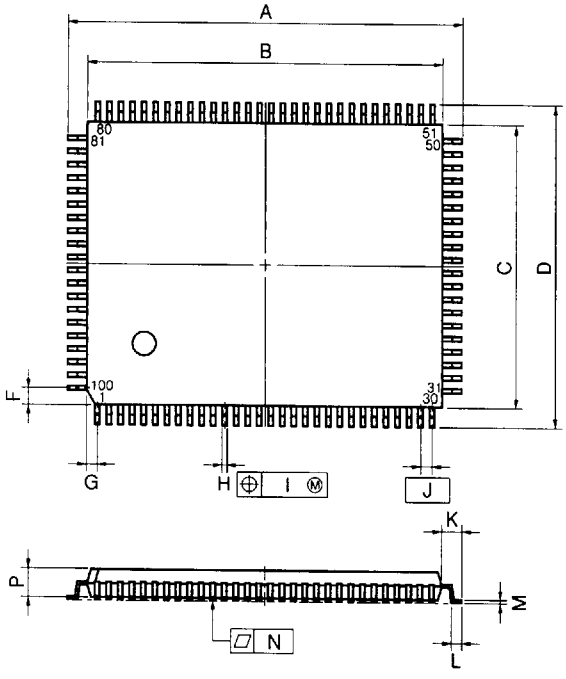


Notes 1. $\overline{CE2}$ and CE2 have the same timing as $\overline{CE}$. In this timing, when $\overline{CE}$ is low, $\overline{CE2}$ is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

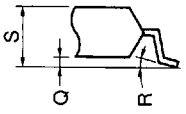
2. $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V (V_{IN}: Input voltage)

Package Drawing

100 PIN PLASTIC LQFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	0.825	0.032
G	0.575	0.023
H	$0.32^{+0.08}_{-0.07}$	0.013±0.003
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.06}_{-0.05}$	0.007±0.002
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S100GF-65-8ET

Remark TQFPs with a 1.4 mm package thickness are called LQFP in EIAJ.

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of μPD431232AL.

Type of Surface Mount Device

μPD431232ALGF: 100-pin plastic TQFP (14 × 20 mm)