DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD43256A (F)

256K-BIT CMOS STATIC RAM

DESCRIPTION

The μPD43256A is a high speed, low power, 32K words by 8 bits CMOS static RAM fabricated with advanced silicon-gate CMOS tecnology. The μPD43256A is low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuitry technique makes the device a high speed and low operating power device which requires no clock or refreshing to operate.

Minimum standby power is drawn by this device when $\overline{CS}$ is at high level, independently of the other inputs level.

Data retention is guaranteed at a power supply voltage as low 2 volts.

The μPD43256A(F) is Extended-Temperature-Version(Ta=-40 to +85).

The μPD43256A(F) is packed in 28-pin DIP, 28-pin SOP .

FEATURES

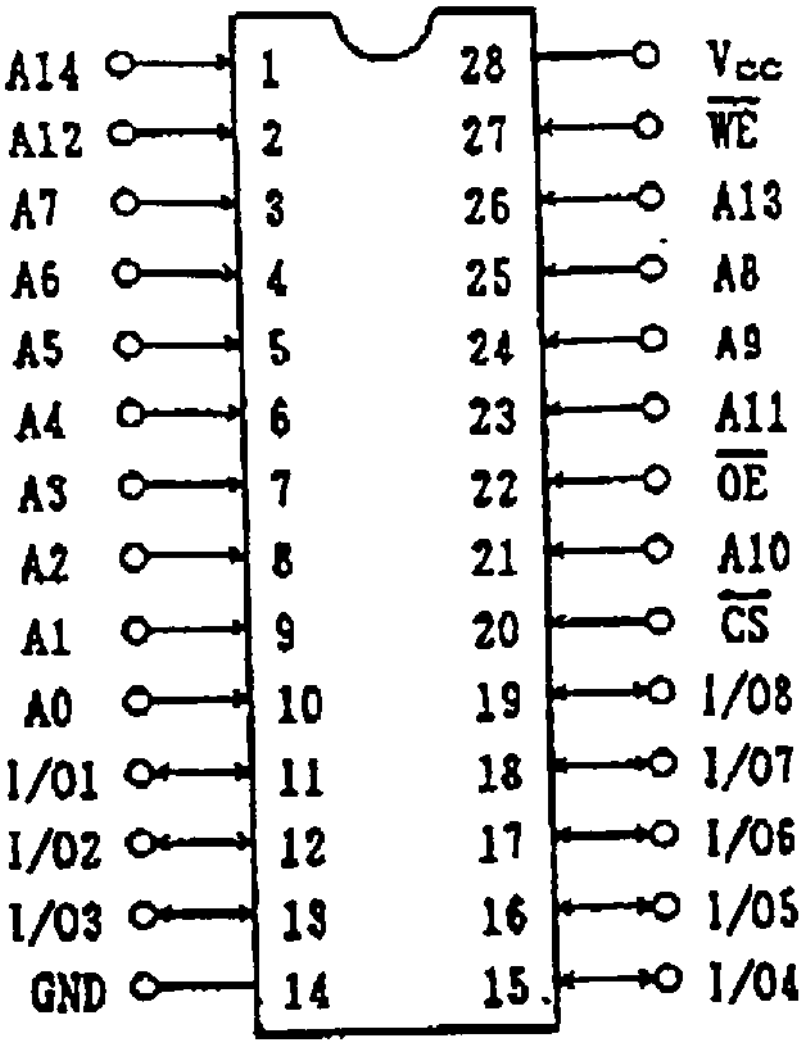
- 32786 words by 8 bits organization
- Fast Access Time
  - μPD43256A(F)-10/10L····100 ns MAX.
  - μPD43256A(F)-12/12L····120 ns MAX.
  - μPD43256A(F)-15/15L····150 ns MAX.
- Low Power Dissipation (L-Version)
  - Standby Supply Current·····L-Version :200μA MAX.
  - Data Retention Supply Current···L-Version···15μA MAX.(Ta=0 to 40°C)
- Extended Temperature Range:Ta=-40 to 85°C
- Single +5V Supply
- Fully Static Operation:No clock or Refreshing required
- TTL Compatible:All Inputs and Outputs
- Common I/O Using Three-State Output
- One Chip Select and One Output Enable Inputs for Easy Application

ORDERING INFORMATION

PART NUMBER	PACKAGE	ACCESS TIME(MAX.)	NOTE
μPD43256AC(F)-10	28-pin Plastic DIP(600mil)	100ns	
μPD43256AC(F)-12	〃	120ns	
μPD43256AC(F)-15	〃	150ns	
μPD43256AC(F)-10L	〃	100ns	L-Version
μPD43256AC(F)-12L	〃	120ns	〃
μPD43256AC(F)-15L	〃	150ns	〃
μPD43256AGU(F)-10L	28-pin Plastic SOP	100ns	L-Version
μPD43256AGU(F)-12L	〃	120ns	〃
μPD43256AGU(F)-15L	〃	150ns	〃

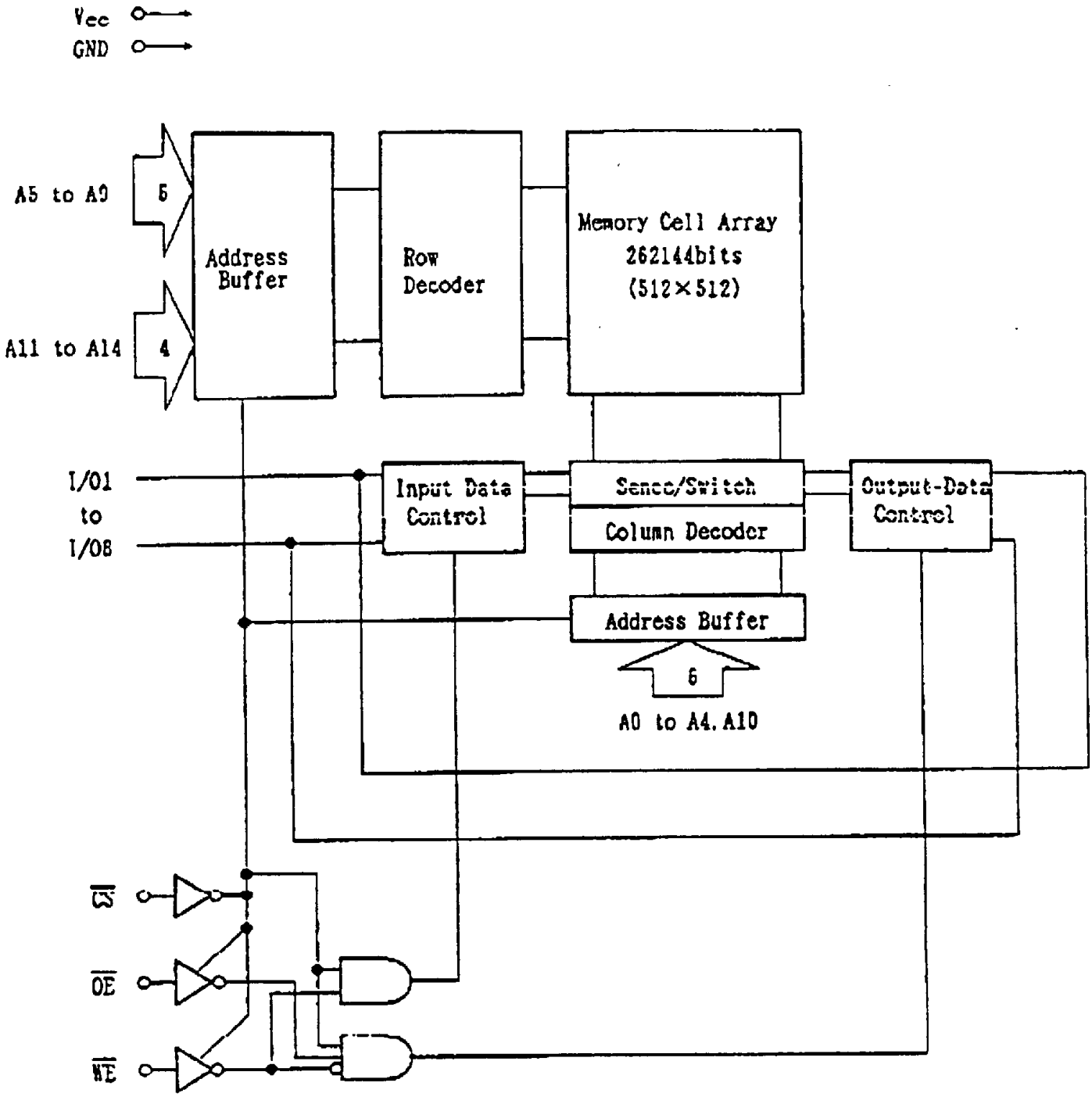
PIN CONFIGURATION

28-pin Plastic DIP/SOP
(TOP VIEW)



A0 to A14	: Address input
I/O1 to I/O8	: Data input/Output
$\overline{CS}$	: Chip Select Input
$\overline{WE}$	: Write Enable Input
$\overline{OE}$	: Output Enable Input
Vcc	: Power Supply (+5 V)
GND	: Ground
NC	: No Connection

BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	Icc
H	×	×	Not Selected	Hi-Z	I_{SB}
L	H	H	Output Disable		I_{CCA}
L	L	H	Read	D_{OUT}	
L	×	L	Write	D_{IN}	

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Supply Voltage	V_{CC}		−0.5 Note1 to +7.0	V
Input/Output Voltage	V_T		−0.5 Note1 to V_{CC}+0.5	V
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Note: −3.0V MIN. (Pulse Width 50ns)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage Vcc	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.4		V_{CC}+0.5	V
Input Low Voltage	V_{IL}		−0.3 Note		0.6	V
Ambient Temperature	Ta		−40		85	°C

Note: −3.0V MIN. (Pulse Width 50ns)

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		μPD43256A(F) MIN.	TYP.	MAX.	μPD43256A(F)-L MIN.	TYP.	MAX.	UNIT
Input Leakage Current	I_{LI}	V_{IN}=0 V to V_{CC}		−1.0		1.0	−1.0		1.0	μA
I/O Leakage Current	I_{LO}	$V_{I/O}$=0 V to V_{CC} $\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}		−1.0		1.0	−1.0		1.0	μA
Operating Supply Current	I_{CCA1}	$\overline{CS}$=V_{IL} MIN. Cycle $I_{I/O}$=0 mA	μPD43256A(F)-10			60			40	mA
			μPD43256A(F)-12			40			40	mA
			μPD43256A(F)-15			35			35	mA
	I_{CCA2}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA				15			15	mA
	I_{CCA3}	$\overline{CS}$≦0.2V, Cycle=1Mhz, $I_{I/O}$=0 mA V_{IL}≦0.2V, V_{IN}≧V_{CC}−0.2V				15			15	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}				5			3	mA
	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2 V			0.02	2		0.002	0.2	mA
Output High Voltage	V_{OH1}	I_{OH}=−1.0 mA		2.4			2.4			V
	V_{OH2}	I_{OH}=−0.1 mA		V_{CC}−0.5			V_{CC}−0.5			V
Output Low Voltage	V_{OL}	I_{OL}=2.1 mA				0.4			0.4	V

CAPACITANCE (Ta=25 ℃, f=1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	単位
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0 V			8	pF
Input Capacitance	C_{IN}	V_{IN}=0 V			5	pF

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

AC TEST CONDITIONS

- Input Pulse Levels : 0.6 ~ 2.4 V
- Input Pulse Rise and Fall Time : 5 ns
- Timing Reference Levels : 1.5 V
- Output Load : See Fig. 1, 2.

Fig. 1

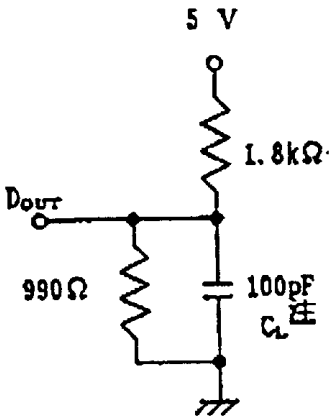
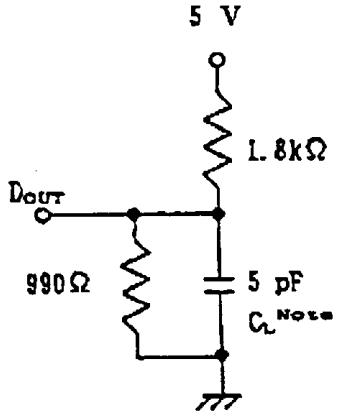


Fig. 2

(t_{CHZ}, t_{OHZ}, t_{CLZ}, t_{OLZ}, t_{WHZ}, t_{OW})

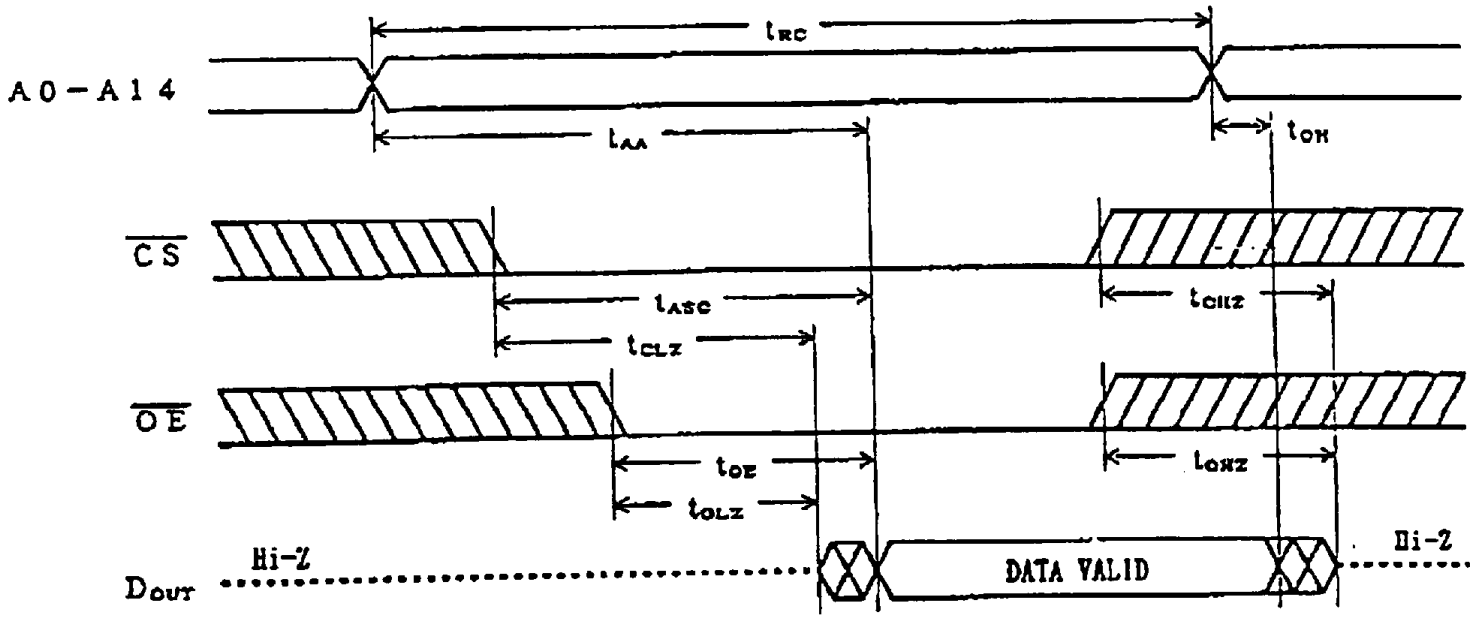


Note: including scope and jig.

READ CYCLE

PARAMETER	SYMBOL	μPD43256A(F)-10		μPD43256A(F)-12		μPD43256A(F)-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
Chip Select Access Time	t_{ACE}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		50		60		70	ns
Output Hold from Addess Change	t_{OH}	10		10		10		ns
Chip Select to Output in Lo-z	t_{CLZ}	10		10		10		ns
Output Enable to Output in Lo-z	t_{OLZ}	5		5		5		ns
Chip Select to Output in Hi-z	t_{CHZ}		35		40		50	ns
Output Enable to Output in Hi-z	t_{OHZ}		35		40		50	ns

READ CYCLE TIMING CHART NOTE1



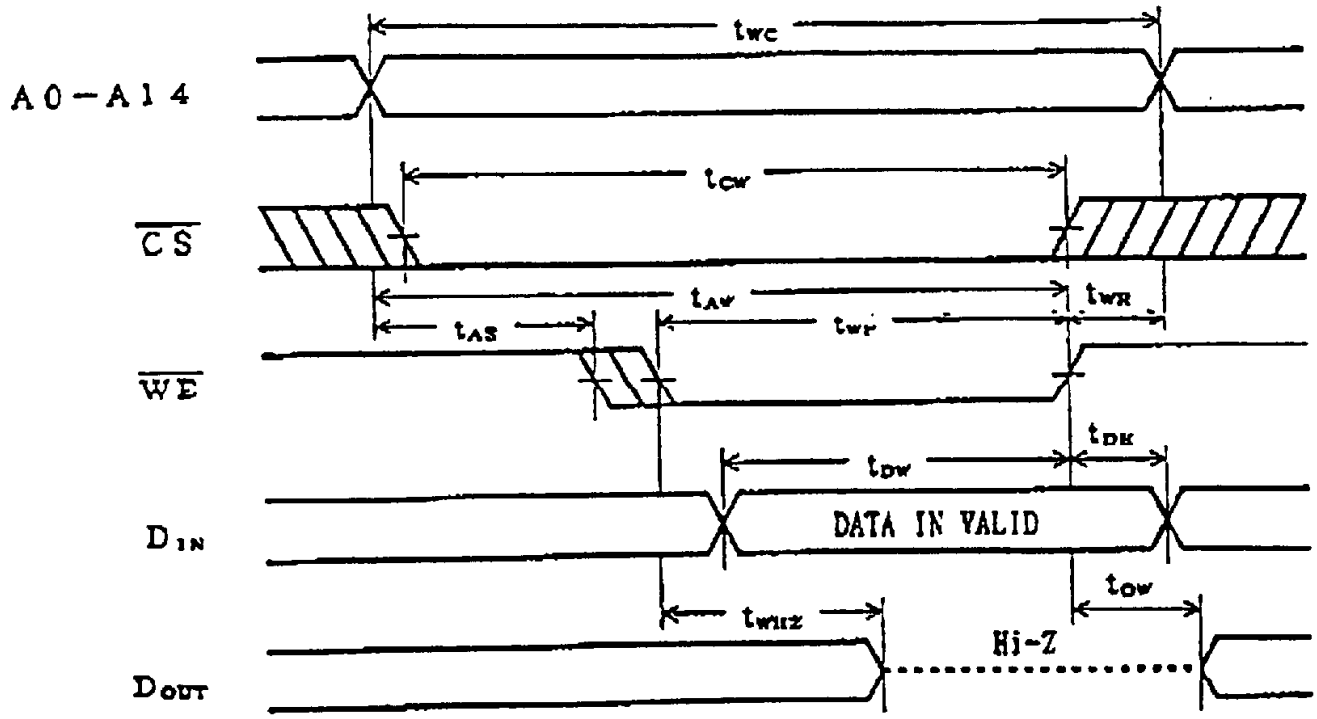
Note 1 : $\overline{WE}$ is high for read cycle.

WRITE CYCLE

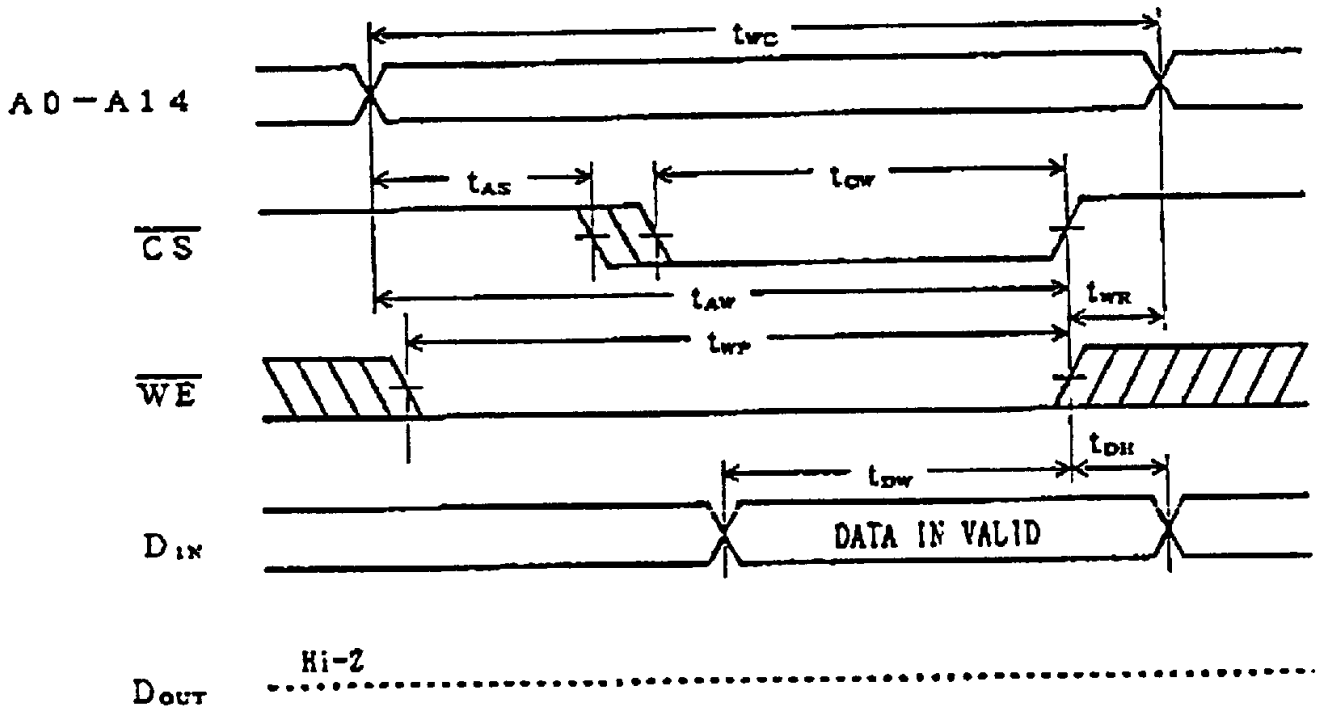
PARAMETER	SYMBOL	μPD43256A(F)-10		μPD43256A(F)-12		μPD43256A(F)-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	twc	100		120		150		n s
Chip Select to end of Write	tcw	80		85		100		n s
Address Valid to end of Write	taw	80		85		100		n s
Address Setup Time	tas	0		0		0		n s
Write Pulse Width	twp	70		70		90		n s
Write Recovery Time	twr	10		10		10		n s
Data Valid to end of Write	tow	40		50		60		n s
Data Hold Time	tDH	0		0		0		n s
Write Enable to Output in Hi-z	twhz		35		40		50	n s
Output Active from end of Write	tow	10		10		10		n s

WRITE CYCLE TIMING CHART

WRITE CYCLE ($\overline{WE}$ CONTROLLED) NOTE 1.2.3



WRITE CYCLE ($\overline{CS}$ CONTROLLED) NOTE 1.2



NOTE1: A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

2: $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

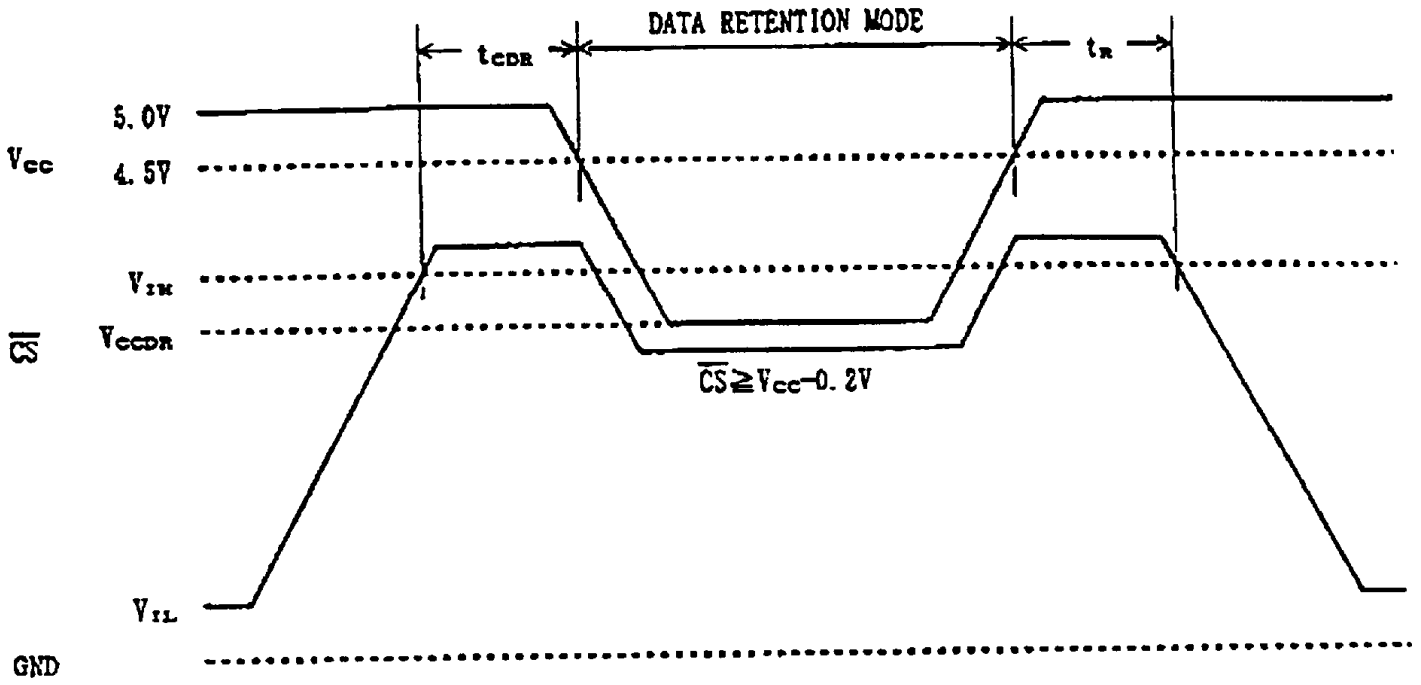
3: If $\overline{OE}$ is high, I/O pins remain in a high impedance state.

LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=-40 to 85°C) L-Version

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{CCDR}	$\overline{CS} \geqq V_{CC}$ 0.2V	2.0		5.5	V
Data Retention Supply Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS} \geqq V_{CC}$-0.2V		1	100 Note	μA
Chip Deselection to Data Retention Mode	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

Note Ta=0 to 40°C : 15μA MAX.

DATA RETENTION TIMING CHART Note 1



Note: The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.