DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD432836AL

2M-BIT CMOS SYNCHRONOUS FAST SRAM
64K-WORD BY 36-BIT
PIPELINED OPERATION

Description

The μPD432836AL is a 65,536-word by 36-bit synchronous static RAM fabricated with advanced CMOS technology using N-channel four-transistor memory cell.

The μPD432836AL integrates unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD432836AL is suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as cache and buffer memory.

The μPD432836ALGF is packaged in 100-pin plastic LQFP for high density and low capacitive loading.

Features

- Synchronous operation
- Internally self-timed write control
- Burst read / write : Interleaved burst sequence
- Fully registered inputs and outputs for 4-1-1-1 pipelined burst operation
- All registers triggered off positive clock edge
- Three chip enables for easy depth expansion
- Common I/O using three state outputs
- Internally controlled output enable
- Internally controlled burst advance
- Dout strobe controlled by SCLK

	Part number	Class	Clock frequency MHz	Clock access time ns	Maximum supply current		Supply voltage	
					Active mA	Standby mA	Chip V	I/O V
★	μPD432836AL	A33	300	3.23	350	3.5	3.3 ± 0.2	2.0 ± 0.2
		A36	275	3.53	350			
		A40	250	3.9	350			
		A44	225	4.34	350			
		A50	200	4.9	350			

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Printed in Japan

The mark ★ shows major revised points.

Ordering Information

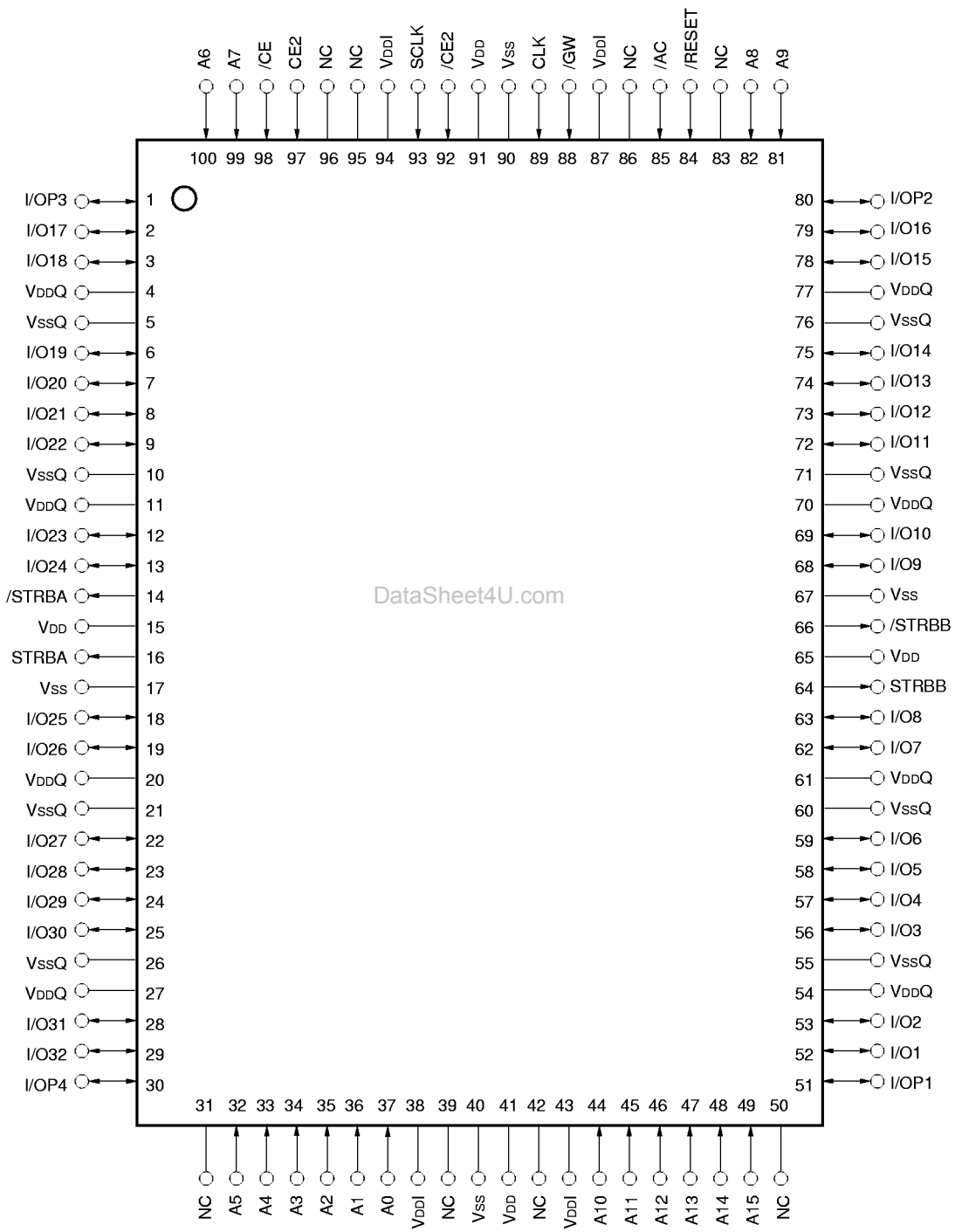
	Part number	Clock frequency MHz	Clock access time ns	Package
★	μPD432836ALGF-A33	300	3.23	100-pin plastic LQFP (14 × 20 mm)
	μPD432836ALGF-A36	275	3.53	
	μPD432836ALGF-A40	250	3.9	
	μPD432836ALGF-A44	225	4.34	
	μPD432836ALGF-A50	200	4.9	

Pin Configuration (Marking Side)

/xxx indicates active low signal.

100-pin plastic LQFP (14 x 20 mm)

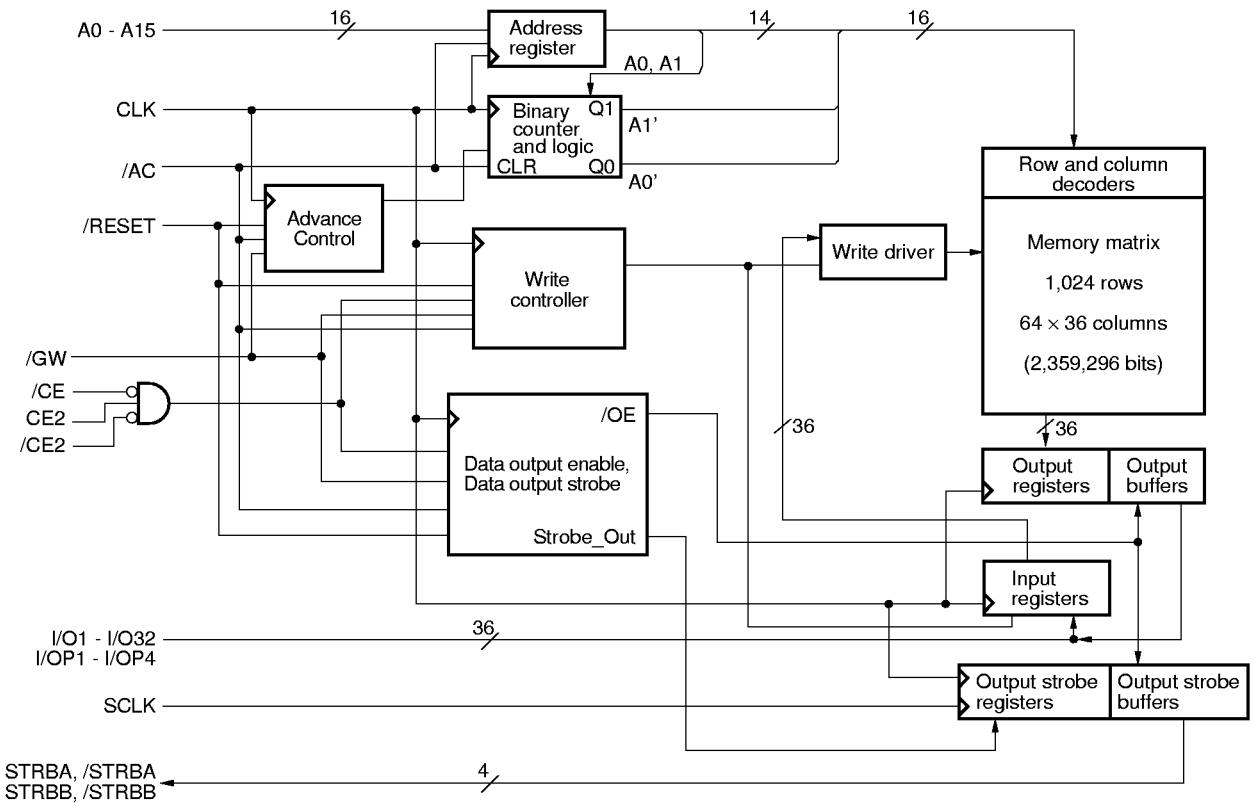
[μPD432836ALGF]



Pin Identification

Symbol	Pin number	Description
A0 - A15	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49	Synchronous Address Input
I/O1 - I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous Data Out
I/OP1 - I/OP4	51, 80, 1, 30	Synchronous Data In (Parity), Synchronous Data Out (Parity)
STRBA, /STRBA, STRBB, /STRBB	16, 14, 64, 66	Synchronous (SCLK) Data Out Strobe Output
/AC	85	Synchronous Address Status Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/GW	88	Synchronous Global Write Input
CLK	89	Clock Input
SCLK	93	Data Out Strobe Clock Input
/RESET	84	Asynchronous Input Initialize internal state at power up
V_{DD}	15, 41, 65, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply Apply same voltage level as $V_{DD}I$
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
$V_{DD}I$	38, 43, 87, 94	Input Buffer Power Supply Apply same voltage level as $V_{DD}Q$
NC	31, 39, 42, 50, 83, 86, 95, 96	No Connection

Block Diagram



Burst Sequence

Interleaved Burst Sequence Table

External Address	A15 - A2, A1, A0
1st Burst Address	A15 - A2, A1, /A0
2nd Burst Address	A15 - A2, /A1, A0
3rd Burst Address	A15 - A2, /A1, /A0

Synchronous Truth Table

Operation	/CE	CE2	/CE2	/AC	/GW	I/O	Address
Deselected [Note]	H	×	×	L	×	Hi-Z	None
Deselected [Note]	L	L	×	L	×	Hi-Z	None
Deselected [Note]	L	×	H	L	×	Hi-Z	None
Read Cycle / Begin Burst	L	H	L	L	H	Hi-Z	External
Read Cycle / Continue Burst	×	×	×	H	×	Hi-Z	Current
Read Cycle / Continue Burst	×	×	×	H	×	Hi-Z	Current
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	Next
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	Next
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	Next
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	None
Write Cycle / Begin Burst	L	H	L	L	L	Hi-Z	External
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Next
Write Cycle / Continue Burst	×	×	×	H	×	Data-in	Next
Write Cycle / Continue Burst	×	×	×	H	×	Hi-Z	Next
Write Cycle / Begin Burst	L	H	L	L	L	Hi-Z	External
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	H	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	H	Hi-Z	Next
Write Cycle / Masked	×	×	×	H	H	Hi-Z	N/A
Write Cycle / Masked	×	×	×	H	H	Hi-Z	N/A
Write Cycle / Begin Burst	L	H	L	L	L	Hi-Z	External
Write Cycle / Continue Burst	×	×	×	H	H	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	H	Hi-Z	Current
Write Cycle / Masked	×	×	×	H	H	Hi-Z	N/A
Write Cycle / Masked	×	×	×	H	H	Hi-Z	N/A
Write Cycle / Masked	×	×	×	H	H	Hi-Z	N/A

Note Deselect status is held until new “Begin Burst” entry.

Remark × : don’t care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		–0.5		+4.0	V	
Output supply voltage	V_{DDQ}		–0.5		V_{DD}	V	
Input supply voltage	V_{DDI}		–0.5		V_{DD}	V	
Input voltage	V_{IN}		–0.5		V_{DDI} + 0.5	V	1
Input / Output voltage	$V_{I/O}$		–0.5		V_{DDQ} + 0.5	V	1
Operating ambient temperature	T_A		0		70	°C	
Storage temperature	T_{stg}		–55		+125	°C	

Note 1. –1.0 V (MIN.) (Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Notes
Supply voltage	V_{DD}		3.1	3.3	3.5	V	
Output supply voltage	V_{DDQ}		1.8		2.2	V	1
Input supply voltage	V_{DDI}		1.8		2.2	V	1
High level input voltage	V_{IH}		V_{DDI} × 0.65		V_{DDI} + 0.5	V	
Low level input voltage	V_{IL}		–0.5		V_{DDI} × 0.35	V	2

Notes 1. $V_{DDI} = V_{DDQ}$

2. –1.0 V (MIN.) (Pulse width : 2 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Notes
Input capacitance	C_{IN}	V_{IN} = 0 V	3.2	4.0	4.8	pF	1
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	5.1	6.0	6.9	pF	1
Clock input capacitance	C_{clk}	V_{clk} = 0 V	3.6	4.0	4.4	pF	2
Capacitance variation Part to part same pin	C_{var_PP}		–0.25		+0.25	pF	

Notes 1. /AC, STRB and /STRB should be treated as I/O and matched to the I/O pins.

2. C_{clk} capacitance is specified for both CLK and SCLK.

Remark These parameters are periodically sampled and not 100% tested.

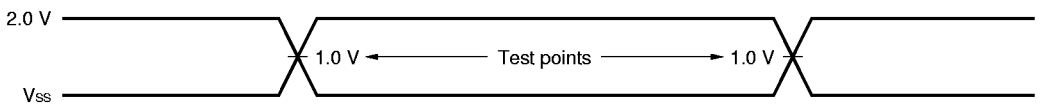
DC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.2 V)

	Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit	Note
	Input leakage current	I_{LI}	V_{IN} = 0 V to V_{DD}I		–10		+10	μA	
	I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{DD}I, Output disabled.		–10		+10	μA	
★	Operating supply current	I_{DD}	Device selected, Cycle = MAX.,	-A33			350	mA	
			V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{DD}I – 0.2 V	-A36			350		
				-A40			350		
				-A44			350		
				-A50			350		
★	Operating V_{DD}Q and V_{DD}I supply current	I_{DD}Q	All outputs toggling, Cycle = MAX.,	-A33			343	mA	
			$C_{I/O}$ = 24 pF	-A36			343		
				-A40			311		
				-A44			280		
				-A50			249		
★	Standby supply current	I_{SB}	Device deselected, Cycle = MAX.,	-A33			63	mA	
			V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{DD}I – 0.2 V,	-A36			63		
			All inputs are static.	-A40			63		
				-A44			57		
				-A50			50		
		I_{SB1}	Device deselected, Cycle = 0 MHz, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{DD}I – 0.2 V, All inputs are static.				3.5	mA	
	High level output voltage	V_{OH}	V_{DD}Q = 2.0 ± 0.2 V, I_{OH} = –1 mA		V_{DD}Q–0.4		V_{DD}Q+0.5	V	
	Low level output voltage	V_{OL}	V_{DD}Q = 2.0 ± 0.2 V, I_{OL} = +1 mA		–0.5		0.4	V	

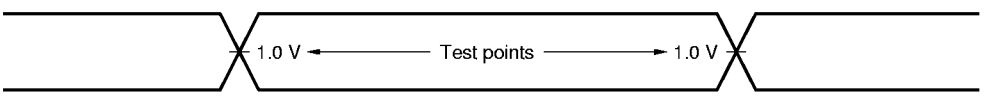
AC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.2 V, $V_{DD}Q$ = $V_{DD}I$ = 2.0 ± 0.2 V)

AC Test Conditions

Input waveform (Rise / Fall time ≤ 2.0 ns)



Output waveform

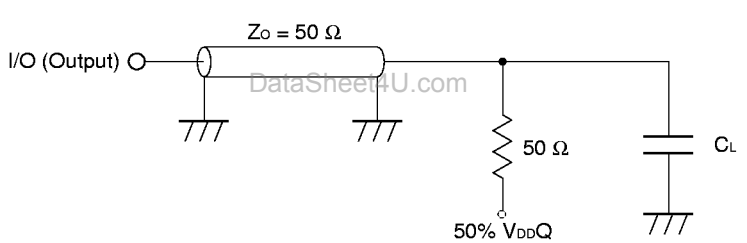


Output load condition

C_L : 10 pF

5 pF (TDC1, TCZ)

Figure External load at test

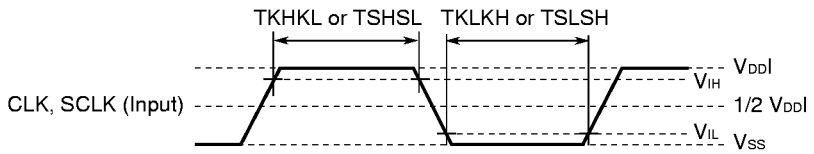


Remark C_L includes capacitances of the probe and jig, and stray capacitances.

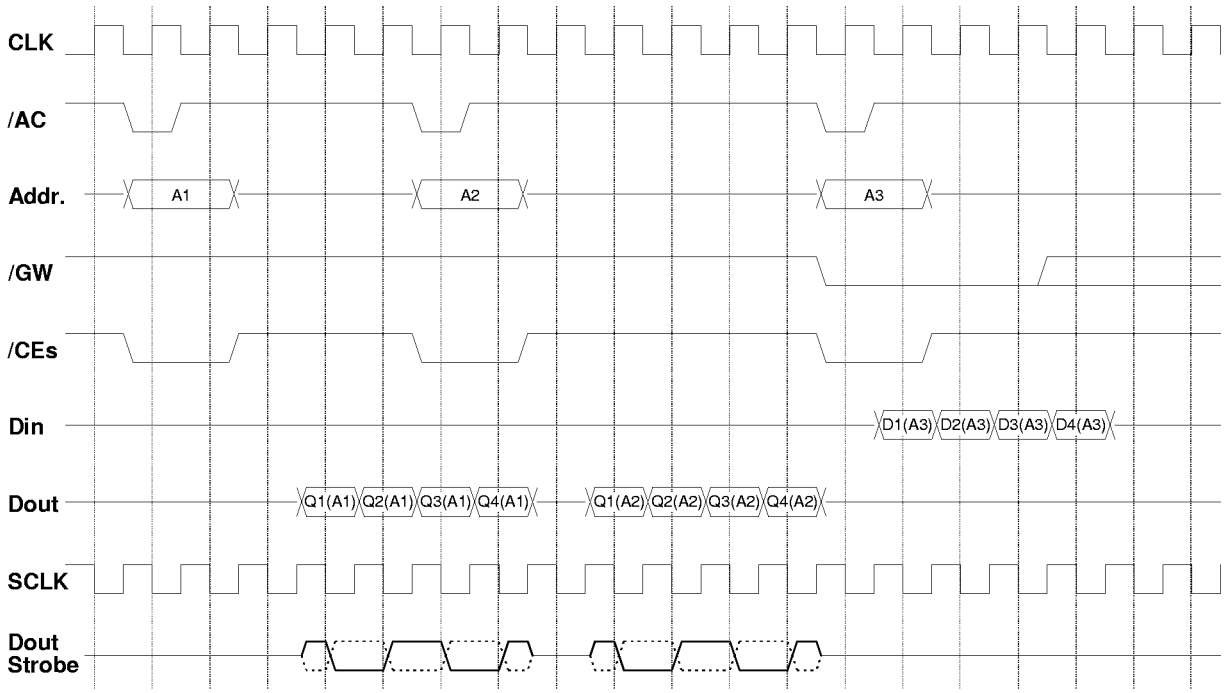
★ Read and Write Cycle

Parameter		Symbol		-A33 (300 MHz)		-A36 (275 MHz)		-A40 (250 MHz)		-A44 (225 MHz)		-A50 (200 MHz)		Unit	Note
		Standard	Alias	MIN.	MAX.	MIN.	MAX.	MIN.	MIN.	MAX.	MAX.	MIN.	MAX.		
Clock cycle time		TKHKH	t_{KC}	3.33	–	3.63	–	4.0	–	4.44	–	5.0	–	ns	
Clock access time		TKHQV	t_{KQ}	–	3.23	–	3.53	–	3.9	–	4.34	–	4.9	ns	
Clock high to output active		TKHQX1	t_{KQLZ}	0	–	0	–	0	–	0	–	0	–	ns	
Clock high to output Hi-Z		TKHQZ	t_{KQHZ}	–	3.23	–	3.53	–	3.9	–	4.34	–	4.9	ns	
Clock high pulse width		TKHKL	t_{KH}	0.8	–	0.92	–	1.06	–	1.24	–	1.46	–	ns	1
Clock low pulse width		TKLKH	t_{KL}	0.8	–	0.92	–	1.06	–	1.24	–	1.46	–	ns	1
Setup time	Address	TAVKH	t_{AS}	0.4	–	0.4	–	0.5	–	0.5	–	0.5	–	ns	
	Address status	TADSVKH	t_{ADSS}	1.0	–	1.1	–	1.1	–	1.2	–	1.5	–	ns	
	Data-in	TDVKH	t_{WDS}	1.0	–	1.1	–	1.1	–	1.2	–	1.5	–	ns	
	Global write	TWVKH	t_{WS}	1.0	–	1.1	–	1.1	–	1.2	–	1.5	–	ns	
	Chip enable	TEVKH	t_{CES}	0.4	–	0.4	–	0.5	–	0.5	–	0.5	–	ns	
Hold time	Address	TKHAX	t_{AH}	3.33	–	3.63	–	4.0	–	4.44	–	5.0	–	ns	
	Address status	TKHADSX	t_{ADSH}	0.2	–	0.2	–	0.3	–	0.4	–	0.5	–	ns	
	Data-in	TKHDX	t_{WDH}	0.2	–	0.2	–	0.3	–	0.4	–	0.5	–	ns	
	Global write	TKHWX	t_{WH}	0.2	–	0.2	–	0.3	–	0.4	–	0.5	–	ns	
	Chip enable	TKHEX	t_{CEH}	3.33	–	3.63	–	4.0	–	4.44	–	5.0	–	ns	
Strobe clock cycle time		TSHSH	t_{KCS}	3.33	–	3.63	–	4.0	–	4.44	–	5.0	–	ns	
Strobe clock high pulse width		TSHSL	t_{KHS}	0.8	–	0.92	–	1.06	–	1.24	–	1.46	–	ns	1
Strobe clock low pulse width		TSLSH	t_{KLS}	0.8	–	0.92	–	1.06	–	1.24	–	1.46	–	ns	1
Strobe clock access time		TSHRV	t_{KQS}	–	3.23	–	3.53	–	3.9	–	4.34	–	4.9	ns	
Rising edge CLK to rising edge SCLK		TCLKSCLK	$t_{CLKSCLK}$	1.37	1.97	1.47	2.17	1.60	2.40	1.82	2.62	2.10	2.90	ns	
Dout setup to strobe valid		TQVRV	t_{RDS}	0.75	–	0.82	–	0.9	–	1.00	–	1.15	–	ns	
Dout hold from strobe valid		TRVQX	t_{RDH}	0.75	–	0.82	–	0.9	–	1.00	–	1.15	–	ns	

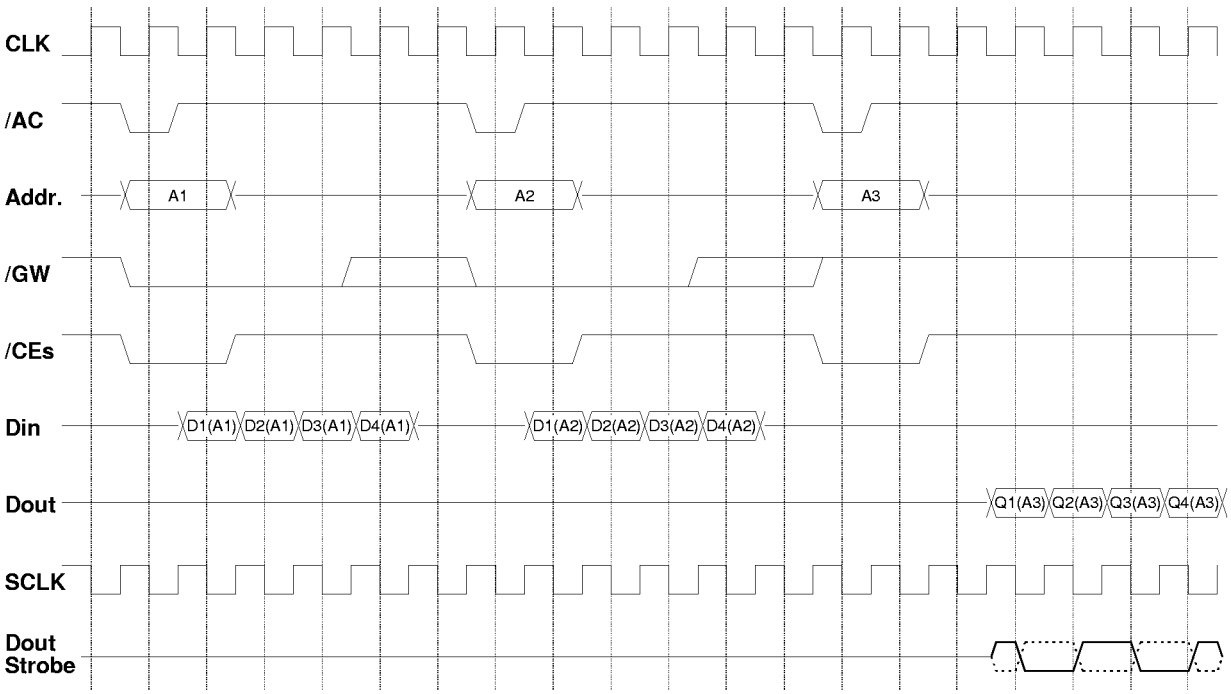
Note 1. Following figure shows the specification of clock pulse width.



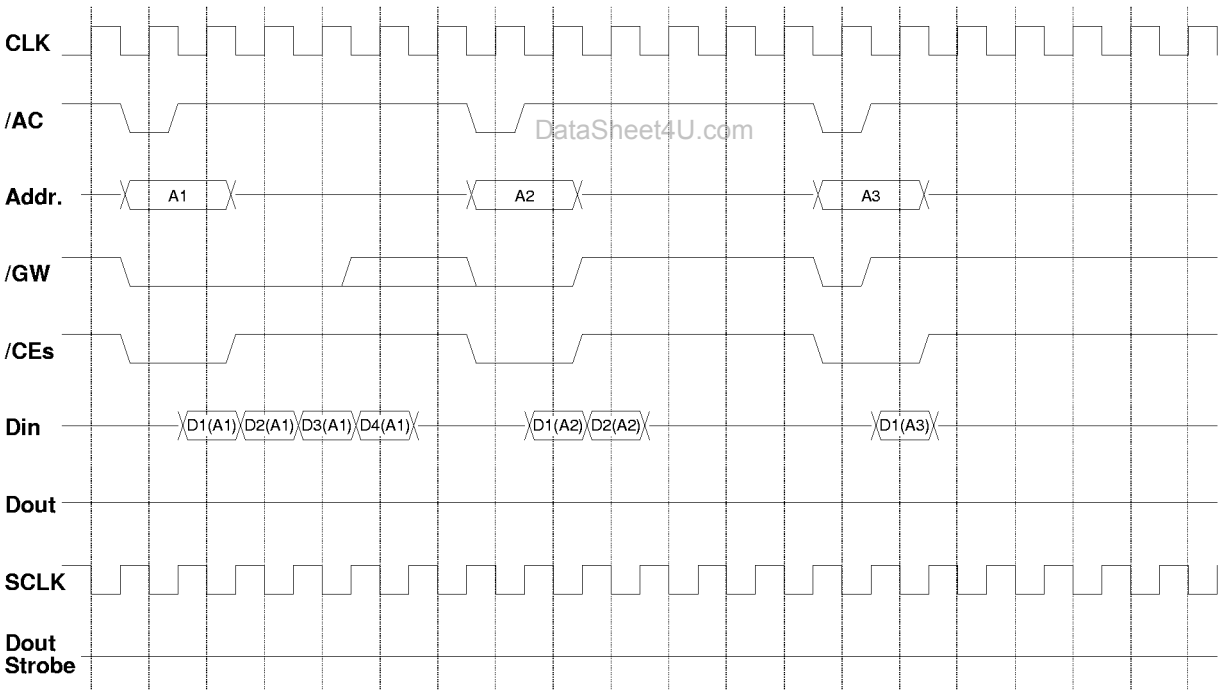
Read - Read - Write



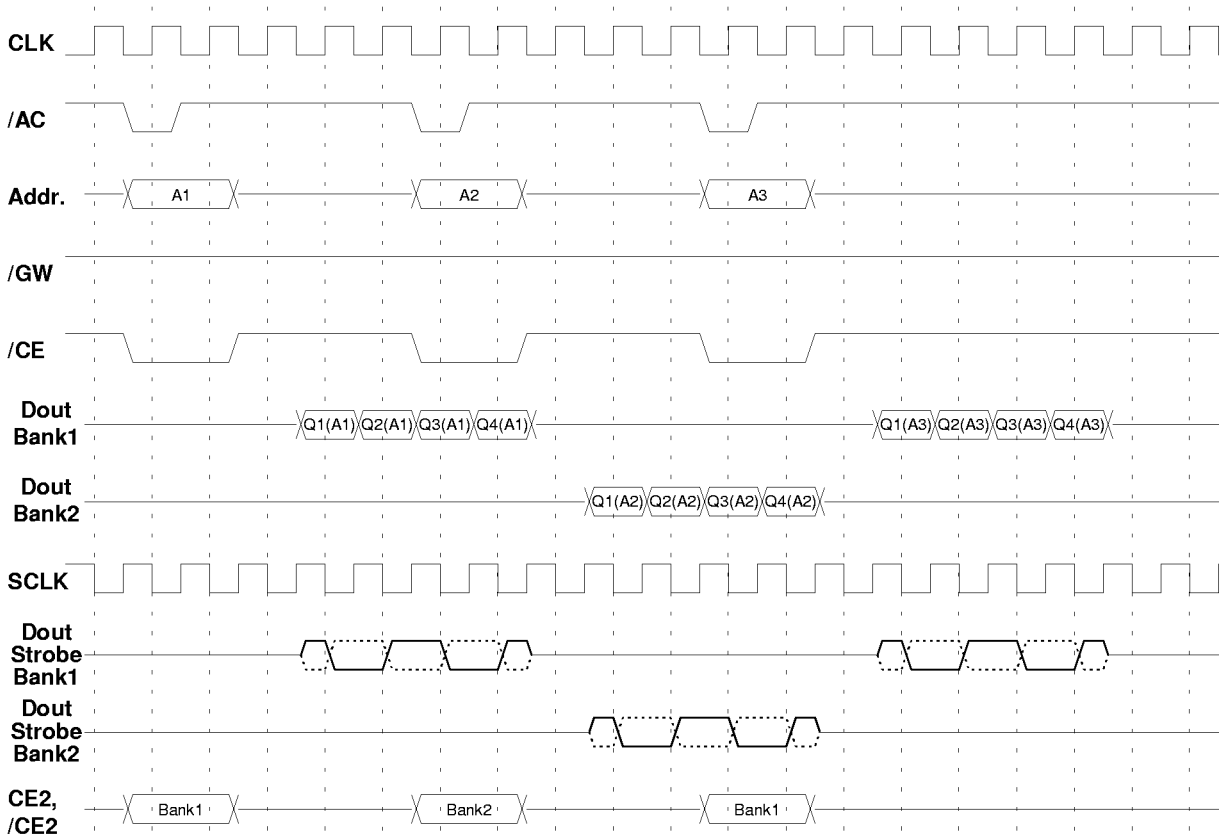
Write - Write - Read



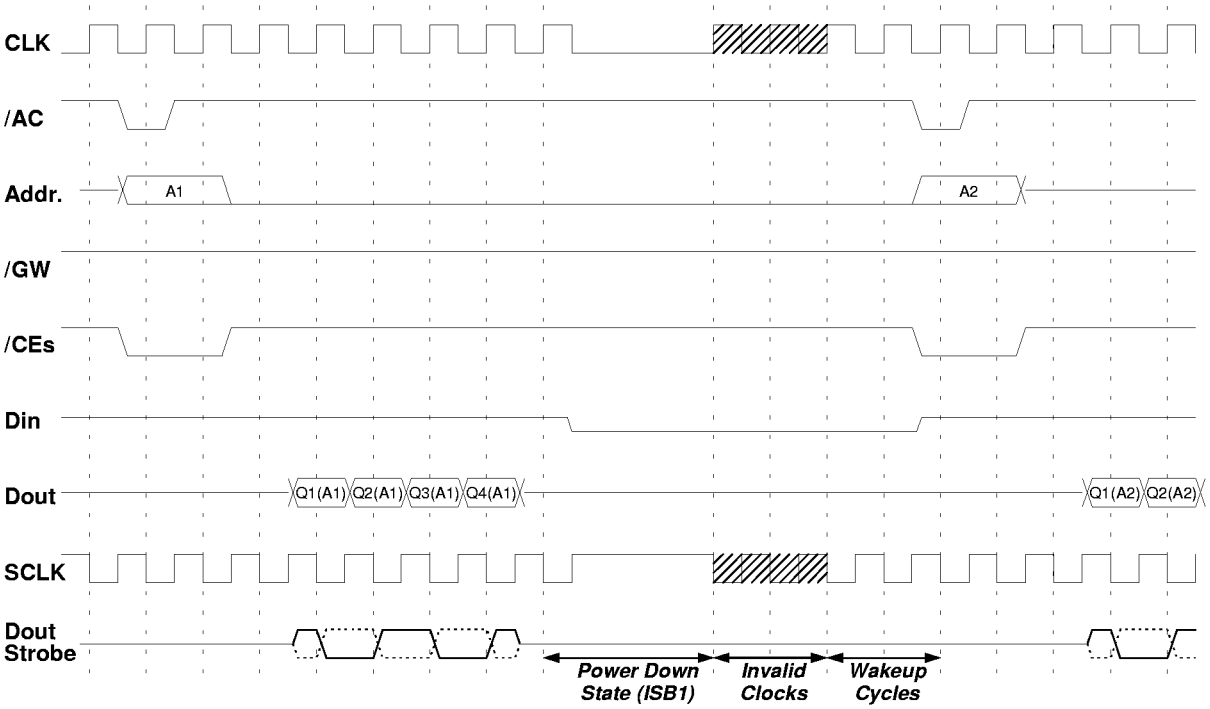
Write (4) - Write (2) - Write (1)



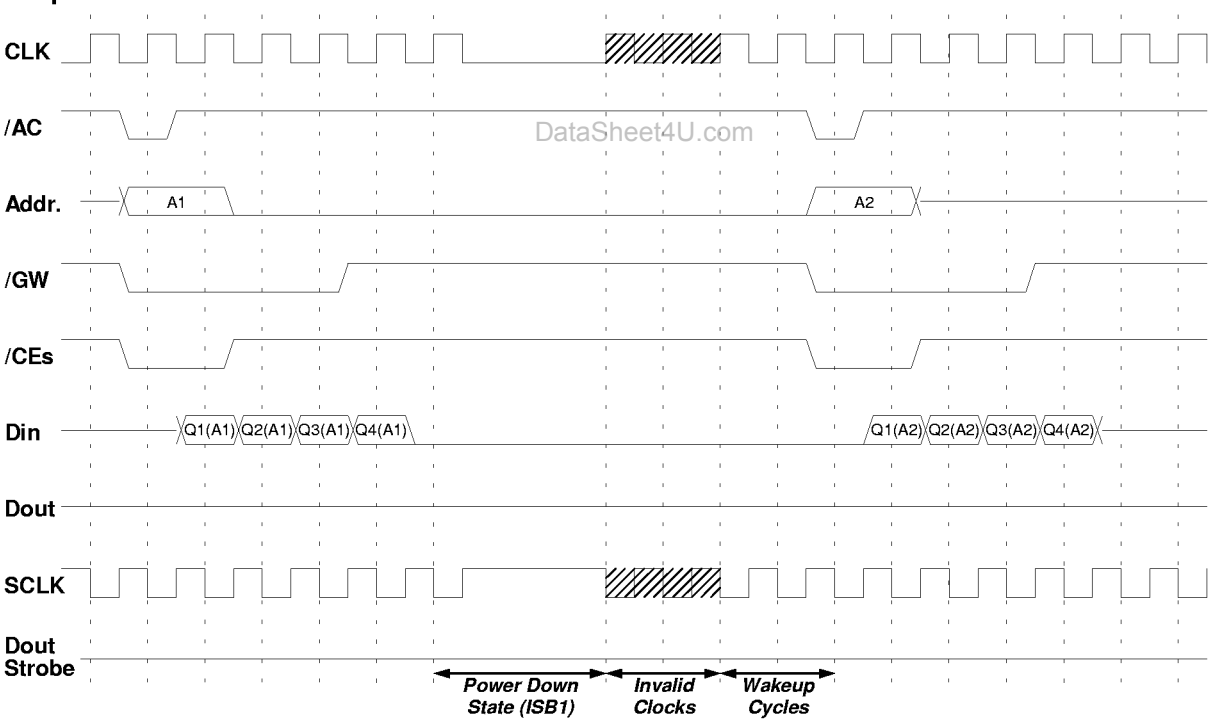
Dual Bank Read



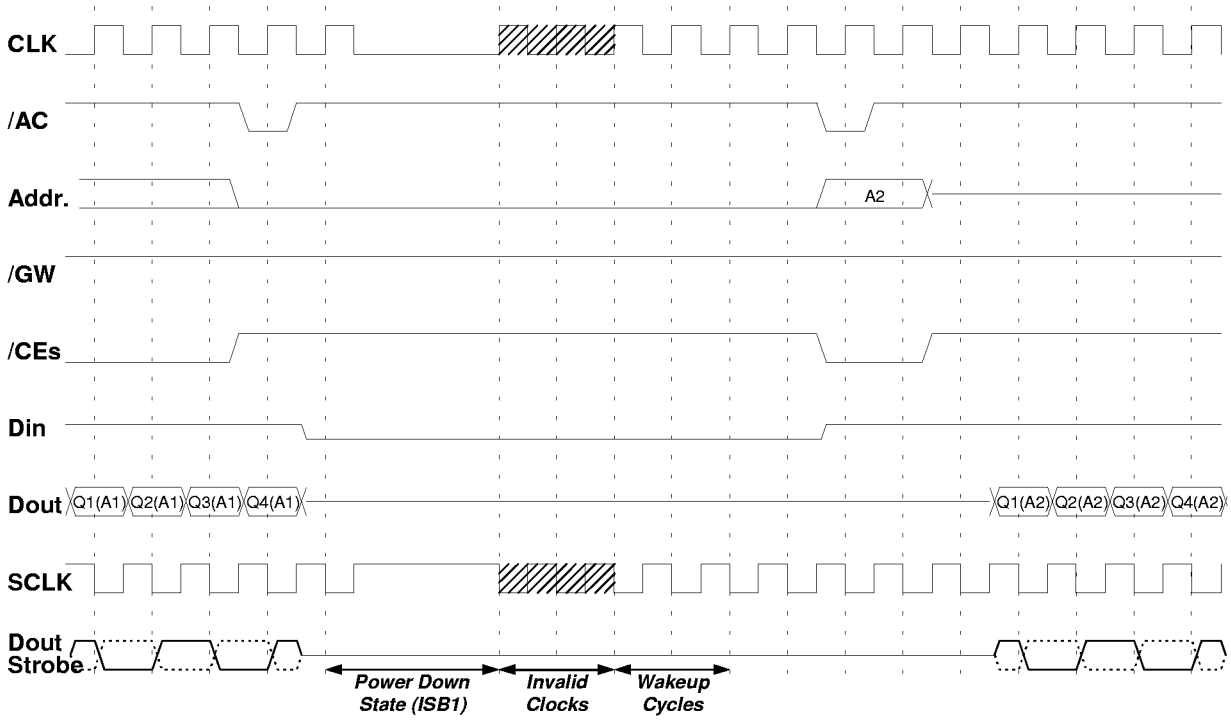
Stop Clock --- Read



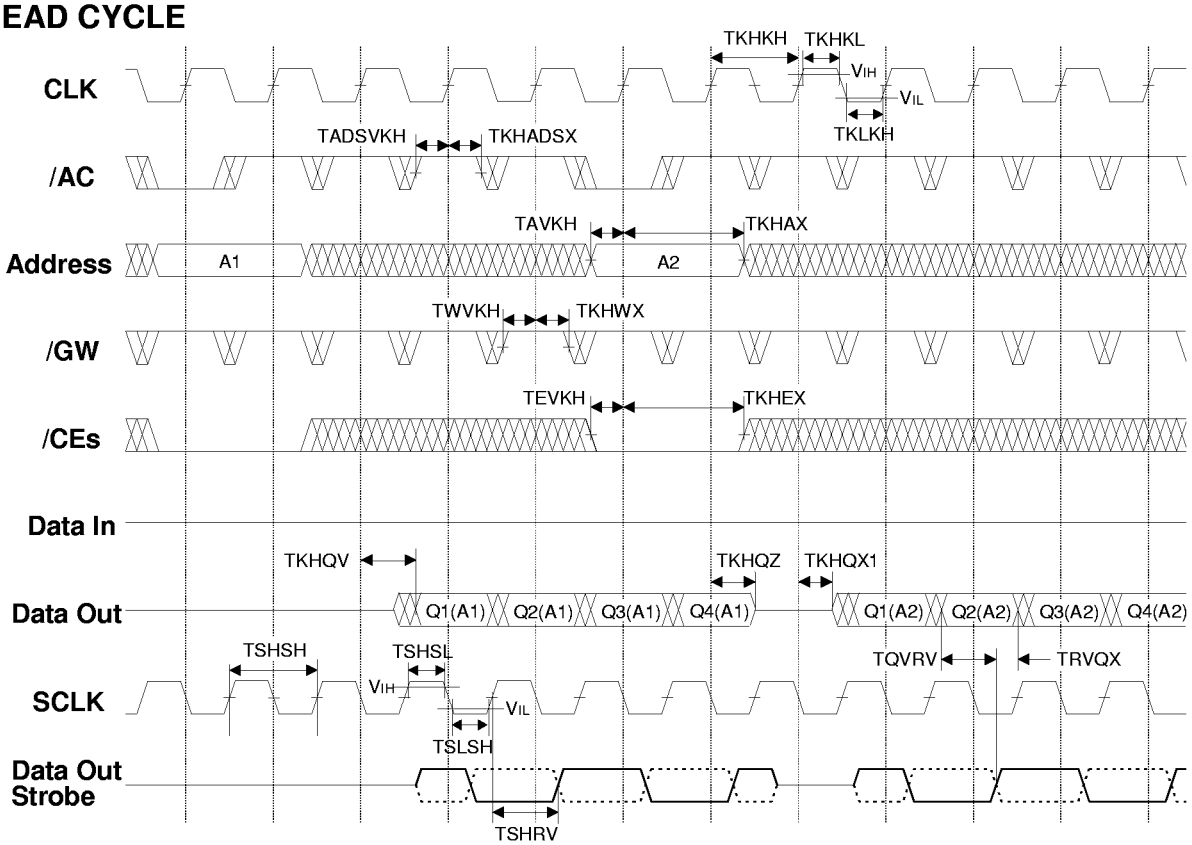
Stop Clock --- Write



Stop Clock --- Deselect



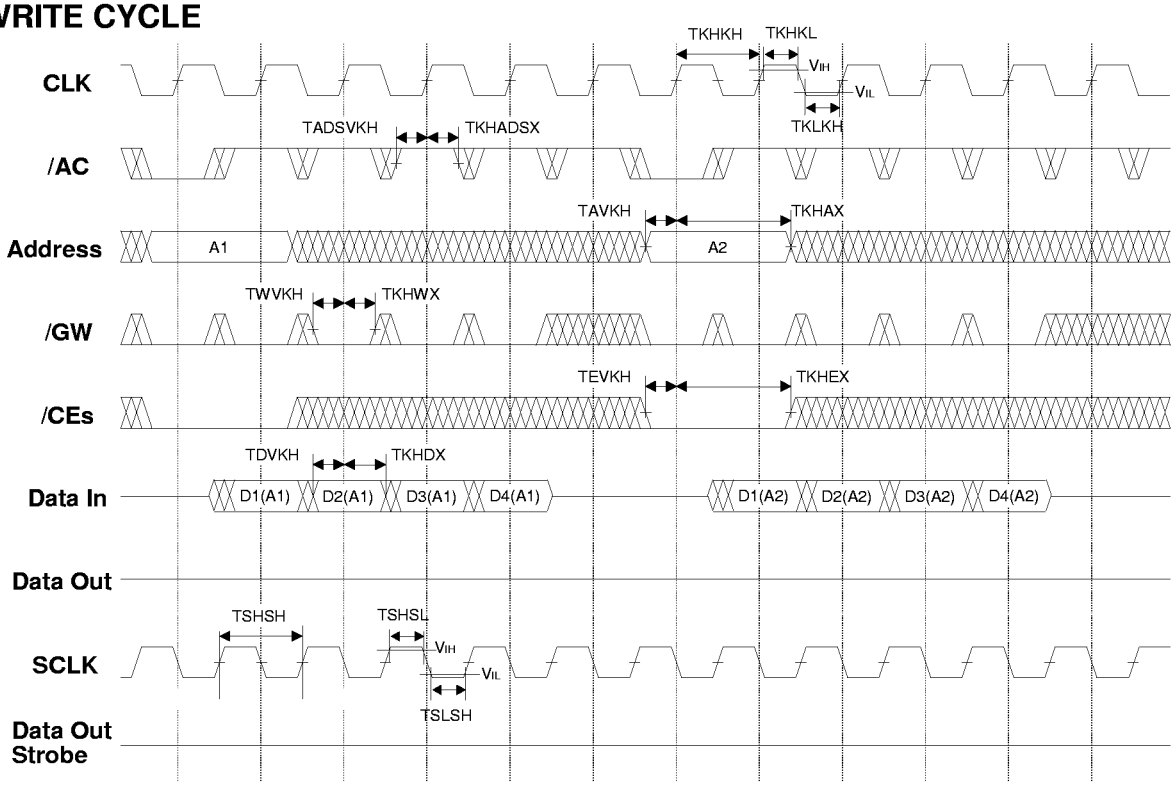
READ CYCLE



Notes 1. Qn (A2) refers to output to address A2. Q1 - Q4 refers to outputs according to burst sequence.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

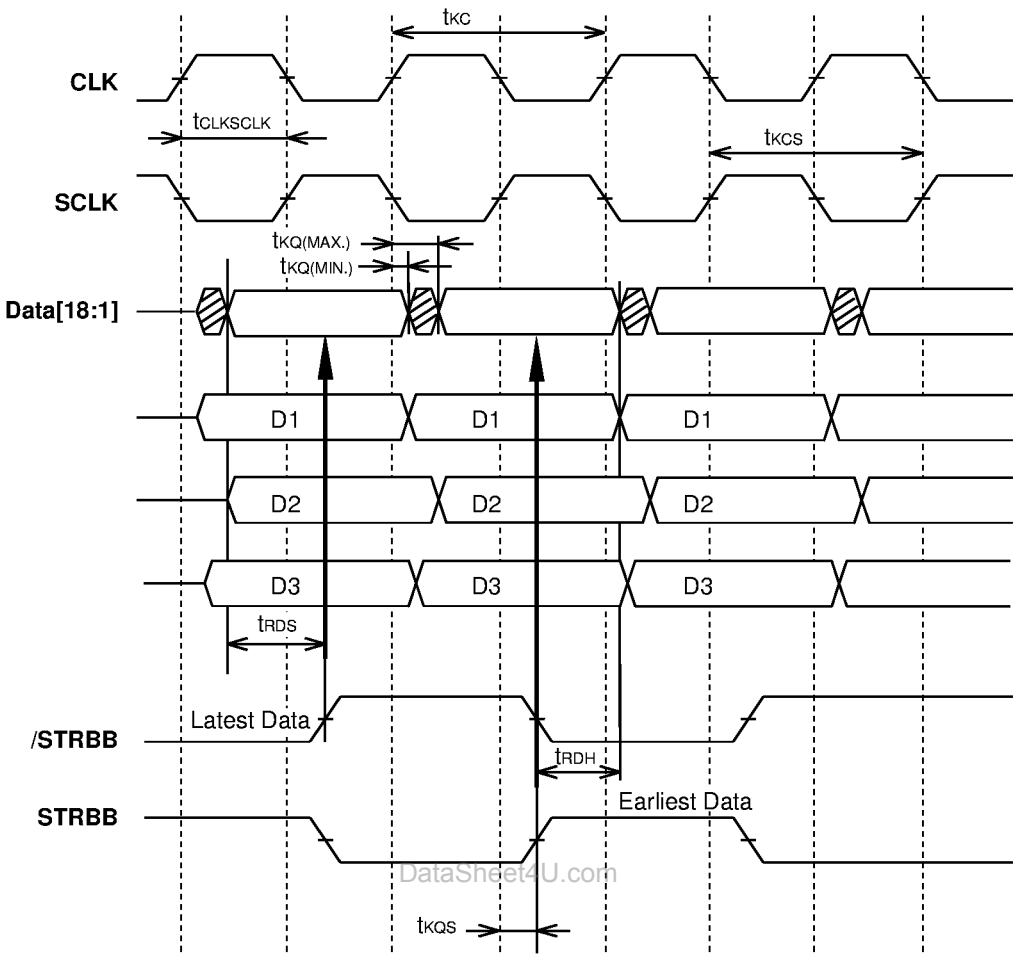
WRITE CYCLE



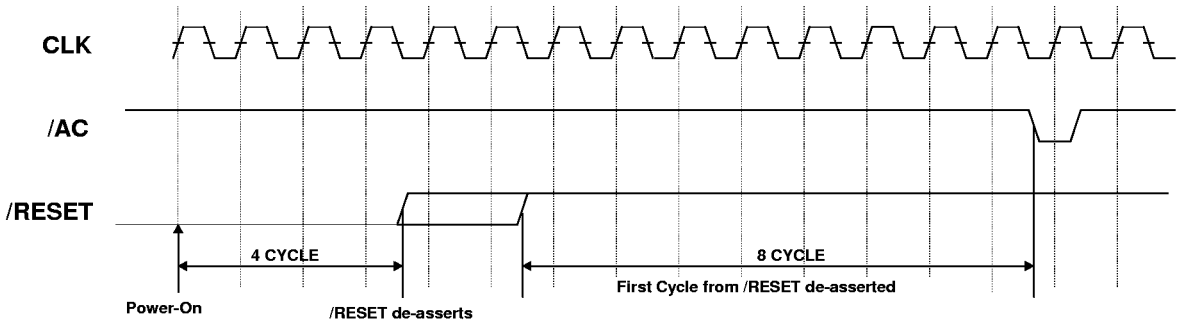
Notes 1. Dn (A2) refers to input to address A2. D1 - D4 refers to inputs according to burst sequence.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

Timing Diagram Reference for Centered Data Strobes



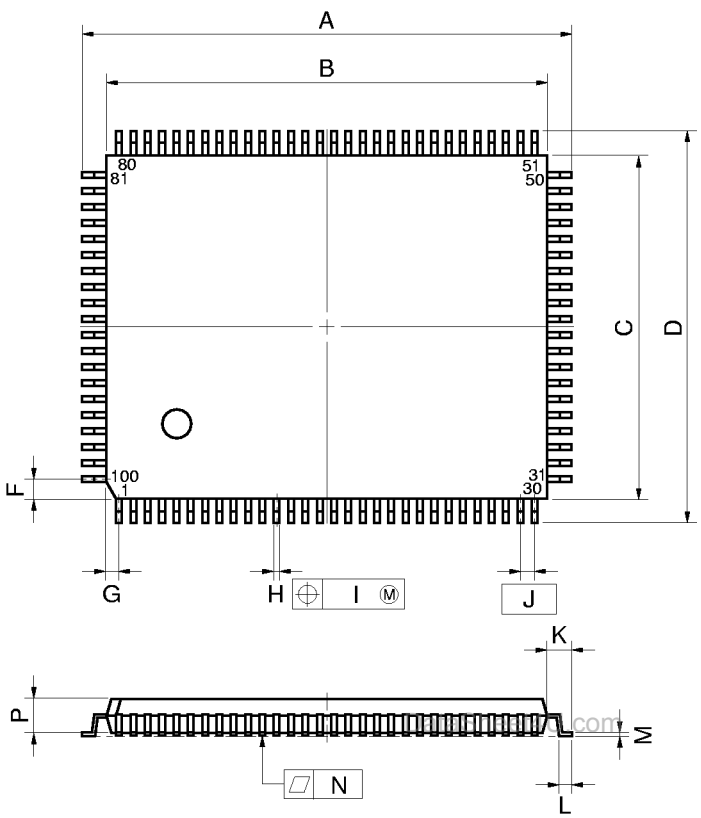
RESET Operation

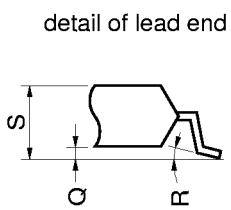


Note This Device needs this Reset Operation after power-up.

Package Drawing

100 PIN PLASTIC LQFP (14×20)





NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	0.825	0.032
G	0.575	0.023
H	$0.32^{+0.08}_{-0.07}$	0.013±0.003
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.06}_{-0.05}$	0.007±0.002
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.7 MAX.	0.067 MAX.

S100GF-65-8ET

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD432836AL.

Type of Surface Mount Devices

μPD432836ALGF : 100-pin plastic LQFP (14 x 20 mm)