μPD434000
524,288 x 8-Bit
Static CMOS RAM

Description

The μPD434000 is a 524,288-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with thin-film transistor (TFT) loads make the μPD434000 a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of $\overline{OE}$ and $\overline{WE}$. Data retention is guaranteed at a power supply voltage as low as 2 volts.

The μPD434000 is available in standard 32-pin DIP, SOP, and TSOP plastic packaging.

Features

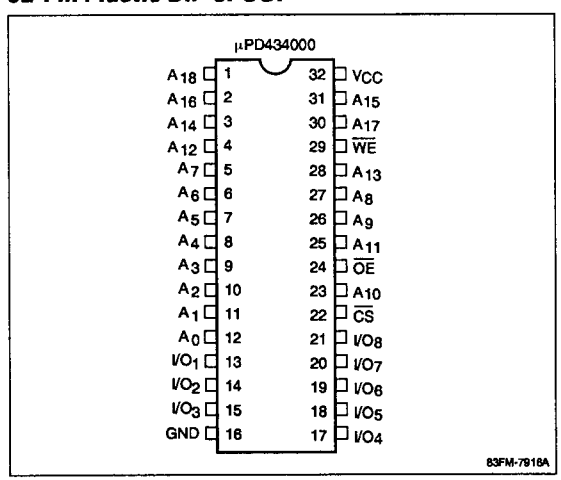
- 524,288-word by 8-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Chip select ($\overline{CS}$) and output enable ($\overline{OE}$) inputs for easy application
- Data retention current of 0.5 μA typical
- Data retention voltage of 2 V minimum
- Packages: 32-pin plastic DIP, SOP, and TSOP

Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
I/O_1 - I/O_8	Data inputs/outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

32-Pin Plastic DIP or SOP



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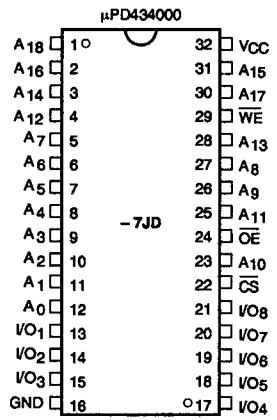
Pin Configurations (cont)

32-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

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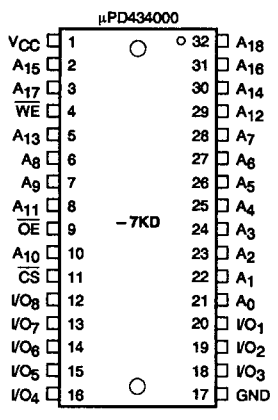
32-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes normal pinout sequence.

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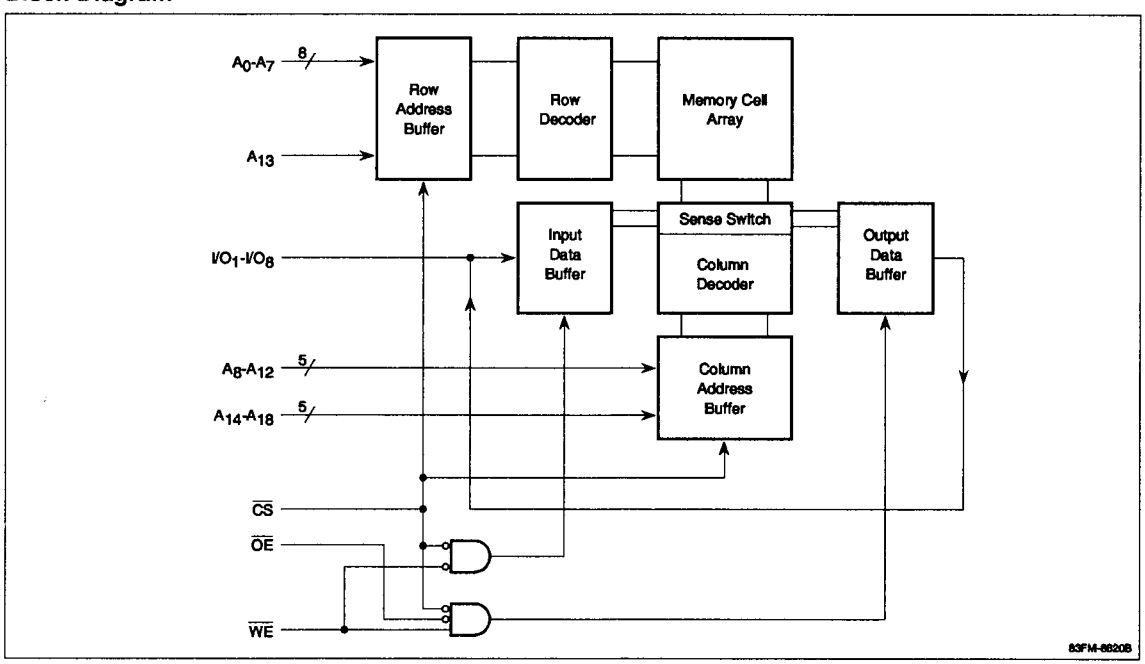
Block Diagram



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Ordering Information

Part Number	Access Time (max)	Standby Supply Current	Package
μPD434000CZ-55	55 ns	2 mA	32-pin plastic DIP
CZ-70	70 ns		
CZ-85	85 ns		
CZ-10	100 ns		
μPD434000CZ-55L	55 ns	0.1 mA	
CZ-70L	70 ns		
CZ-85L	85 ns		
CZ-10L	100 ns		
μPD434000CZ-55LL	55 ns	0.05 mA	
CZ-70LL	70 ns		
CZ-85LL	85 ns		
CZ-10LL	100 ns		
μPD434000GW-55	55 ns	2 mA	32-pin plastic SOP
GW-70	70 ns		
GW-85	85 ns		
GW-10	100 ns		
μPD434000GW-55L	55 ns	0.1 mA	
GW-70L	70 ns		
GW-85L	85 ns		
GW-10L	100 ns		
μPD434000GW-55LL	55 ns	0.05 mA	
GW-70LL	70 ns		
GW-85LL	85 ns		
GW-10LL	100 ns		

Ordering Information (cont)

Part Number	Access Time (max)	Standby Supply Current	Package
μPD434000G5-55	55 ns	2 mA	32-pin plastic TSOP (normal pinouts)
G5-70	70 ns		
G5-85	85 ns		
G5-10	100 ns		
μPD434000G5-55L	55 ns	0.1 mA	
G5-70L	70 ns		
G5-85L	85 ns		
G5-10L	100 ns		
μPD434000G5-55LL	55 ns	0.05 mA	
G5-70LL	70 ns		
G5-85LL	85 ns		
G5-10LL	100 ns		
μPD434000G5M-55	55 ns	2 mA	32-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns		
G5M-85	85 ns		
G5M-10	100 ns		
μPD434000G5M-55L	55 ns		
G5M-70L	70 ns	0.1 mA	
G5M-85L	85 ns		
G5M-10L	100 ns		
μPD434000G5M-55LL	55 ns		
G5M-70LL	70 ns	0.05 mA	
G5M-85LL	85 ns		
G5M-10LL	100 ns		

Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) −3.0 V minimum (pulse width = 30 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter †	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Input/output capacitance	$C_{I/O}$			10	pF

† Parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Note:

(1) −3.0 V minimum (pulse width = 30 ns).

Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
D_{OUT} disabled	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

X = don't care.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD434000			μPD434000-L			μPD434000-LL				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	−1		1	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	−1		1	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{CS}$ = V_{IH}
Operating supply current	I_{CCA2}			15			15			15	mA	$I_{I/O}$ = 0 mA; $\overline{CS}$ = V_{IL}
	I_{CCA3}			15			15			15	mA	$\overline{CS}$ ≤ 0.2 V; t_{RC} = 1 μs; V_{IL} ≤ 0.2 V; V_{IH} ≥ V_{CC} − 0.2 V; $I_{I/O}$ = 0 mA
Standby supply current	I_{SB}			5			3			3	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}		0.02	2		0.002	0.1		0.001	0.05	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4			0.4			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			2.4			2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V_{CC} − 0.5			V_{CC} − 0.5			V	I_{OH} = −0.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; see figure 1 for ac test conditions.

		-55		-70		-85		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating supply current	I_{CCA1}		70		65		60		55	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); $I_{I/O}$ = 0 mA
Address access time	t_{AA}		55		70		85		100	ns	
$\overline{CS}$ access time	t_{ACS}		55		70		85		100	ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address valid to end of write	t_{AW}	50		60		70		80		ns	
$\overline{CS}$ to output in high-Z	t_{CHZ}		25		30		30		35	ns	
$\overline{CS}$ to output in low-Z	t_{CLZ}	10		10		10		10		ns	
$\overline{CS}$ to end of write	t_{CW}	50		60		70		80		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		35		40		ns	
Output enable to output valid	t_{OE}		30		35		45		50	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
Output enable to output in high-Z	t_{OHZ}		25		30		30		35	ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns	
Output active from end of write	t_{OW}	5		5		5		5		ns	
Read cycle time	t_{RC}	55		70		85		100		ns	
Write cycle time	t_{WC}	55		70		85		100		ns	
Write enable to output in high-Z	t_{WHZ}		25		30		30		35	ns	
Write pulse width	t_{WP}	45		55		65		70		ns	
Write recovery time	t_{WR}	5		5		5		5		ns	

Low V_{CC} Data Retention Characteristics

T_A = 0 to +70°C; see figure 2 for timing diagram.

		-L Version			-LL Version				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2		5.5	2		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	† I_{CCDR1}		1	50		0.5	20	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselection to data retention	t_{CDR}	0			0			ns	
Operation recovery time	t_R	5			5			ms	

† At 0 to 40°C, the maximum for I_{CCDR1} is 15 μA for the -L version and 3 μA for the -LL version.

Figure 1. AC Test Conditions

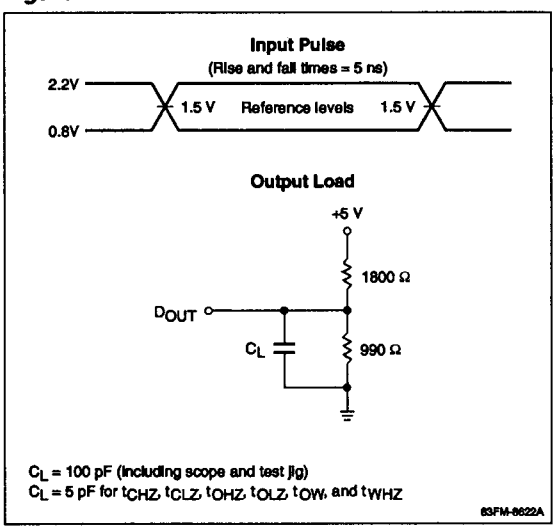
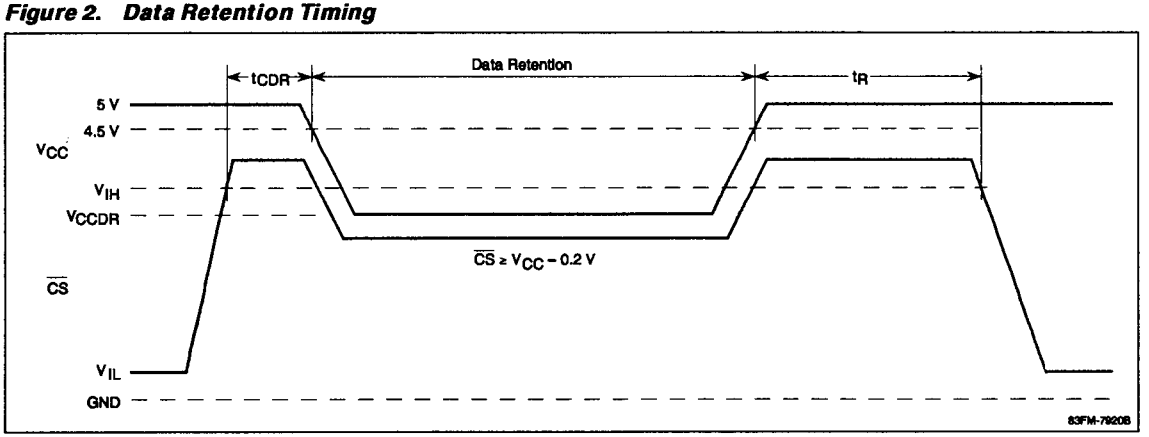
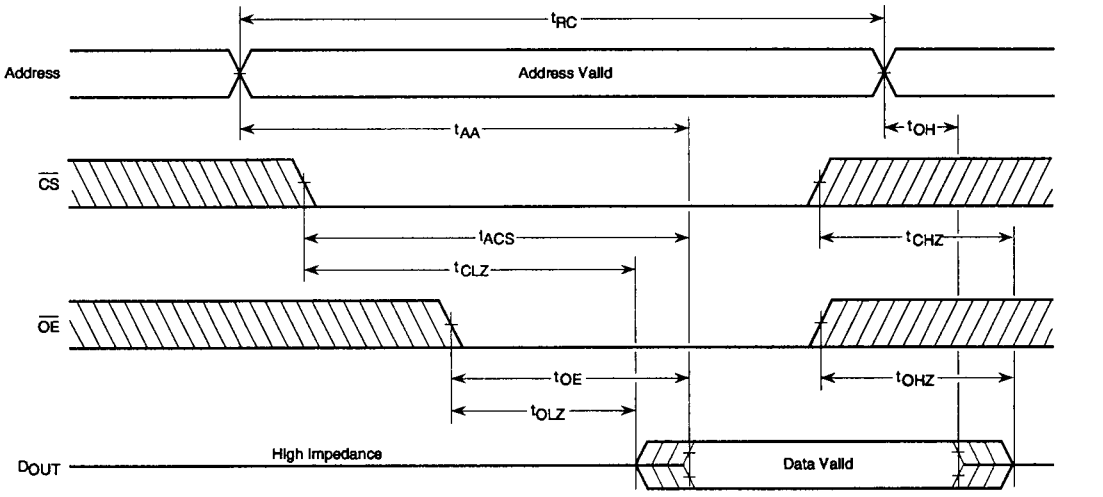


Figure 2. Data Retention Timing



Timing Waveforms

Read Cycle



Notes:
[1] $\overline{WE}$ is high for a read cycle.

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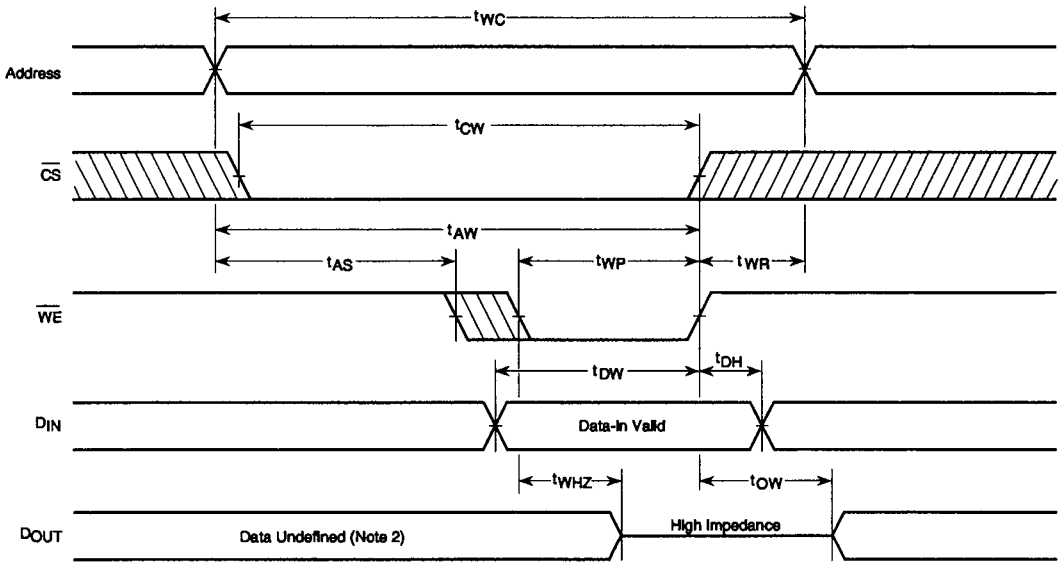
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[2] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to the output must not be applied.

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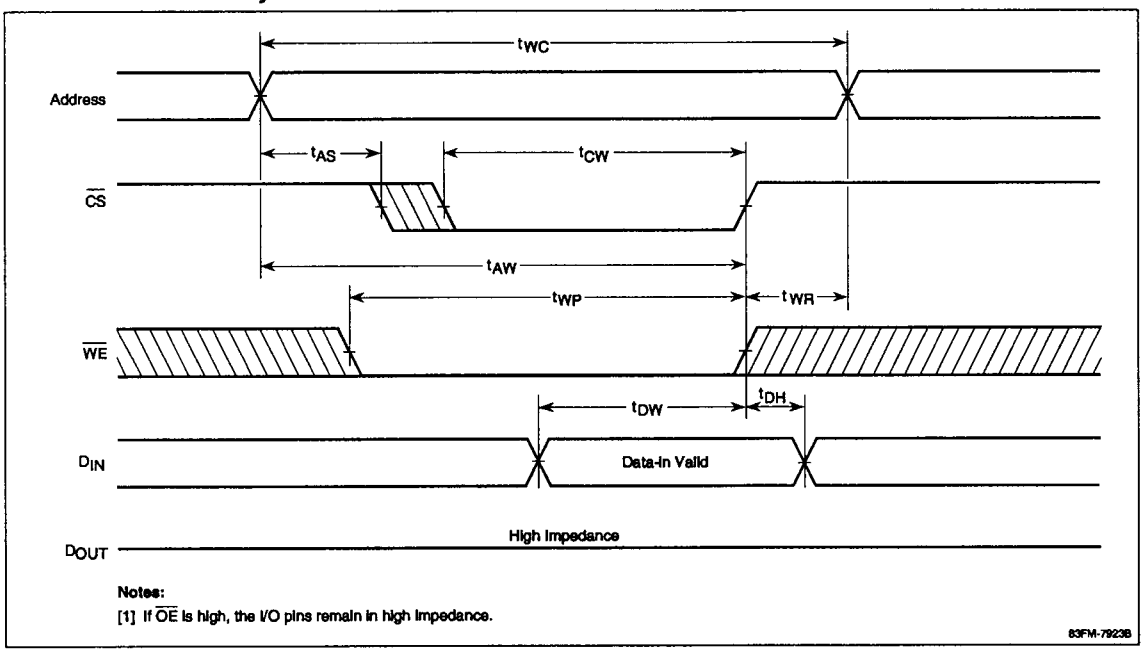
24d

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:
[1] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

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