NEC

MOS INTEGRATED CIRCUIT

μPD434001

4M-BIT CMOS FAST STATIC RAM
4M-WORD BY 1-BIT

Description

The μPD434001 is a high speed, low power, 4,194,304 bits (4,194,304 words by 1 bit) CMOS static RAM.
The μPD434001 is packed in 32-pin plastic SOJ.

Features

- 4,194,304 words by 1 bit organization
- Fast access time 20 ns (MAX.)
- $\overline{OE}$ input for easy application
- Test mode function on chip

Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply current mA (MAX.)	Standby supply current mA (MAX.)
μPD434001LE-20	32-pin plastic SOJ (400 mil)	20	140	10
μPD434001LE-25		25	130	

The information in this document is subject to change without notice.

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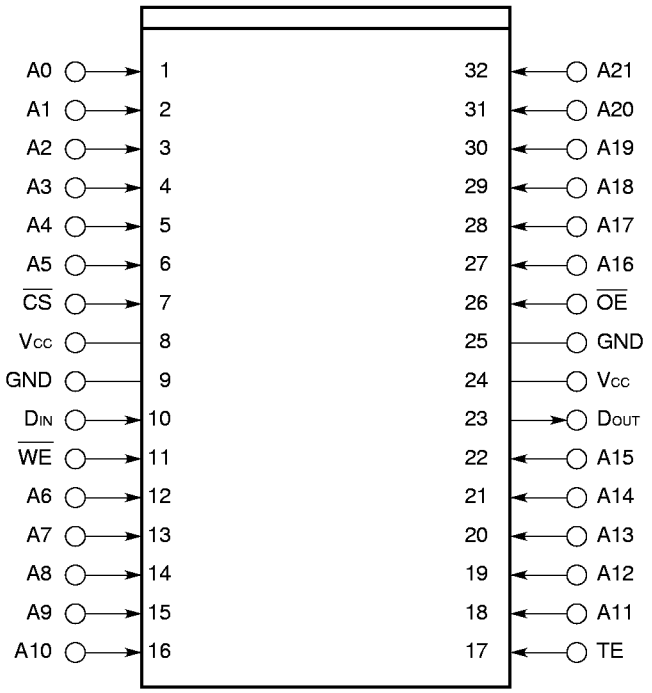
Pin Configuration (Marking Side)

32-pin plastic SOJ (400 mil)

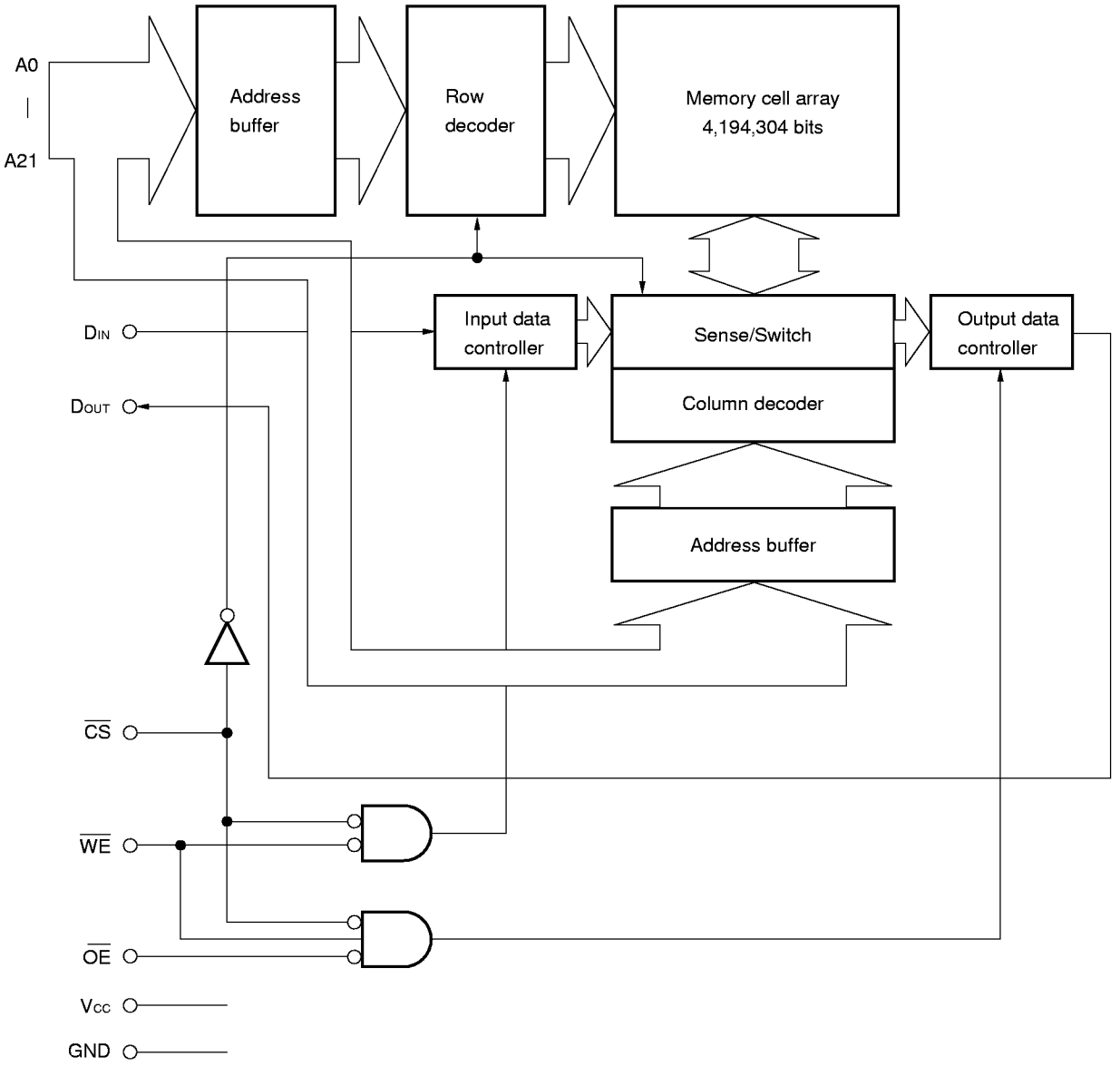
μPD434001LE-20
μPD434001LE-25



A0 – A21	:	Address inputs
D_{IN}	:	Data input
D_{OUT}	:	Data output
$\overline{CS}$	:	Chip Select
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground
TE [Note]	:	Test mode Enable

Note TE should be connected to GND in normal operation.

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	×	×	Not selected	Hi-Z	I_{SB}
L	H	H	Output disable		I_{CC}
L	L	H	Read	D_{OUT}	
L	×	L	Write	D_{IN}	

Remark × : Don't care

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5[Note] to +7.0	V
Input/Output voltage	V_T	−0.5[Note] to V_{CC} + 0.3	V
Operating ambient temperature	T_A	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note −2.0 V (MIN.) (Pulse width: 10 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
High level input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Low level input voltage	V_{IL}	−0.5[Note]		+0.8	V
Operating ambient temperature	T_A	0		+70	°C

Note −2.0 V (MIN.) (Pulse width: 10 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–2		+2	μA
Output leakage current	I_{LO}	V_{OUT} = 0 V to V_{CC}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		–2		+2	μA
Operating supply current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA, Minimum cycle	μPD434001-20			140	mA
			μPD434001-25			130	
Standby supply current	I_{SB}	$\overline{CS}$ = V_{IH}, Minimum cycle	μPD434001-20			60	mA
			μPD434001-25			50	
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} – 0.2 V, V_{IN} ≧ V_{CC} – 0.2 V or V_{IN} ≦0.2 V				10	
High level output voltage	V_{OH}	I_{OH} = –4.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 8 mA				0.4	V

Remark V_{IN}: Input voltage

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input/Output capacitance	C_{OUT}	V_{OUT} = 0 V			10	pF

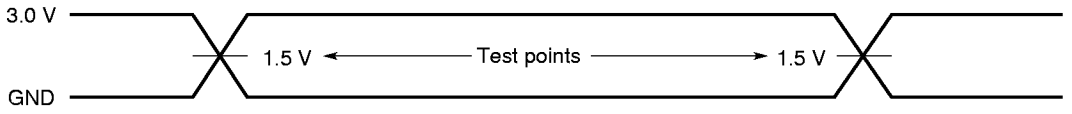
Remarks **1.** V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

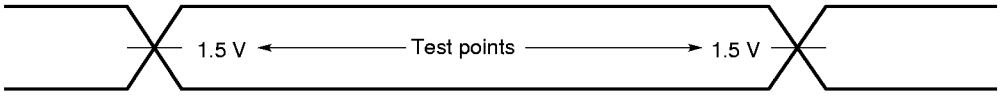
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/fall time ≦ 3 ns)



Output waveform



Output load

AC Characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2.**

Figure 1

(For t_{AA}, t_{ACS}, t_{OE}, t_{OH})

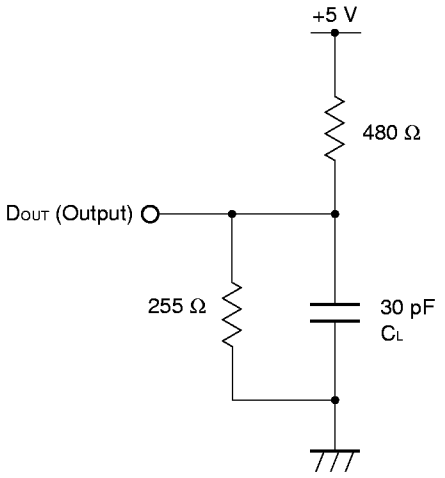
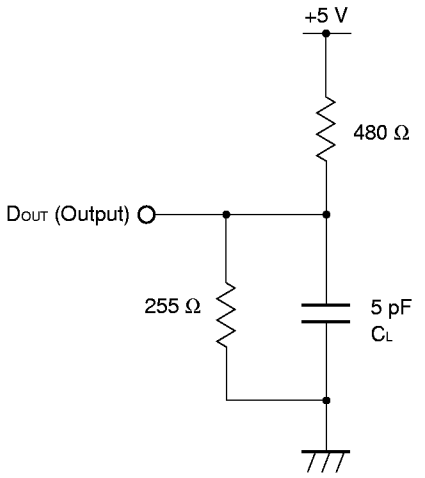


Figure 2

(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

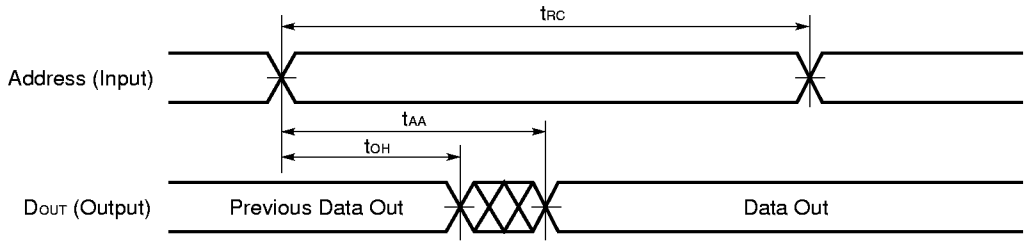
Read Cycle

Parameter	Symbol	μPD434001LE-20		μPD434001LE-25		Unit	Conditions
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	20		25		ns	
Address access time	t_{AA}		20		25	ns	**Note 1.**
$\overline{CS}$ access time	t_{ACS}		20		25	ns	
$\overline{OE}$ access time	t_{OE}		10		12	ns	
Output hold from address change	t_{OH}	3		3		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	3		3		ns	**Note 2.**
$\overline{OE}$ to output in low impedance	t_{OLZ}	0		0		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		8		10	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		8		10	ns	

Notes 1. See the output load shown in **Figure 1**.

2. See the output load shown in **Figure 2**.

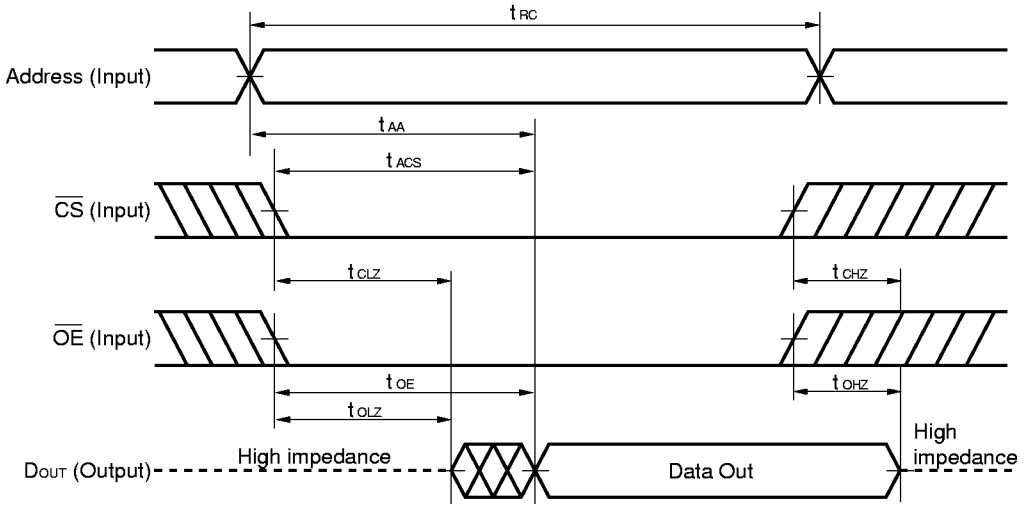
Read Cycle Timing Chart 1 (Address Access)



Remarks 1. In read cycle, $\overline{WE}$ should be fixed to high level.

2. $\overline{CS} = \overline{OE} = V_{IL}$

Read Cycle Timing Chart 2 ($\overline{CS}$ Access)



Caution Address valid prior to or coincident with $\overline{CS}$ low level input.

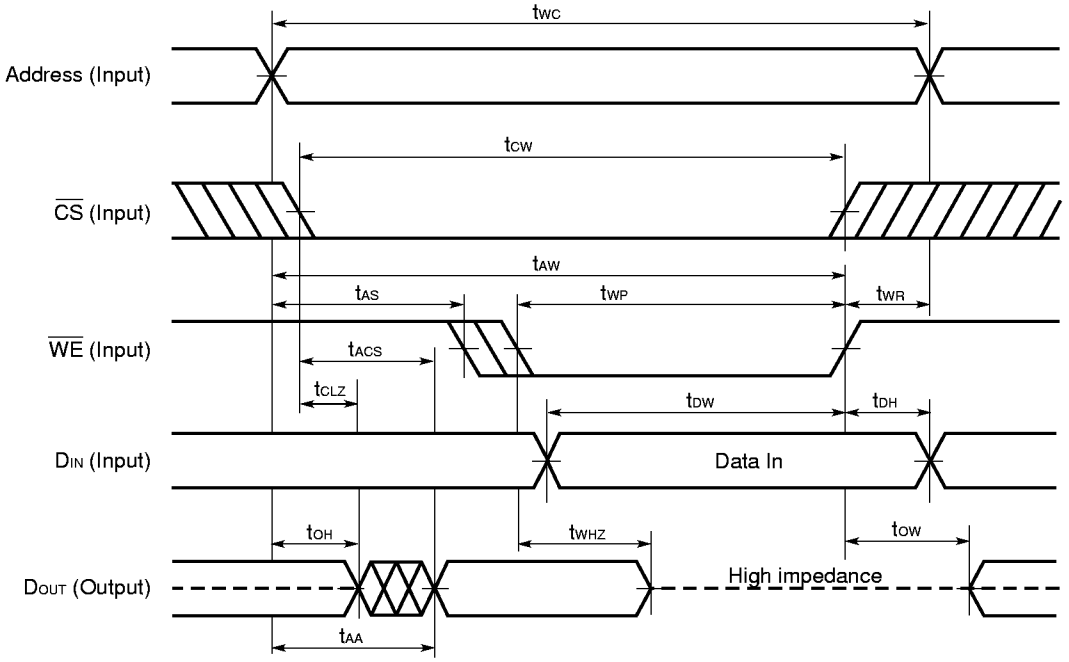
Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle

Parameter	Symbol	μPD434001LE-20		μPD434001LE-25		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	20		25		ns	
$\overline{CS}$ to end of write	t_{CW}	14		17		ns	
Address valid to end of write	t_{AW}	14		17		ns	
Write pulse width	t_{WP}	12		15		ns	
Data valid to end of write	t_{DW}	10		12		ns	
Data hold time	t_{DH}	0		0		ns	
Address setup time	t_{AS}	0		0		ns	
Write recovery time	t_{WR}	3		3		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		8		10	ns	**Note**
Output active from end of write	t_{OW}	0		0		ns	

Note See the output load shown in **Figure 2**.

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remarks 1. Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

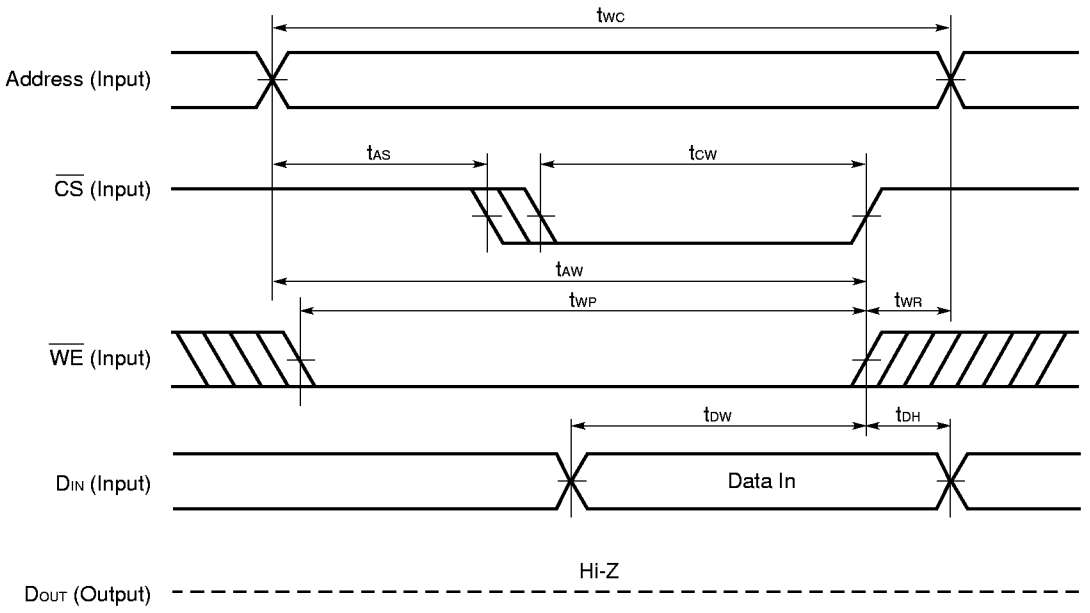
2. When $\overline{WE}$ is at low level, the D_{OUT} pin is always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the D_{OUT} pin high impedance.

3. t_{WR} is measured between rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and end of t_{WC}.

4. t_{WHZ} is measured at V_{OL} + 200 mV and V_{OH} – 200 mV with the output load shown in **Figure 2**.

5. t_{OW} is measured at ±200 mV from steady-state voltage with the output load shown in **Figure 2**.

Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)



Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remarks 1. Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

2. t_{WR} is measured between rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and end of t_{WC}.

Test Mode

Test mode is used to test the memory cells in a shorter time than normal testing. Test mode reduces test time to 1/8. In this test mode, internal organization is apparently 512K words by 8 bits. Input levels of A19, A20 and A21 pin do not need to be controlled.

1. How to enter test mode

To enter the test mode, execute the test mode set cycle.

2. Read/Write in test mode

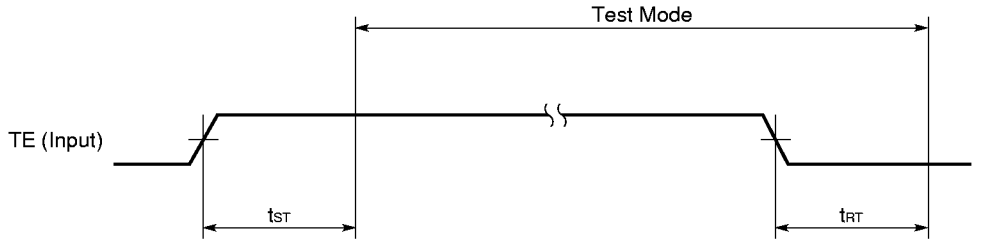
Write data of "1" or "0" from D_{IN} pin. Write operation is performed with 8 bits written at once. Therefore, 8-bit data in total are written at a write operation.

Then user should change the write operation to read operation to read judgement data. If the data is "1", the cells operate correctly. If the data is "0", they operate incorrectly. Repeating write/read operations 524,288 (512K) times checks 4M-bit of the memory.

3. How to exit from test mode

To exit the test mode, execute the test mode reset cycle.

Test Mode Set/Reset Cycle Timing Chart

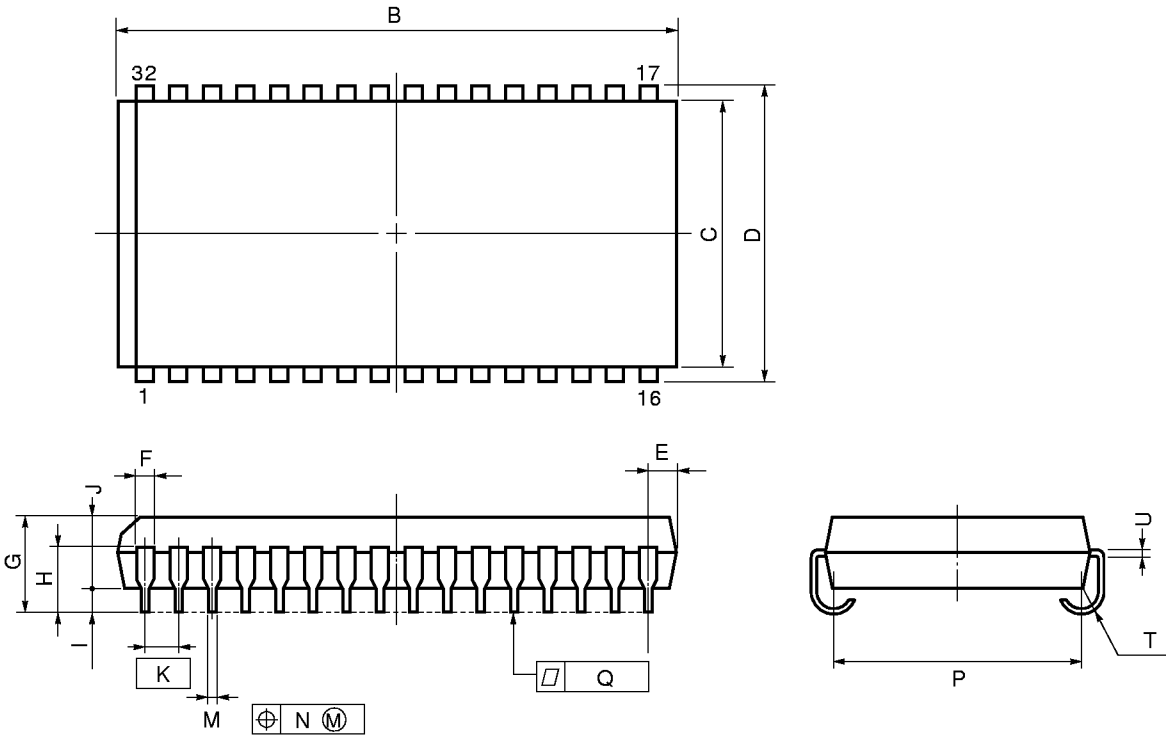


Test Mode Set/Reset Cycle

Parameter	Symbol	μPD434001LE-20		μPD434001LE-25		Unit
		MIN.	MAX.	MIN.	MAX.	
Test mode set time	t_{ST}	30		30		ns
Test mode reset time	t_{RT}	30		30		ns

Package Drawing

32 PIN PLASTIC SOJ (400 mil)



P32LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD434001.

TYPE OF SURFACE MOUNT DEVICE

μPD434001LE: 32-pin plastic SOJ (400 mil)