NEC

MOS INTEGRATED CIRCUIT
μPD434008A

4M-BIT CMOS FAST SRAM
512K-WORD BY 8-BIT

Description

The μPD434008A is a high speed, low power, 4,194,304 bits (524,288 words by 8 bits) CMOS static RAM.

Operating supply voltage is 5.0 V ± 0.5 V.

The μPD434008A is packaged in 36-pin plastic SOJ.

Features

• 524,288 words by 8 bits organization

• Fast access time : 12, 15, 17, 20 ns (MAX.)

• Output Enable input for easy application

• Single +5.0 V power supply

★ ### Ordering Information

Part number	Package	Access time (MAX.)	Supply current (MAX.)	
			At operating	At standby
μPD434008ALE-12	36-pin plastic SOJ (400 mil)	12 ns	200 mA	10 mA
μPD434008ALE-15		15 ns	170 mA	
μPD434008ALE-17		17 ns	160 mA	
μPD434008ALE-20		20 ns	150 mA	

The information in this document is subject to change without notice.

The mark ★ shows major revised points.

Pin Configuration (Marking Side)

/xxx indicates active low signal.

36-pin plastic SOJ (400 mil)

[µPD434008ALE]

Left pin		Right pin
A0	1	36 NC
A1	2	35 A18
A2	3	34 A17
A3	4	33 A16
A4	5	32 A15
/CS	6	31 /OE
I/O1	7	30 I/O8
I/O2	8	29 I/O7
Vcc	9	28 GND
GND	10	27 Vcc
I/O3	11	26 I/O6
I/O4	12	25 I/O5
/WE	13	24 A14
A5	14	23 A13
A6	15	22 A12
A7	16	21 A11
A8	17	20 A10
A9	18	19 NC
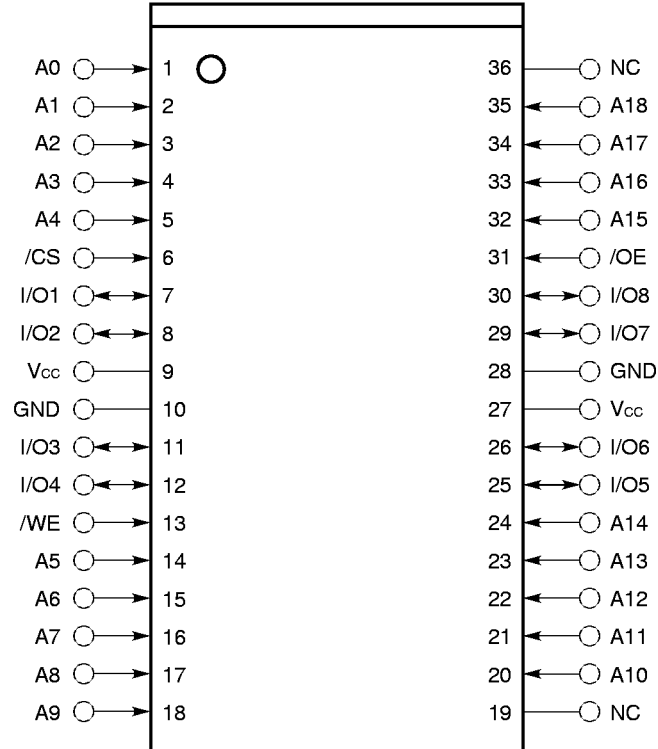
A0 - A18	:	Address Inputs
I/O1 - I/O8	:	Data Inputs / Outputs
/CS	:	Chip Select
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

Block Diagram

Truth Table

/CS	/OE	/WE	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
L	L	H	Read	D_{OUT}	I_{CC}
L	×	L	Write	D_{IN}	
L	H	H	Output disable	High impedance	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		-0.5 [Note] to $+7.0$	V
Input / Output voltage	V_T		-0.5 [Note] to $V_{CC}+0.5$	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to $+125$	°C

Note -2.0 V (MIN.) (pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.2		$V_{CC}+0.5$	V
Low level input voltage	V_{IL}		-0.5 [Note]		$+0.8$	V
Operating ambient temperature	T_A		0		70	°C

Note -2.0 V (MIN.) (pulse width : 2 ns)

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DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–2		+2	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		–2		+2	μA
Operating supply current	I_{CC}	/CS = V_{IL}, $I_{I/O}$ = 0 mA, Minimum cycle time	Cycle time : 12 ns			200	mA
			Cycle time : 15 ns			170	
			Cycle time : 17 ns			160	
			Cycle time : 20 ns			150	
Standby supply current	I_{SB}	/CS = V_{IH}, V_{IN} = V_{IH} or V_{IL}				50	mA
	I_{SB1}	V_{CC} − 0.2 V ≤ /CS, V_{IN} ≤ 0.2 V or V_{CC} − 0.2 V ≤ V_{IN}				10	
High level output voltage	V_{OH}	I_{OH} = −4.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA				0.4	V

Remark V_{IN} : Input voltage

Capacitance (T$_A$ = 25 °C, f = 1 MHz)

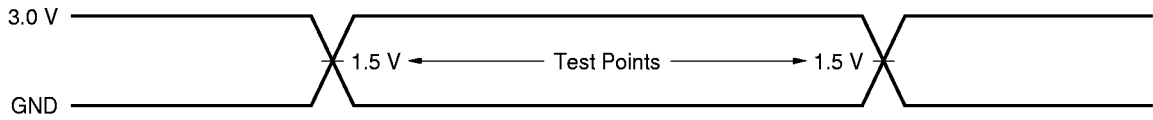| Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

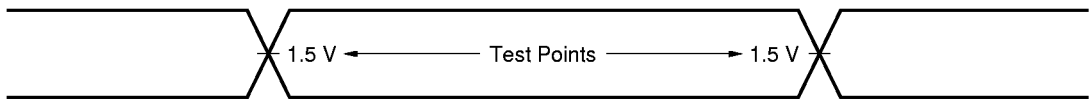**2.** These parameters are periodically sampled and not 100% tested.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)

```
3.0 V ──────────┐         ┌──────────────────────────────┐         ┌──────────
                 \       /                                  \       /
                  X─ 1.5 V ◄──────── Test Points ────────► 1.5 V ─X
                 /       \                                  /       \
GND  ───────────┘         └──────────────────────────────┘         └──────────
```

Output Waveform

```
    ────────────┐         ┌──────────────────────────────┐         ┌──────────
                 \       /                                  \       /
                  X─ 1.5 V ◄──────── Test Points ────────► 1.5 V ─X
                 /       \                                  /       \
    ────────────┘         └──────────────────────────────┘         └──────────
```

Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.

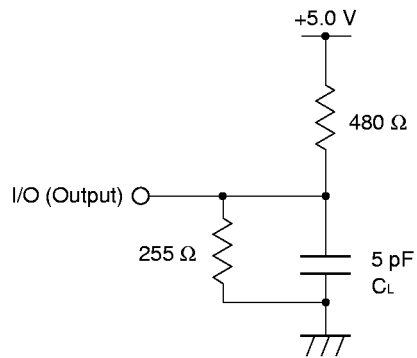| **Figure 1**	**Figure 2**
(for t_{AA}, t_{ACS}, t_{OE}, t_{OH})	(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW})
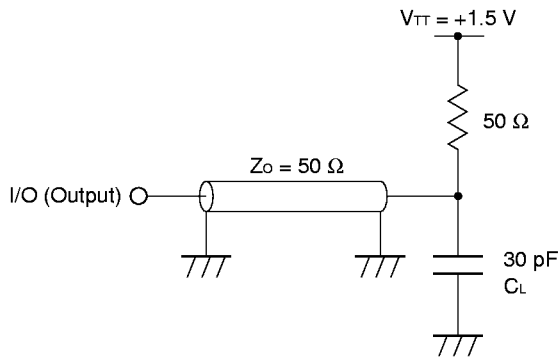
Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

Parameter	Symbol	-12		-15		-17		-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	12		15		17		20		ns	
Address access time	t_{AA}		12		15		17		20	ns	1
/CS access time	t_{ACS}		12		15		17		20	ns	
/OE access time	t_{OE}		6		7		8		10	ns	
Output hold from address change	t_{OH}	3		3		3		3		ns	
/CS to output in low impedance	t_{CLZ}	3		3		3		3		ns	2, 3
/OE to output in low impedance	t_{OLZ}	0		0		0		0		ns	
/CS to output in high impedance	t_{CHZ}		6		7		8		8	ns	
/OE to output hold in high impedance	t_{OHZ}		6		7		8		8	ns	

Notes 1. See the output load shown in **Figure 1**.

   2. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

   3. These parameters are periodically sampled and not 100% tested.

Read Cycle Timing Chart 1 (Address Access)
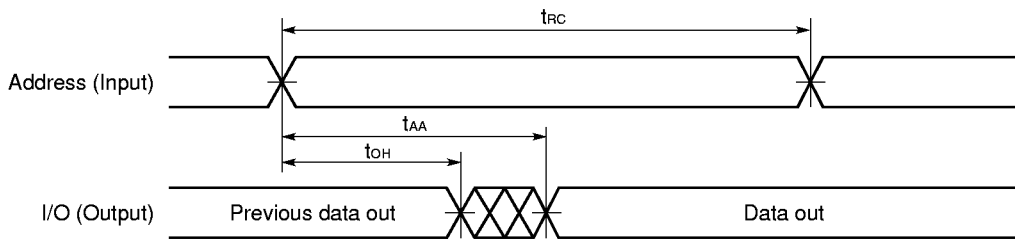
Remarks 1. In read cycle, /WE should be fixed to high level.

   2. /CS = /OE = V_{IL}

Read Cycle Timing Chart 2 (/CS Access)
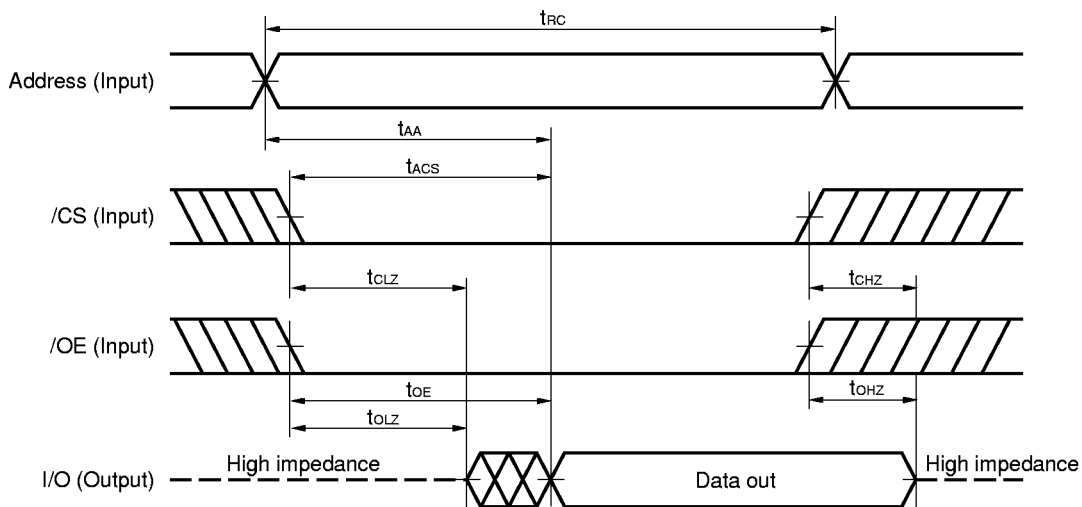
**Caution**   Address valid prior to or coincident with /CS low level input.

Remark   In read cycle, /WE should be fixed to high level.

Write Cycle

Parameter	Symbol	-12		-15		-17		-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	12		15		17		20		ns	
/CS to end of write	t_{CW}	8		10		11		12		ns	
Address valid to end of write	t_{AW}	8		10		11		12		ns	
Write pulse width	t_{WP}	8		10		11		12		ns	
Data valid to end of write	t_{DW}	6		7		8		9		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write recovery time	t_{WR}	1		1		1		1		ns	
/WE to output in high impedance	t_{WHZ}		6		7		8		8	ns	1, 2
Output active from end of write	t_{OW}	3		3		3		3		ns	

Notes 1. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

   **2.** These parameters are periodically sampled and not 100% tested.

Write Cycle Timing Chart 1 (/WE Controlled)
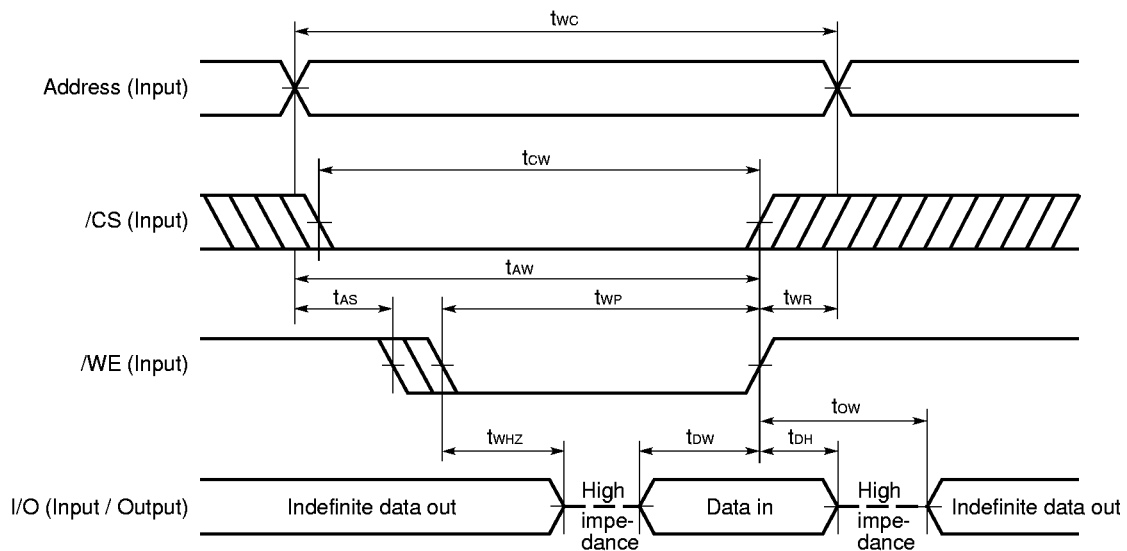
Caution   /CS or /WE should be fixed to high level during address transition.

Remarks 1. Write operation is done during the overlap time of a low level /CS and a low level /WE.

   2. During t_{WHZ}, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

   3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

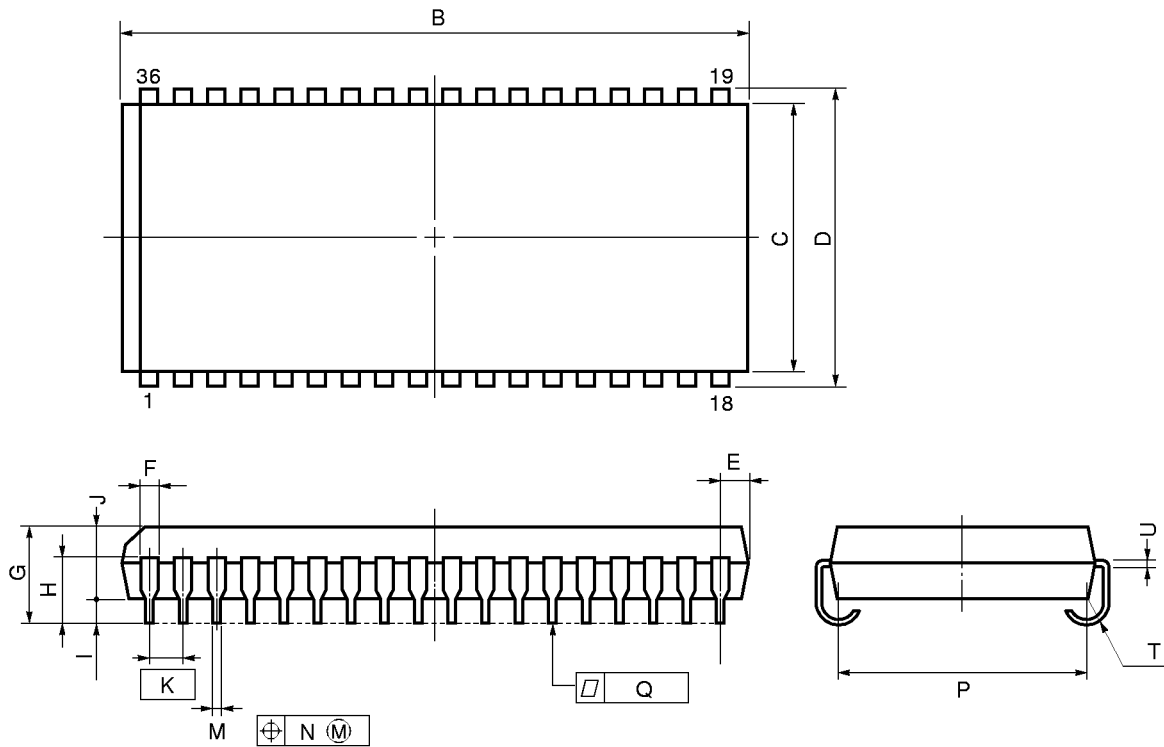**Write Cycle Timing Chart 2 (/CS Controlled)**
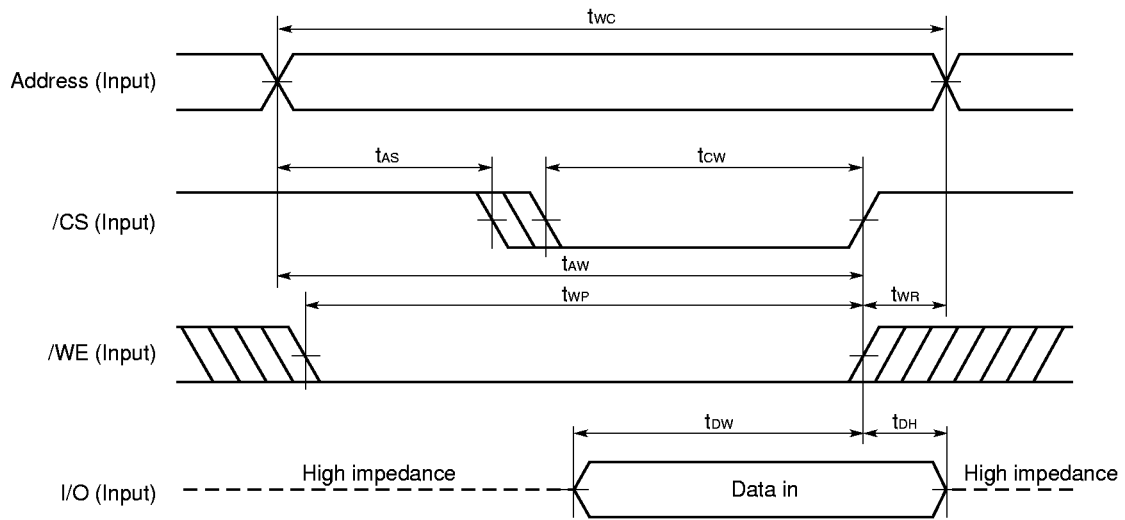
Caution /CS or /WE should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level /CS and a low level /WE.

Package Drawing

36 PIN PLASTIC SOJ (400 mil)

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P36LE-400A

ITEM	MILLIMETERS	INCHES
B	23.6±0.2	0.929±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD434008A.

Type of Surface Mount Device

μPD434008ALE : 36-pin plastic SOJ (400 mil)

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed imme-diately after power-on for devices having reset function.