

## Description

The μPD4361 is a 65,536-word by 1-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD4361 a high-speed device that requires very low power and no clock or refreshing.

The device is packaged in a 22-pin plastic DIP and 22-pin ceramic leadless chip carrier and has two types of access times, address and chip select. In addition, the μPD4361C-L features low-power data retention.

## Features

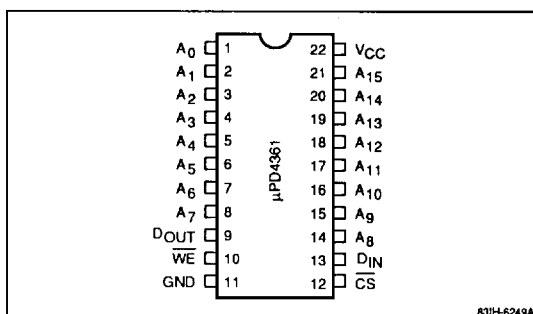
- 65, 536 x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Data retention current of 50 μA max available from -L versions only
- Standard 22-pin plastic DIP and ceramic LCC
- Standard JEDEC pin configurations

## Ordering Information

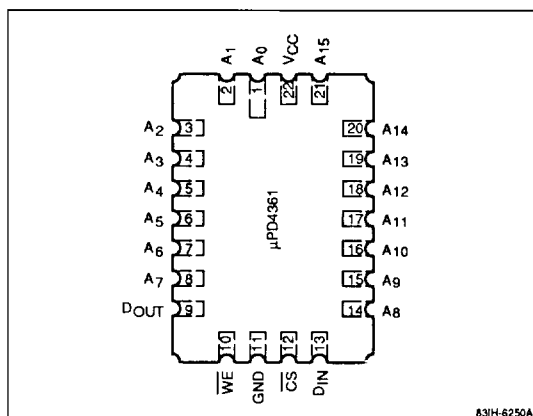
| Part Number  | Access Time (max) | Package            |
|--------------|-------------------|--------------------|
| μPD4361C-45  | 45 ns             | 22-pin plastic DIP |
| C-55         | 55 ns             |                    |
| C-70         | 70 ns             |                    |
| μPD4361C-45L | 45 ns             | 22-pin plastic DIP |
| C-55L        | 55 ns             |                    |
| C-70L        | 70 ns             |                    |
| μPD4361K-40  | 40 ns             | 22-pin ceramic LCC |
| K-45         | 45 ns             |                    |
| K-55         | 55 ns             |                    |

## Pin Configurations

### 22-Pin Plastic DIP



### 22-Pin Ceramic LCC



## Pin Identification

| Symbol                           | Function             |
|----------------------------------|----------------------|
| A <sub>0</sub> - A <sub>15</sub> | Address Inputs       |
| D <sub>IN</sub>                  | Data Input           |
| D <sub>OUT</sub>                 | Data output          |
| CS                               | Chip select          |
| WE                               | Write enable         |
| GND                              | Ground               |
| VCC                              | +5-volt power supply |

### Absolute Maximum Ratings

|                                           |                |
|-------------------------------------------|----------------|
| Supply voltage, $V_{CC}$                  | -0.5 to +7.0 V |
| Input voltage, $V_{IN}$ (Note 1)          | -0.5 to +7.0 V |
| Operating temperature, $T_{OPR}$ (Note 2) | 0 to +70°C     |
| Storage temperature, $T_{STG}$ (Note 3)   | -55 to +125°C  |
| Power dissipation, $P_D$                  | 1.0 W          |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

#### Notes:

- (1)  $V_{IN} = -3.0$  V minimum for 20 ns maximum pulse.
- (2)  $T_{OPR}$  for 4361K = -10 to +85°C.
- (3)  $T_{STG}$  for 4361K = -65 to +150°C.

### Truth Table

| Function     | $\overline{CS}$ | $\overline{WE}$ | Input/Output | $I_{CC}$ |
|--------------|-----------------|-----------------|--------------|----------|
| Not selected | H               | X               | High-Z       | Standby  |
| Read         | L               | H               | $D_{OUT}$    | Active   |
| Write        | L               | L               | High-Z       | Active   |

### Recommended Operating Conditions

| Parameter             | Symbol   | Min  | Typ | Max            | Unit |
|-----------------------|----------|------|-----|----------------|------|
| Supply voltage        | $V_{CC}$ | 4.5  | 5.0 | 5.5            | V    |
| Input voltage, high   | $V_{IH}$ | 2.2  |     | $V_{CC} + 0.5$ | V    |
| Input voltage, low    | $V_{IL}$ | -0.5 |     | 0.8            | V    |
| Operating temperature | $T_A$    | 0    |     | 70             | °C   |

#### Notes:

- (1)  $V_{IL} = -3.0$  V minimum for 20 ns maximum pulse.

### Capacitance

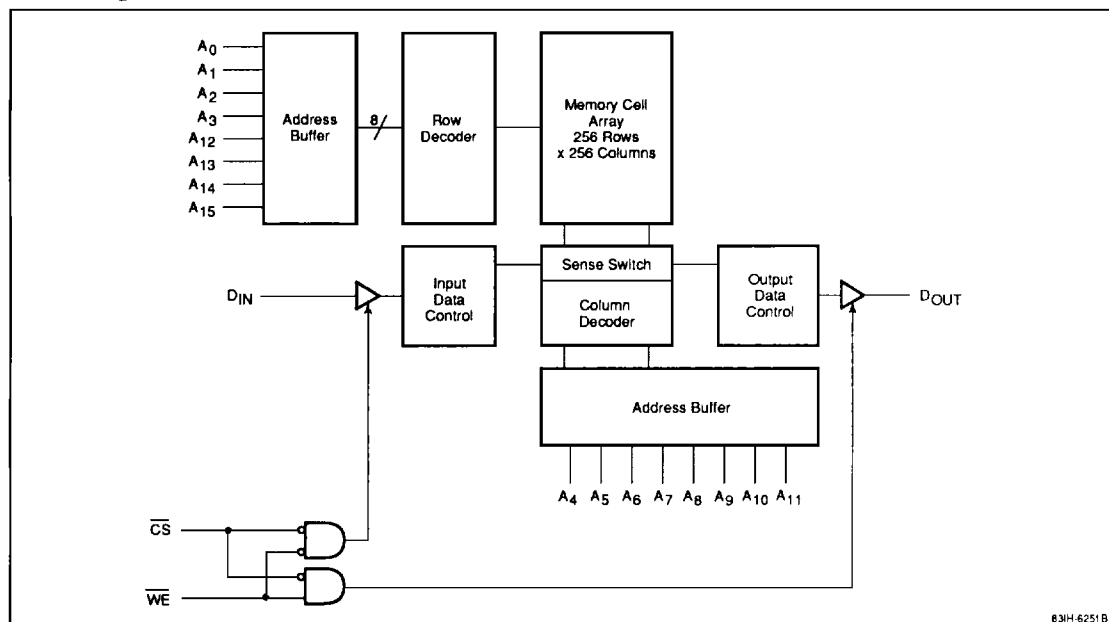
$T_A = 25^\circ\text{C}$ ;  $f = 1$  MHz;  $V_{IN}$  and  $V_{OUT} = 0$  V (Note 1)

| Parameter          | Symbol     | Min | Typ | Max | Unit |
|--------------------|------------|-----|-----|-----|------|
| Input capacitance  | $C_{IN}$   |     |     | 5   | pF   |
| Output capacitance | $C_{DOUT}$ |     |     | 7   | pF   |

#### Notes:

- (1) This parameter is sampled and not 100% tested.

### Block Diagram



831H-6251B

## DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$ ;  $V_{CC} = +5.0 \text{ V} \pm 10\%$

| Parameter                | Symbol    | Min | Typ | Max | Unit | Test Conditions                                                                                           |
|--------------------------|-----------|-----|-----|-----|------|-----------------------------------------------------------------------------------------------------------|
| Input leakage current    | $I_{LI}$  | -2  |     | 2   | μA   | $V_{IN} = 0 \text{ V to } V_{CC}$                                                                         |
| Output leakage current   | $I_{LO}$  | -2  |     | 2   | μA   | $V_{OUT} = 0 \text{ V to } V_{CC}$ ; $\overline{CS} = V_{IH}$                                             |
| Operating supply current | $I_{CC}$  |     |     | 120 | mA   | $\overline{CS} = V_{IL}$ ; $I_{DOUT} = 0 \text{ mA}$                                                      |
| Standby supply current   | $I_{SB}$  |     |     | 20  | mA   | $\overline{CS} = V_{IH}$                                                                                  |
|                          | $I_{SB1}$ |     |     | 2   | mA   | $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ ; $V_{IN} \leq 0.2 \text{ V or } \geq V_{CC} - 0.2 \text{ V}$ |
| Output voltage, low      | $V_{OL}$  |     |     | 0.4 | V    | $I_{OL} = 8.0 \text{ mA}$                                                                                 |
| Output voltage, high     | $V_{OH}$  | 2.4 |     |     | V    | $I_{OH} = -4.0 \text{ mA}$                                                                                |

## AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$ ;  $V_{CC} = +5.0 \text{ V} \pm 10\%$

| Parameter                         | Symbol           | μPD4361-40 |     | μPD4361-45 |     | μPD4361-55 |     | μPD4361-70 |     | Unit | Test Conditions |
|-----------------------------------|------------------|------------|-----|------------|-----|------------|-----|------------|-----|------|-----------------|
|                                   |                  | Min        | Max | Min        | Max | Min        | Max | Min        | Max |      |                 |
| Read Operation                    |                  |            |     |            |     |            |     |            |     |      |                 |
| Read cycle time                   | t <sub>RC</sub>  | 40         |     | 45         |     | 55         |     | 70         |     | ns   | (Note 2)        |
| Address access time               | t <sub>AA</sub>  |            | 40  |            | 45  |            | 55  |            | 70  | ns   |                 |
| Chip select access time           | t <sub>ACS</sub> |            | 40  |            | 45  |            | 55  |            | 70  | ns   |                 |
| Output hold from address change   | t <sub>OH</sub>  | 5          |     | 5          |     | 5          |     | 5          |     | ns   |                 |
| Chip select to output in low-Z    | t <sub>LZ</sub>  | 5          |     | 5          |     | 5          |     | 5          |     | ns   | (Note 3)        |
| Chip deselect to output in high-Z | t <sub>HZ</sub>  | 0          | 22  | 0          | 25  | 0          | 30  | 0          | 30  | ns   | (Note 4)        |
| Chip select to power-up time      | t <sub>PU</sub>  | 0          |     | 0          |     | 0          |     | 0          |     | ns   |                 |
| Chip deselect to power-down time  | t <sub>PD</sub>  | 0          | 27  | 0          | 30  | 0          | 40  | 0          | 40  | ns   |                 |
| Write Operation                   |                  |            |     |            |     |            |     |            |     |      |                 |
| Write cycle time                  | t <sub>WC</sub>  | 40         |     | 45         |     | 55         |     | 70         |     | ns   | (Note 2)        |
| Chip select to end of write       | t <sub>CW</sub>  | 37         |     | 40         |     | 50         |     | 60         |     | ns   |                 |
| Address valid to end of write     | t <sub>AW</sub>  | 37         |     | 40         |     | 50         |     | 60         |     | ns   |                 |
| Address setup time                | t <sub>AS</sub>  | 0          |     | 0          |     | 0          |     | 0          |     | ns   |                 |
| Write pulse width                 | t <sub>WP</sub>  | 23         |     | 25         |     | 30         |     | 40         |     | ns   |                 |
| Write recovery time               | t <sub>WR</sub>  | 0          |     | 0          |     | 0          |     | 0          |     | ns   |                 |
| Data valid to end of write        | t <sub>DW</sub>  | 23         |     | 25         |     | 25         |     | 30         |     | ns   |                 |
| Data hold time                    | t <sub>DH</sub>  | 0          |     | 0          |     | 0          |     | 0          |     | ns   |                 |
| Write enable to output in high-Z  | t <sub>WZ</sub>  | 0          | 22  | 0          | 25  | 0          | 25  | 0          | 30  | ns   | (Note 4)        |
| Output active from end of write   | t <sub>OW</sub>  | 0          |     | 0          |     | 0          |     | 0          |     | ns   | (Note 3)        |

### Notes:

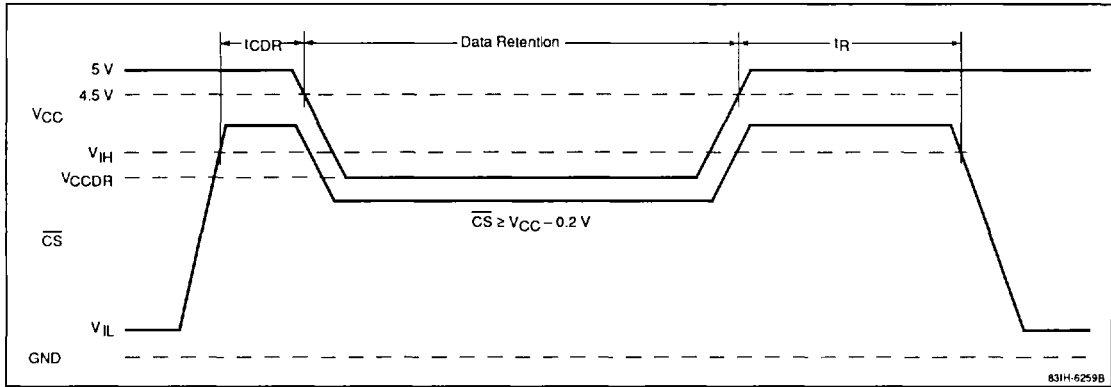
- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.
- (2) All read cycle timings are referenced from the last valid address to the first transitioning address.
- (3) Transition is measured at  $\pm 200 \text{ mV}$  from steady-state voltage with the loading shown in figure 2.
- (4) Transition is measured at  $V_{OL} + 200 \text{ mV}$  and  $V_{OH} - 200 \text{ mV}$  with the loading shown in figure 2.

Low V<sub>CC</sub> Data Retention Characteristics (for -L Version Only)

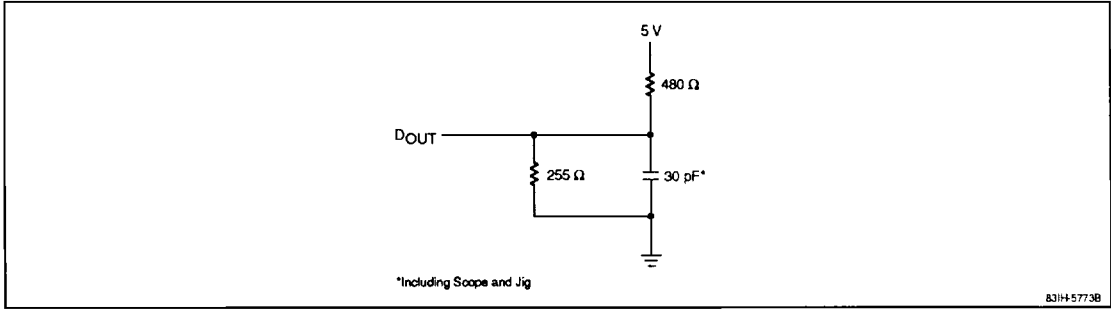
T<sub>A</sub> = 0 to 70°C

| Parameter                       | Symbol            | Min             | Typ | Max | Unit | Test Conditions                                                                                                                                      |
|---------------------------------|-------------------|-----------------|-----|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data retention supply voltage   | V <sub>CCDR</sub> | 2.0             |     | 5.5 | V    | $\overline{CS} \geq V_{CC} - 0.2\text{ V}; V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$                          |
| Data retention supply current   | I <sub>CCDR</sub> |                 | 1   | 50  | μA   | V <sub>CC</sub> = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2\text{ V}; V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$ |
| Chip deselect to data retention | t <sub>CDR</sub>  | 0               |     |     | ns   |                                                                                                                                                      |
| Operation recovery time         | t <sub>R</sub>    | t <sub>RC</sub> |     |     | ns   |                                                                                                                                                      |

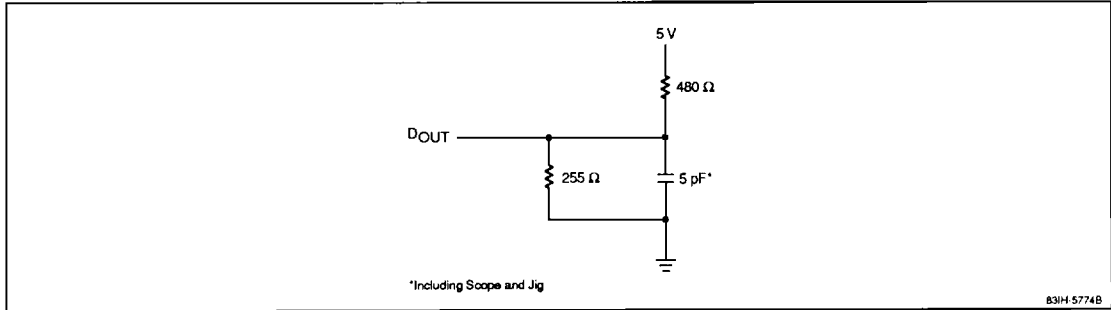
Data Retention Timing



**Figure 1. Output Load**

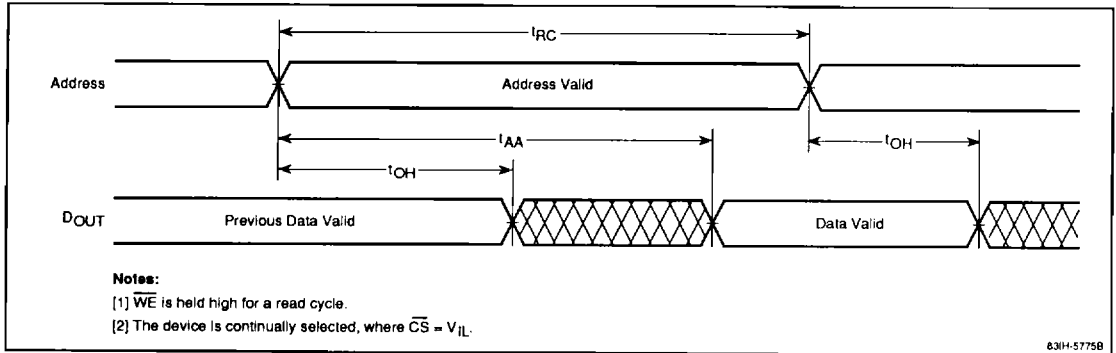


**Figure 2. Output Load for  $t_{HZ}$ ,  $t_{LZ}$ ,  $t_{WZ}$ , and  $t_{OW}$**

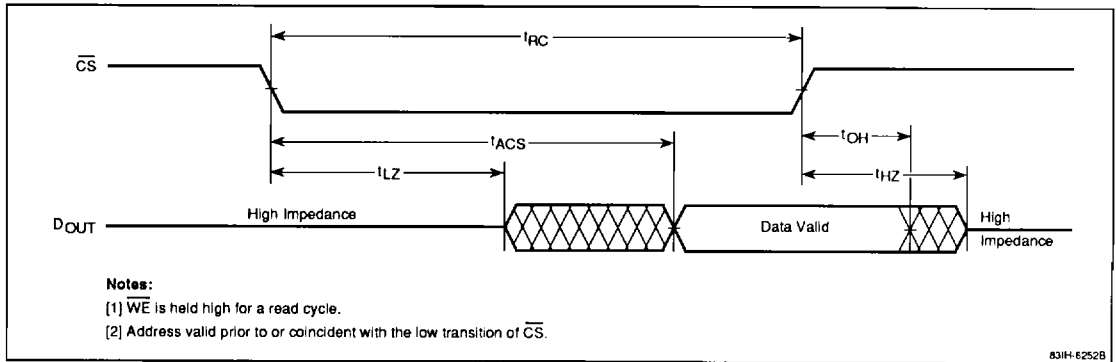


## Timing Waveforms

### Address Access Cycle

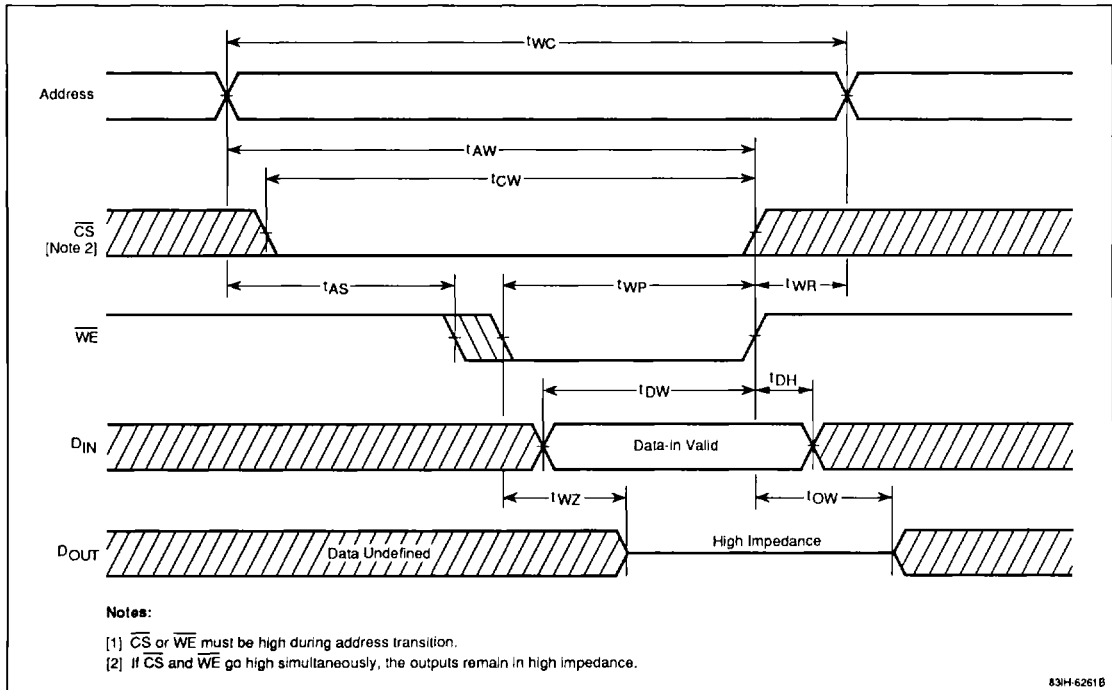


### Chip Select Access Cycle



## Timing Waveforms (cont)

### ***WE-Controlled Write Cycle***



**Timing Waveforms (cont)**

***$\overline{CS}$ -Controlled Write Cycle***

