

**NEC****MOS INTEGRATED CIRCUIT**  
 **$\mu$ PD44323362****32M-BIT CMOS SYNCHRONOUS FAST STATIC RAM**  
**1M-WORD BY 36-BIT**  
**HSTL INTERFACE / REGISTER-REGISTER / LATE WRITE****Description**

The  $\mu$ PD44323362 is a 1,048,576 words by 36 bits synchronous static RAM fabricated with advanced CMOS technology using Full-CMOS six-transistor memory cell.

The  $\mu$ PD44323362 is suitable for applications which require high-speed, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

The  $\mu$ PD44323362 is packaged in a 119-pin PLASTIC BGA (Ball Grid Array).

**Features**

- Fully synchronous operation
- HSTL Input / Output levels
- Fast clock access time: 2.0 ns / 250 MHz
- Asynchronous output enable control: /G
- Byte write control: /SBa (DQa1 to DQa9), /SBb (DQb1 to DQb9), /SBc (DQc1 to DQc9), /SBd (DQd1 to DQd9)
- Common I/O using three-state outputs
- Internally self-timed write cycle
- Late write with 1 dead cycle between Read-Write
- User-configurable outputs: Controlled impedance outputs or push-pull outputs
- Boundary scan (JTAG) IEEE 1149.1 compatible
- $2.5 \pm 0.125$  V (Chip) / 1.4 to 1.9 V (I/O) supply
- 119 bump BGA package, 1.27 mm pitch, 14 mm  $\times$  22 mm
- Sleep mode: ZZ (Enables sleep mode, active high)

**★ Ordering Information**

Part number	Access time	Clock frequency	Package
$\mu$ PD44323362F1-C40-FJ1	2.0 ns	250 MHz	119-pin PLASTIC BGA

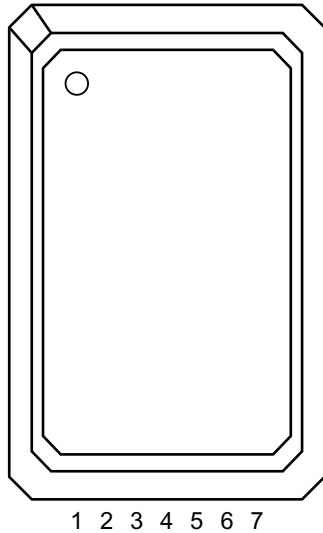
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Pin Configuration

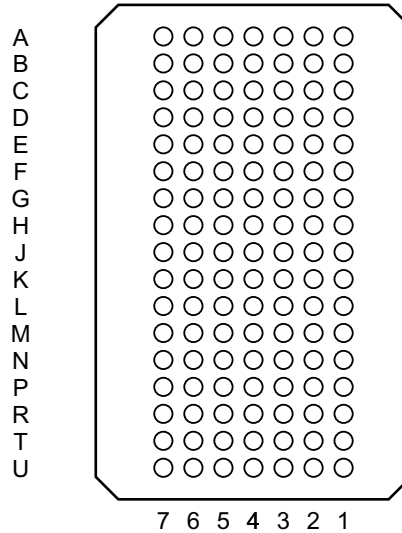
/xxx indicates active low signal.

119-pin plastic BGA

Top View



Bottom View



1	2	3	4	5	6	7
V <sub>DDQ</sub>	SA12	SA9	NC	SA5	SA2	V <sub>DDQ</sub>
NC	SA18	SA16	SA19	SA15	SA17	NC
NC	SA13	SA10	V <sub>DD</sub>	SA6	SA3	NC
DQc8	DQc9	V <sub>SS</sub>	ZQ	V <sub>SS</sub>	DQb9	DQb8
DQc6	DQc7	V <sub>SS</sub>	/SS	V <sub>SS</sub>	DQb7	DQb6
V <sub>DDQ</sub>	DQc5	V <sub>SS</sub>	/G	V <sub>SS</sub>	DQb5	V <sub>DDQ</sub>
DQc3	DQc4	/SBc	NC	/SBb	DQb4	DQb3
DQc1	DQc2	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQb2	DQb1
V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
DQd1	DQd2	V <sub>SS</sub>	K	V <sub>SS</sub>	DQa2	DQa1
DQd3	DQd4	/SBd	/K	/SBa	DQa4	DQa3
V <sub>DDQ</sub>	DQd5	V <sub>SS</sub>	/SW	V <sub>SS</sub>	DQa5	V <sub>DDQ</sub>
DQd6	DQd7	V <sub>SS</sub>	SA0	V <sub>SS</sub>	DQa7	DQa6
DQd8	DQd9	V <sub>SS</sub>	SA1	V <sub>SS</sub>	DQa9	DQa8
NC	SA14	M1	V <sub>DD</sub>	M2	SA4	NC
NC	NC	SA11	SA8	SA7	NC	ZZ
V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

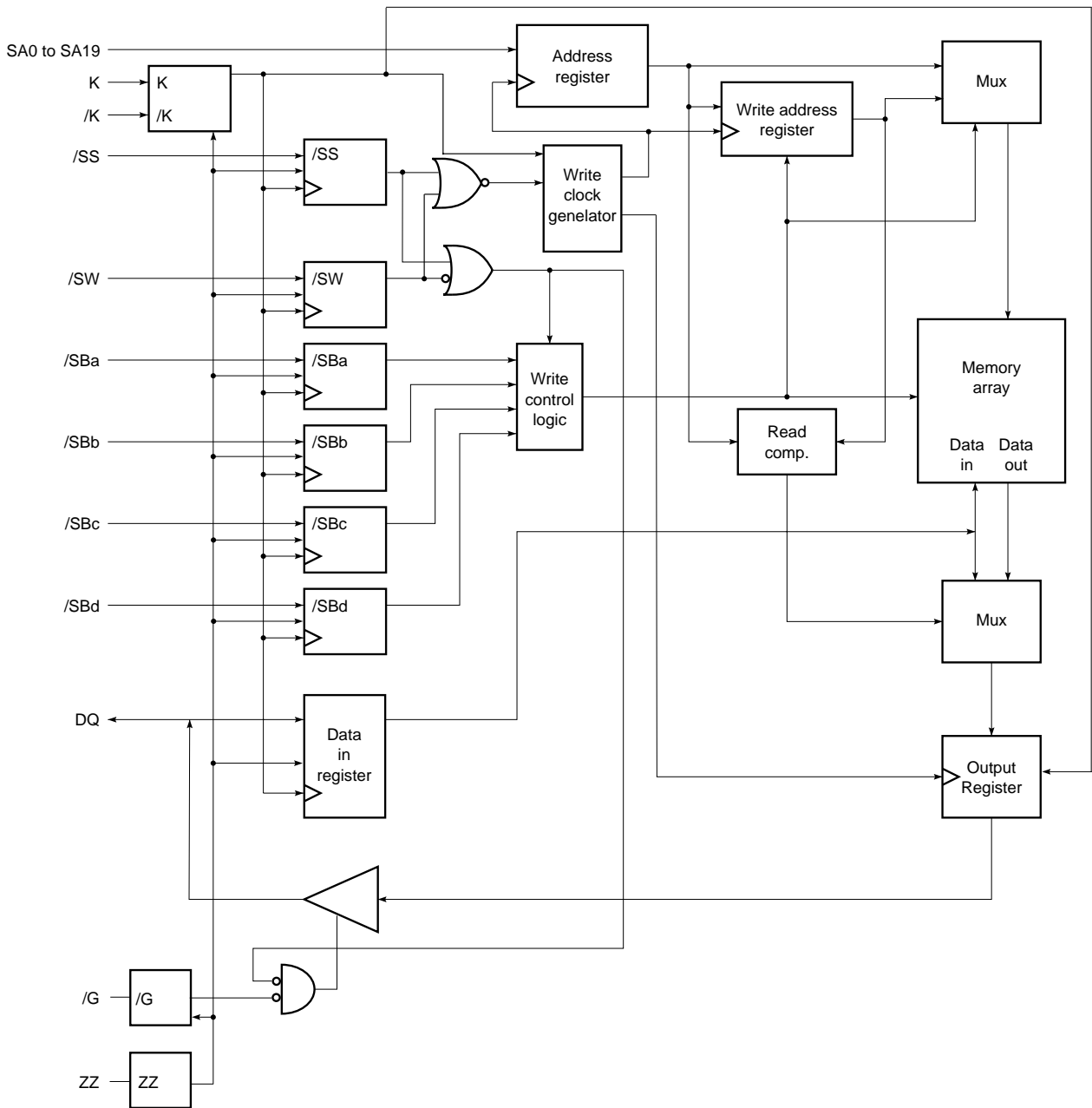
	7	6	5	4	3	2	1
A	V <sub>DDQ</sub>	SA2	SA5	NC	SA9	SA12	V <sub>DDQ</sub>
B	NC	SA17	SA15	SA19	SA16	SA18	NC
C	NC	SA3	SA6	V <sub>DD</sub>	SA10	SA13	NC
D	DQb8	DQb9	V <sub>SS</sub>	ZQ	V <sub>SS</sub>	DQc9	DQc8
E	DQb6	DQb7	V <sub>SS</sub>	/SS	V <sub>SS</sub>	DQc7	DQc6
F	V <sub>DDQ</sub>	DQb5	V <sub>SS</sub>	/G	V <sub>SS</sub>	DQc5	V <sub>DDQ</sub>
G	DQb3	DQb4	/SBb	NC	/SBc	DQc4	DQc3
H	DQb1	DQb2	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQc2	DQc1
J	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQa1	DQa2	V <sub>SS</sub>	K	V <sub>SS</sub>	DQd2	DQd1
L	DQa3	DQa4	/SBa	/K	/SBd	DQd4	DQd3
M	V <sub>DDQ</sub>	DQa5	V <sub>SS</sub>	/SW	V <sub>SS</sub>	DQd5	V <sub>DDQ</sub>
N	DQa6	DQa7	V <sub>SS</sub>	SA0	V <sub>SS</sub>	DQd7	DQd6
P	DQa8	DQa9	V <sub>SS</sub>	SA1	V <sub>SS</sub>	DQd9	DQd8
R	NC	SA4	M2	V <sub>DD</sub>	M1	SA14	NC
T	ZZ	NC	SA7	SA8	SA11	NC	NC
U	V <sub>DDQ</sub>	NC	TDO	TCK	TDI	TMS	V <sub>DDQ</sub>

**Pin Name and Functions**

Pin name	Description	Function
V <sub>DD</sub>	Core Power Supply	Supplies power for RAM core
V <sub>SS</sub>	Ground	
V <sub>DDQ</sub>	Output Power Supply	Supplies power for output buffers
V <sub>REF</sub>	Input Reference	
K, /K	Main Clock	
SA0 to SA19	Synchronous Address Input	
DQa1 to DQd9	Synchronous Data Input / Output	
/SS	Synchronous Chip Select	Logically selects SRAM
/SW	Synchronous Byte Write Enable	Write command
/SBa	Synchronous Byte "a" Write Enable	Write DQa1 to DQa9
/SBb	Synchronous Byte "b" Write Enable	Write DQb1 to DQb9
/SBc	Synchronous Byte "c" Write Enable	Write DQc1 to DQc9
/SBd	Synchronous Byte "d" Write Enable	Write DQd1 to DQd9
/G	Asynchronous Output Enable	Asynchronous input
ZZ	Asynchronous Sleep Mode	Enables sleep mode, active high
ZQ	Output Impedance Control	
M1, M2	Mode Select	Selects operation mode <sup>Note</sup>
NC	No Connection	
TMS	Test Mode Select (JTAG)	
TDI	Test Data Input (JTAG)	
TCK	Test Clock Input (JTAG)	
TDO	Test Data Output (JTAG)	

**Note** This device only supports Single Differential Clock, R/R Mode.  
 (R/R stands for Registered Input / Registered Output.)

Late Write Block Diagram



**Programmable Impedance / Power Up Requirements**

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V<sub>SS</sub> to allow for the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 175 ohm and 350 ohm. Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. The impedance update of the output driver occurs only when the SRAM is in high impedance. Write and Deselect operations will synchronously switch the SRAM into and out of high impedance, therefore, triggering an update. Power up requirements for the SRAM are that V<sub>DD</sub> must be powered before or simultaneously with V<sub>DDQ</sub> followed by V<sub>REF</sub>; inputs should be powered last. The limitation on V<sub>DDQ</sub> is that it must not exceed V<sub>DD</sub> during power up. In order to guarantee the optimum internally regulated supply voltage, the SRAM requires 4096 clock cycles of power-up time after V<sub>DD</sub> reaches its operating range. And CID impedance is not updated during the clock stopped.

**Sleep Mode**

Sleep Mode is enabled by switching asynchronous signal ZZ High. When the SRAM is in Sleep Mode, the output will go to a high impedance state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t<sub>ZZR</sub>) is required before the SRAM resumes normal operation. And CID impedance is not updated during the sleep mode.

**Synchronous Truth Table**

ZZ	/SS	/SW	/SBa	/SBb	/SBc	/SBd	Mode	DQa1 to DQa9	DQb1 to DQb9	DQc1 to DQc9	DQd1 to DQd9	Power
L	H	x	x	x	x	x	Not selected	High-Z	High-Z	High-Z	High-Z	Active
L	L	H	x	x	x	x	Read	Dout	Dout	Dout	Dout	Active
L	L	L	L	L	L	L	Write	Din	Din	Din	Din	Active
L	L	L	L	H	H	H	Write	Din	High-Z	High-Z	High-Z	Active
L	L	L	H	L	L	L	Write	High-Z	Din	Din	Din	Active
H	x	x	x	x	x	x	Sleep Mode	High-Z	High-Z	High-Z	High-Z	Standby

**Remark** x : Don't care

**Output Enable Truth Table**

Mode	/G	DQ
Read	L	Dout
Read	H	High-Z
Sleep (ZZ = H)	x	High-Z
Write (/SW = L)	x	High-Z
Deselect (/SS = H)	x	High-Z

**Mode Select (I/O)** <sup>Note 1</sup>

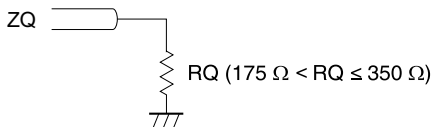
M1	M2	Mode
V <sub>SS</sub>	V <sub>DD</sub>	Single Differential Clock (K, /K), R/R Mode <sup>Note 2</sup>

- Notes**
1. This device only supports Single Differential Clock, R/R Mode. Mode Select Pins (M1, M2) are to be tied to either V<sub>DD</sub> or V<sub>SS</sub>.
  2. R/R: Registered Input / Registered Output

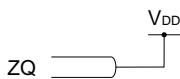
**Mode Select (Output Buffer)**

ZQ	Mode	Note
IZQ × RQ	Controlled impedance push-pull output buffer mode	1
V <sub>DD</sub>	Push-pull output buffer mode	2

**Notes** 1. See figure.



2. See figure.



**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V <sub>DD</sub>		-0.5		+3.0	V	1
Output supply voltage	V <sub>DDQ</sub>		-0.5		+3.0	V	1
Input voltage	V <sub>IN</sub>		-0.5		V <sub>DD</sub> + 0.3 (3.0 V MAX)	V	1
Input / Output voltage	V <sub>I/O</sub>		-0.5		V <sub>DD</sub> + 0.3 (3.0 V MAX)	V	1
Junction temperature	T <sub>j</sub>		5		110	°C	
Storage temperature	T <sub>stg</sub>		-55		+125	°C	

**Note 1.** -1.0 V MIN. (Pulse width 10% T<sub>cyc</sub>)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions (T<sub>j</sub> = 5 to 110 °C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Core supply voltage	V <sub>DD</sub>		2.375	2.5	2.625	V
Output buffer supply voltage	V <sub>DDQ</sub>		1.4		1.9	V
Input reference voltage	V <sub>REF</sub>		0.68		0.95	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>		V <sub>REF</sub> - 0.1	V
High level input voltage	V <sub>IH</sub>		V <sub>REF</sub> + 0.1		V <sub>DDQ</sub> + 0.3	V

**Note** -1.0 V MIN. (Pulse width 10% T<sub>cyc</sub>)

**Recommended AC Operating Conditions (T<sub>j</sub> = 5 to 110 °C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input reference voltage	V <sub>REF (RMS)</sub>		-5%		+5%	V
Low level input voltage	V <sub>IL</sub>		-0.3		V <sub>REF</sub> - 0.2	V
High level input voltage	V <sub>IH</sub>		V <sub>REF</sub> + 0.2		V <sub>DDQ</sub> + 0.3	V

**Capacitance (T<sub>A</sub> <sup>Note</sup> = 25 °C, f = 1 MHz)**

Parameter <sup>Note</sup>	Symbol	Test conditions	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	6	pF
Input / Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V	7	pF
Clock input capacitance	C <sub>clk</sub>	V <sub>clk</sub> = 0 V	7	pF

**Note** T<sub>A</sub> = Operating ambient temperature

**Remark** These parameters are sampled and not 100% tested.

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>DD</sub>	-5		+5	μA
DQ leakage current	I <sub>LO</sub>	V <sub>I/O</sub> = 0 to V <sub>DDQ</sub> , /SS = V <sub>IH</sub> or /G = V <sub>IH</sub>	-5		+5	μA
Operating supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , /SS = V <sub>IL</sub> , ZZ = V <sub>IL</sub> , cycle = 250 MHz, IDQ = 0 mA			550	mA
Quiescent active power supply current	I <sub>CC2</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , /SS = V <sub>IL</sub> , ZZ = V <sub>IL</sub> , Cycle = 4 MHz, IDQ = 0 mA			250	mA
Sleep mode power supply current	I <sub>SBZZ</sub>	ZZ = V <sub>IH</sub> , All other inputs = V <sub>IH</sub> or V <sub>IL</sub> , Cycle = DC, IDQ = 0 mA			150	mA
Power supply standby current	I <sub>SBSS</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , /SS = V <sub>IH</sub> , ZZ = V <sub>IL</sub> , Cycle = 250 MHz, IDQ = 0 mA			300	mA

**Output Voltage on Controlled Impedance Push-Pull Output Buffer Mode (V<sub>ZQ</sub> = I<sub>ZQ</sub> × R<sub>Q</sub>)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = (V <sub>DDQ</sub> /2) / (R <sub>Q</sub> /5) ± 15% @V <sub>OL</sub> = V <sub>DDQ</sub> / 2 (175 Ω < R <sub>Q</sub> < 350 Ω)	V <sub>SS</sub>		V <sub>DDQ</sub> /2	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = (V <sub>DDQ</sub> /2) / (R <sub>Q</sub> /5) ± 15% @V <sub>OH</sub> = V <sub>DDQ</sub> / 2 (175 Ω < R <sub>Q</sub> < 350 Ω)	V <sub>DDQ</sub> /2		V <sub>DDQ</sub>	V

**Output Voltage on Push-Pull Output Buffer Mode (V<sub>ZQ</sub> = V<sub>DD</sub>)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = +4 mA	-		0.3	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	V <sub>DDQ</sub> - 0.3		-	V



AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

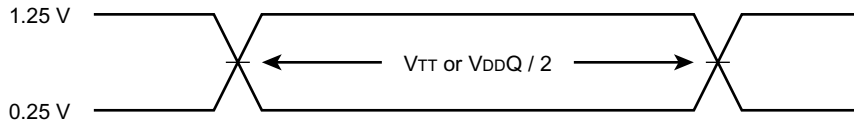
AC Characteristics Test Conditions ( $T_A^{Note} = 0$  to  $70$  °C,  $V_{DD} = 2.375$  to  $2.625$  V,  $V_{DDQ} = 1.5$  V)

Parameter	Symbol	Conditions	Unit
High level input voltage	$V_{IH}$	1.25	V
Low level input voltage	$V_{IL}$	0.25	V
Input reference voltage	$V_{REF}$	0.75	V
Input rise time	$T_R$	0.5	ns
Input fall time	$T_F$	0.5	ns
Input and output timing reference level		Cross point	

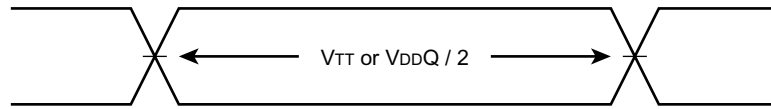
**Note**  $T_A$  = Operating ambient temperature

**Remark** Parameter tested with  $R_Q = 250$  Ω and  $V_{DDQ} = 1.5$  V.

Input waveform (rise and fall time = 0.5 ns (20 to 80%))



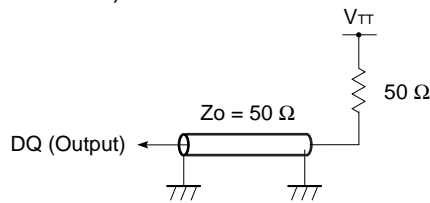
Output waveform



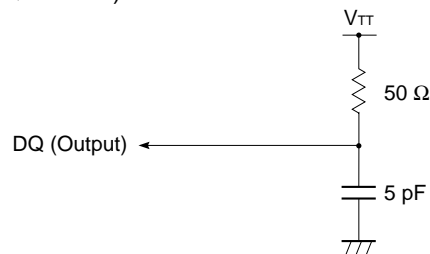
Read and Write Cycle

Parameter		Symbol	MIN.	MAX.	Unit	Note
Clock cycle time		$t_{KHKH}$	4.0	–	ns	
Clock phase time		$t_{KHKL} / t_{KLKH}$	1.5	–	ns	
Setup times	Address	$t_{AVKH}$	0.5	–	ns	
	Write data	$t_{DVKH}$				
	Write enable	$t_{WVKH}$				
	Chip select	$t_{SVKH}$				
Hold times	Address	$t_{KHAX}$	0.5	–	ns	
	Write data	$t_{KHDX}$				
	Write enable	$t_{KH WX}$				
	Chip select	$t_{KHSX}$				
Clock access time		$t_{KHQV}$	–	2.0	ns	1
K high to Q change		$t_{KHQX}$	0.5	–	ns	2
/G low to Q valid		$t_{GLQV}$	–	2.0	ns	1
/G low to Q change		$t_{GLQX}$	0.5	–	ns	2
/G high to Q High-Z		$t_{GHQZ}$	1.0	2.0	ns	2
K high to Q High-Z (/SW)		$t_{KHQZ}$	1.0	2.5	ns	2
K high to Q High-Z (/SS)		$t_{KHQZ2}$	1.0	2.5	ns	2
K high to Q Low-Z		$t_{KHQX2}$	0.7	–	ns	
/G high Pulse width		$t_{GHGL}$	4.0	–	ns	3
/G high to K high		$t_{GHKH}$	1.0	–	ns	3
K high to /G low		$t_{KHGL}$	2.5	–	ns	3
Sleep mode recovery		$t_{ZZR}$	2	–	Cycle	4
Sleep mode enable		$t_{ZZE}$	–	2	Cycle	4

Notes 1. See figure. ( $V_{TT} = 0.75\text{ V}$ ,  $R_Q = 250\ \Omega$ )



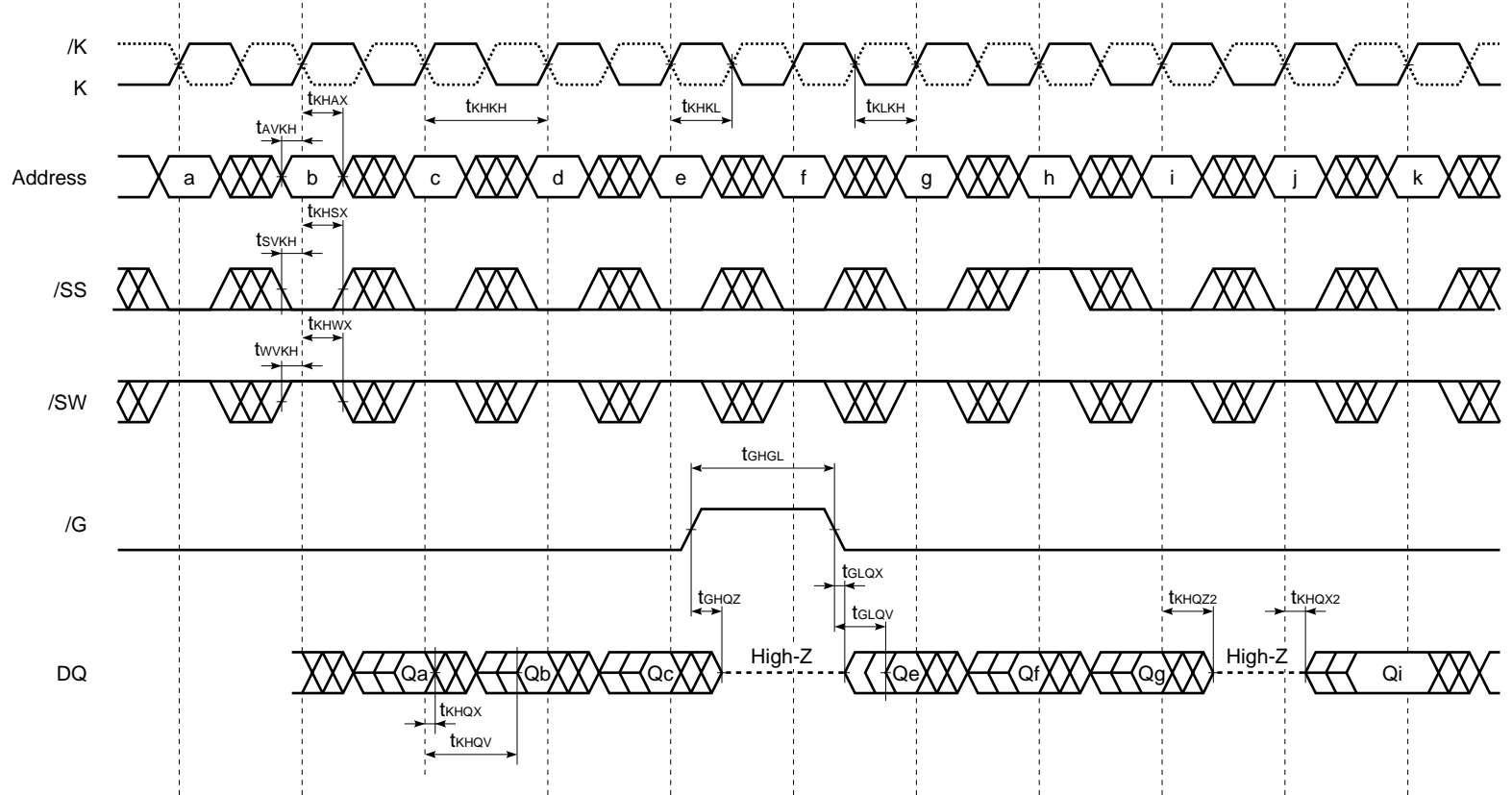
2. See figure. ( $V_{TT} = 0.75\text{ V}$ ,  $R_Q = 250\ \Omega$ )



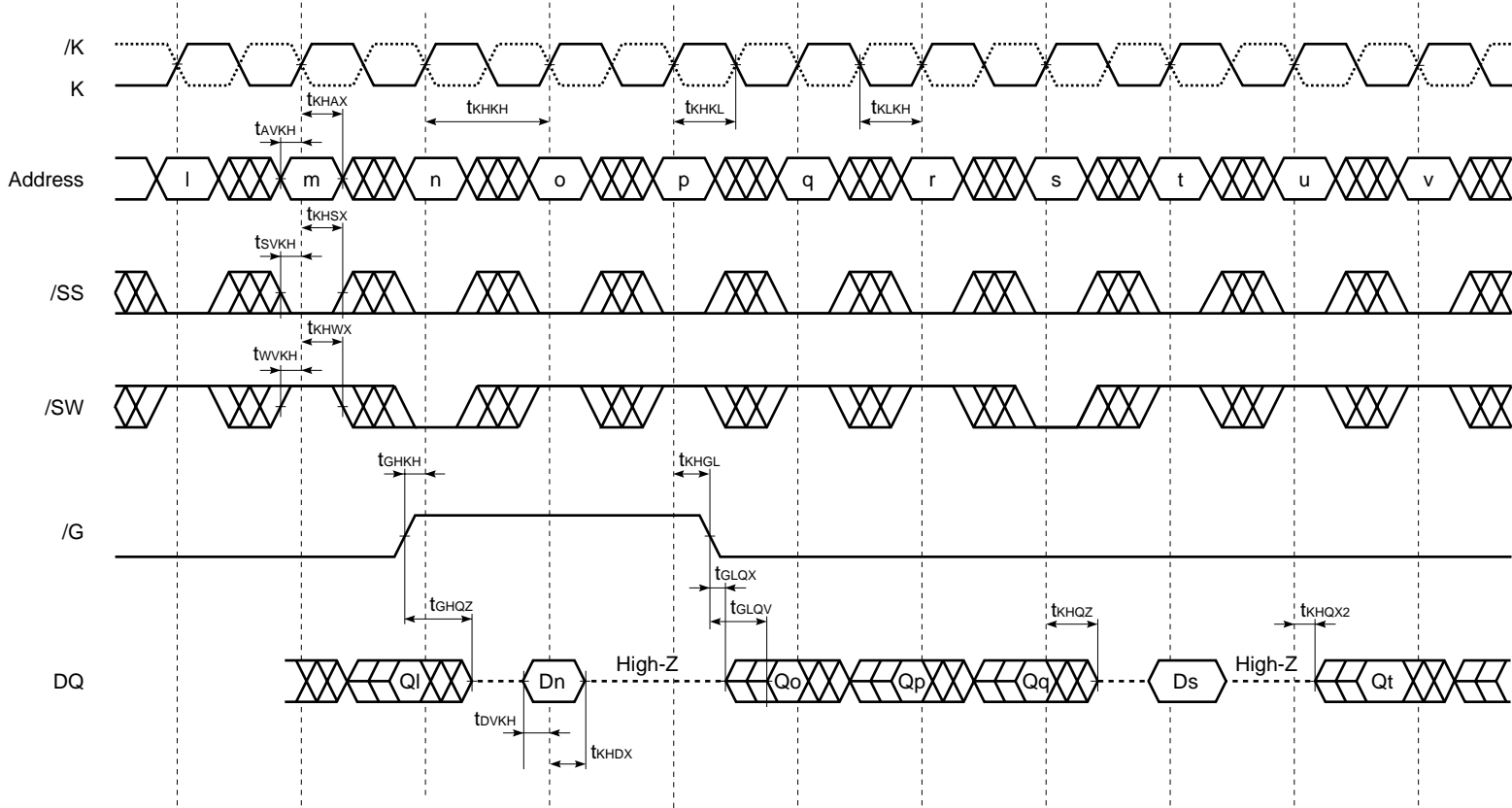
3. Controlled impedance push-pull output buffer mode only.

4. /SS must be 'high' before sleep mode entry.

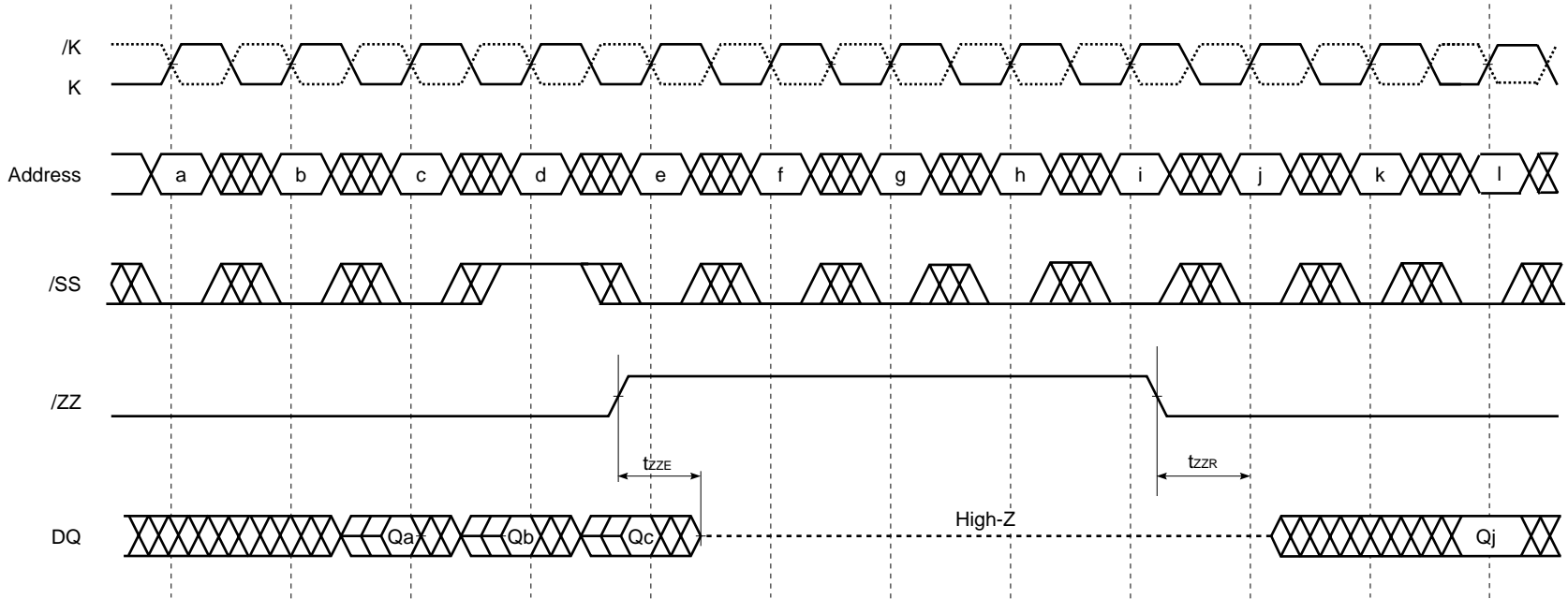
Read Operation



Write Operation



Sleep Mode



**JTAG Specifications**

The μPD44323362 supports a limited set of JTAG functions as in IEEE standard 1149.1.

**Test Access Port (TAP) Pins**

Pin name	Pin assignments	Description
TCK	4 U	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	2 U	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	3 U	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	5 U	Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

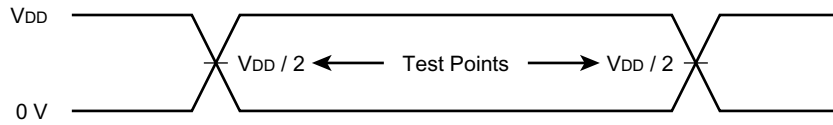
**Remark** The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

**JTAG DC Characteristics (T<sub>j</sub> = 5 to 110 °C)**

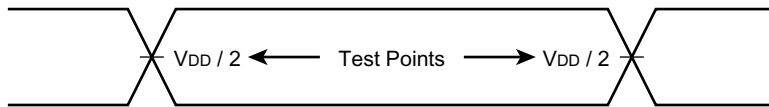
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG input high voltage	V <sub>IH</sub>		2.2		V <sub>DD</sub> + 0.3 (3.0 V MAX)	V	
JTAG input low voltage	V <sub>IL</sub>		-0.3		+0.5	V	
JTAG output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8 mA	2.4		-	V	
JTAG output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA	-		0.4	V	

JTAG AC Test Conditions ( $T_j = 5$  to  $110$  °C)

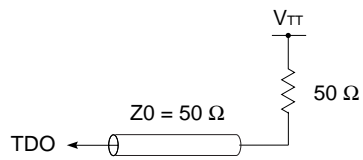
Input waveform (rise / fall time = 1 ns (20 to 80%))



Output waveform



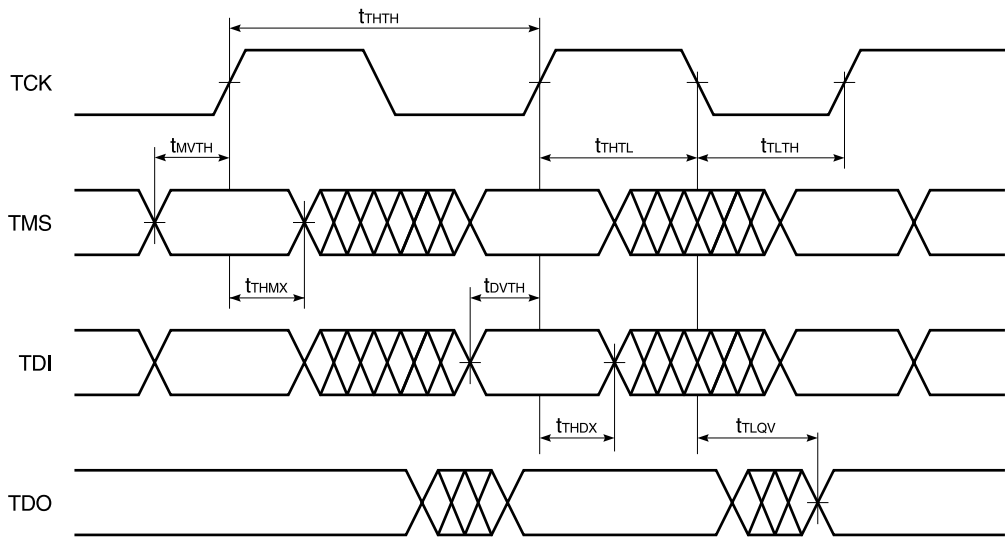
Output load ( $V_{TT} = 1.5$  V)



JTAG AC Characteristics (T<sub>j</sub> = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock cycle time (TCK)	t <sub>THTH</sub>		100		–	ns	
Clock phase time (TCK)	t <sub>THTL</sub> / t <sub>TLTH</sub>		40		–	ns	
Setup time (TMS / TDI)	t <sub>MVTH</sub> / t <sub>DVTH</sub>		10		–	ns	
Hold time (TMS / TDI)	t <sub>HMX</sub> / t <sub>HDX</sub>		10		–	ns	
TCK low to TDO valid (TDO)	t <sub>TLQV</sub>		–		20	ns	

JTAG Timing Diagram





**Scan Register Definition (1)**

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number

**Scan Register Definition (2)**

Register name	Bit size	Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	70	bit

**ID Register Definition**

ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
XXXX	0000 0000 0011 1100	00000010000	1

SCAN Exit Order

Bit no.	Signal name	Bump ID
1	M2	5R
2	SA1	4P
3	SA8	4T
4	SA4	6R
5	SA7	5T
6	ZZ	7T
7	DQa9	6P
8	DQa8	7P
9	DQa7	6N
10	DQa6	7N
11	DQa5	6M
12	DQa4	6L
13	DQa3	7L
14	DQa2	6K
15	DQa1	7K
16	/SBa	5L
17	/K	4L
18	K	4K
19	/G	4F
20	/SBb	5G
21	DQb1	7H
22	DQb2	6H
23	DQb3	7G
24	DQb4	6G
25	DQb5	6F
26	DQb6	7E
27	DQb7	6E
28	DQb8	7D
29	DQb9	6D
30	SA2	6A
31	SA3	6C
32	SA6	5C
33	SA5	5A
34	SA17	6B
35	SA15	5B

Bit no.	Signal name	Bump ID
36	SA16	3B
37	SA18	2B
38	SA9	3A
39	SA10	3C
40	SA13	2C
41	SA12	2A
42	DQc9	2D
43	DQc8	1D
44	DQc7	2E
45	DQc6	1E
46	DQc5	2F
47	DQc4	2G
48	DQc3	1G
49	DQc2	2H
50	DQc1	1H
51	/SBc	3G
52	ZQ	4D
53	/SS	4E
54	SA19	4B
55	NC	4H
56	/SW	4M
57	/SBd	3L
58	DQd1	1K
59	DQd2	2K
60	DQd3	1L
61	DQd4	2L
62	DQd5	2M
63	DQd6	1N
64	DQd7	2N
65	DQd8	1P
66	DQd9	2P
67	SA11	3T
68	SA14	2R
69	SA0	4N
70	M1	3R

**JTAG Instructions**

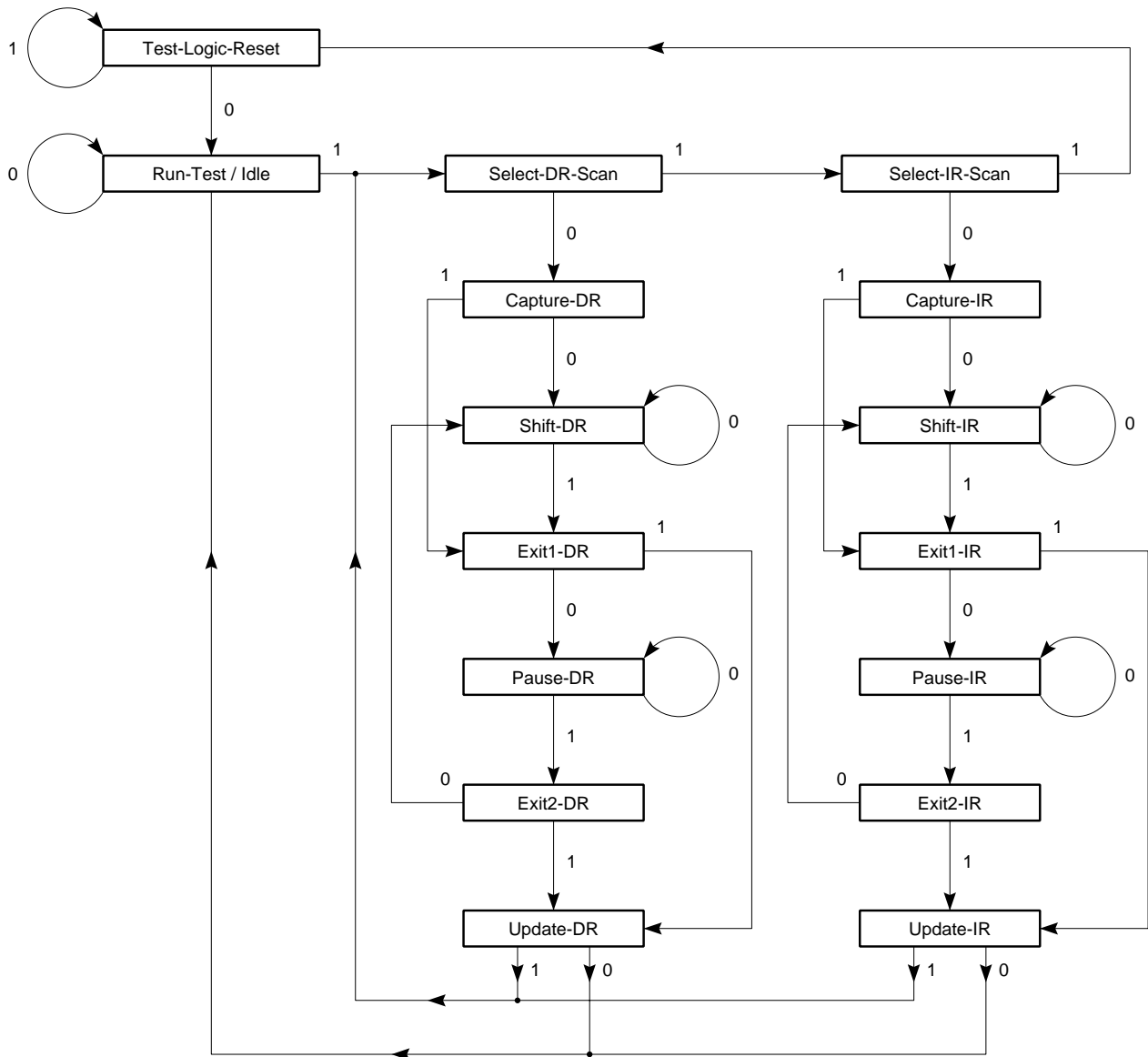
Instructions	Description
EXTEST	EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE instruction, except the RAM output are forced to high impedance any time the instruction is loaded.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE	Sample is a Standard 1149.1 mandatory public instruction. When the sample instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time ( $t_{CS}$ plus $t_{CH}$ ). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. This functionality is not Standard 1149.1 compliant.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

**JTAG Instruction Cording**

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	1
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

**Note 1.** TRISTATE all data drivers and CAPTURE the pad values into a SERIAL SCAN LATCH.

TAP Controller State Diagram



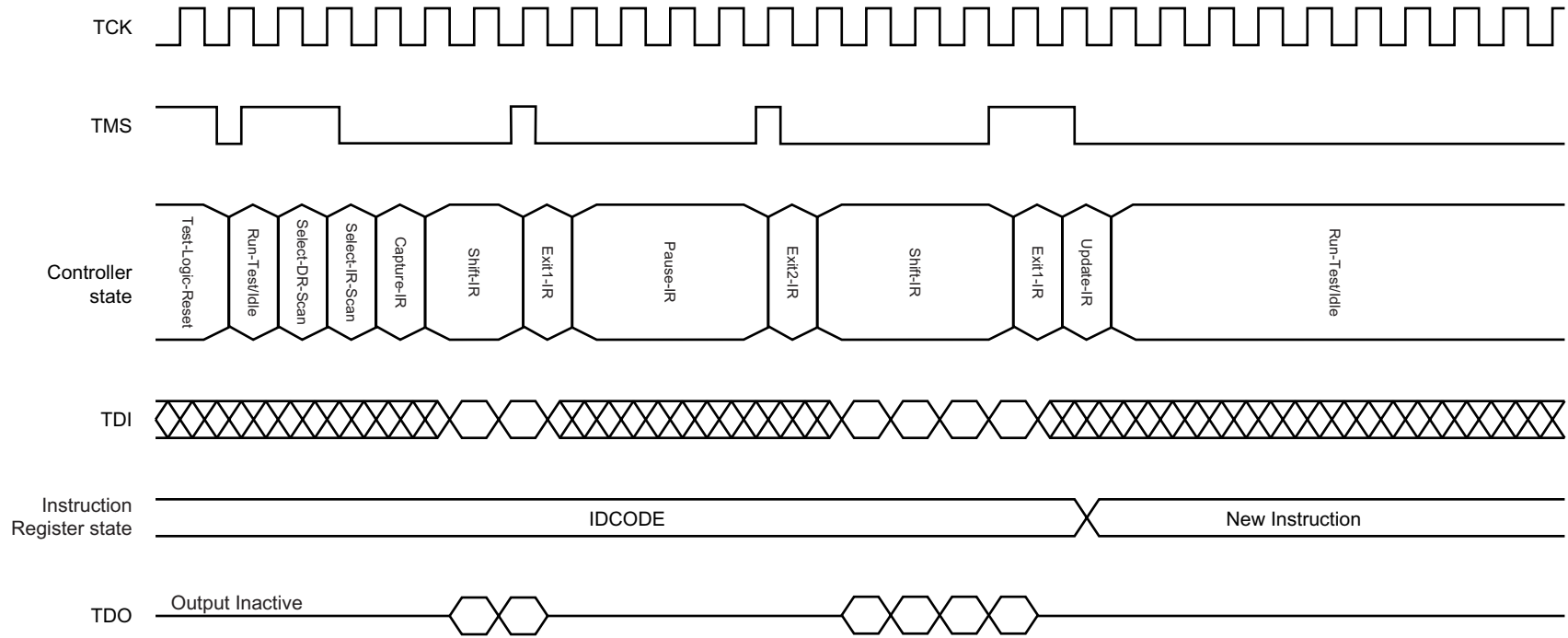
**Disabling The Test Access Port**

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V<sub>SS</sub> to preclude mid level inputs.

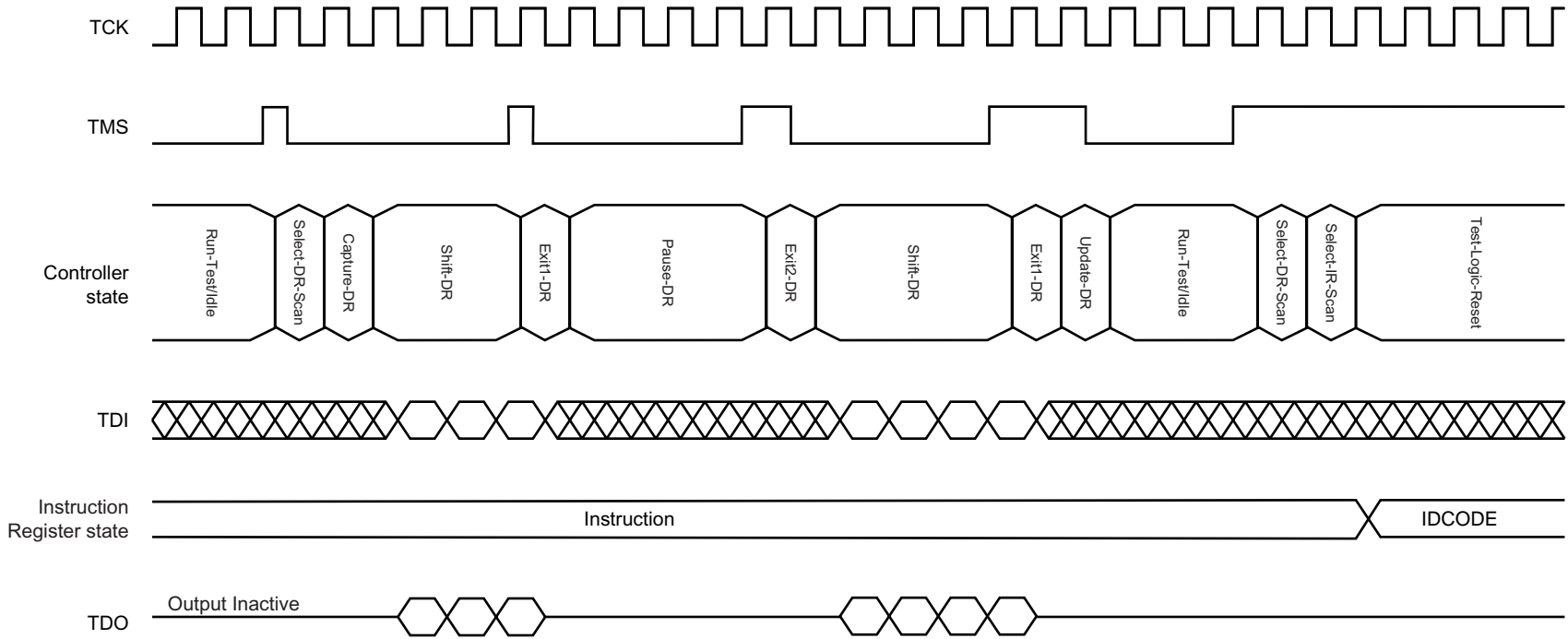
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V<sub>DD</sub> through a 1k Ω resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)

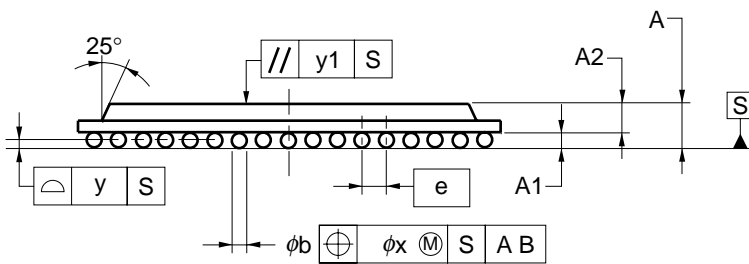
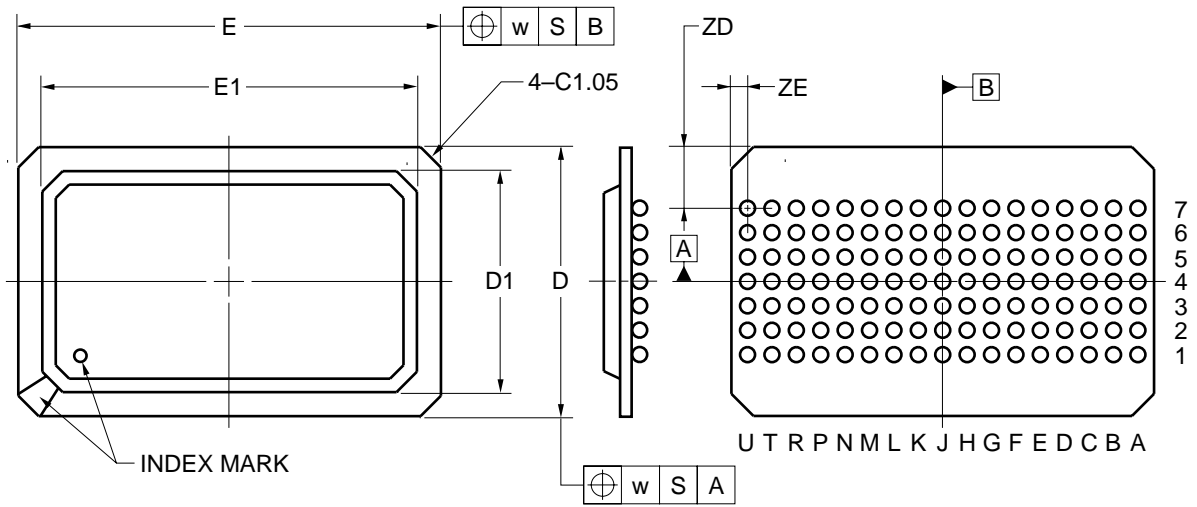


Test Logic (Data Scan)



Package Drawing

119-PIN PLASTIC BGA (14x22)



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	22.00±0.20
D1	12.00
E1	19.50
w	0.30
e	1.27
A	2.06±0.30
A1	0.60±0.10
A2	1.46
b	0.75±0.15
x	0.15
y	0.15
y1	0.35
ZD	3.19
ZE	0.84

P119F1-127-FJ1

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD44323362.

**Type of Surface Mount Device**

$\mu$ PD44323362F1-FJ1: 119-pin plastic BGA



Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
4th edition/ May 2004	Throughout	Throughout	Modification	—	Preliminary Data Sheet → Data Sheet
	Throughout	Throughout	Deletion	Ordering Information	μPD44323182F1-C40-FJ1 μPD44323182F1-C50-FJ1 μPD44323362F1-C50-FJ1

[MEMO]

**NOTES FOR CMOS DEVICES****① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

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