NEC
μPD446
μPD446-1
μPD446-2
PRELIMINARY

2048 x 8 BIT STATIC CMOS RAM

DESCRIPTION

The μPD446 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD446 a very low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when $\overline{CE}$ equals V_{CC} independently of the other input levels.

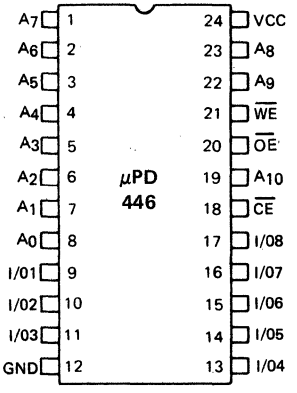
Data retention is guaranteed at a power supply voltage as low as 2V.

The μPD446 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or Refreshing required
- TTL Compatible — All Inputs and Outputs
- Common I/O Using Three-State Output
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Max Access/Min Cycle Times Down to 120 ns
- Low Power Dissipation, 45 mA Max Active/100 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage — 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs

PIN CONFIGURATION



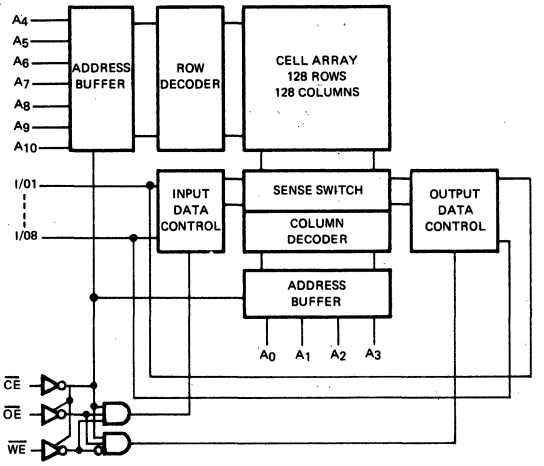
PIN NAMES

A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1-I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	ICC
H	X	X	NOT SELECTED	HZ	STANDBY
L	H	H	NOT SELECTED	HZ	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE
L	X	L	WRITE	D_{IN}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . . -0.3 to VCC + 0.3V
Storage Temperature Range . . . . . -55°C to 125°C
Operating Temperature Range . . . . . 0°C to 70°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0 to 70°C; V_{CC} = 5.0V ± 10%

CHARACTERISTIC	SYMBOL	μPD446-2			μPD446-1			μPD446			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	-0.3		0.8	-0.3		0.8	V	
Input Leakage Current	I_{LI}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	V_{IN} = 0~ V_{CC}
I/O Leakage Current	I_{LO}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	V_{CS} = V_{IH} $V_{I/O}$ = 0 ~ V_{CC}
Operating Supply Current	I_{CCA1}		30	45		25	38		20	30	mA	V_{CS} = V_{IL} $I_{I/O}$ = 0 MIN TCYCLE
	I_{CCA2}		5	10		5	10		5	10	mA	V_{CS} = V_{IL} $I_{I/O}$ = 0 DC CURRENT
Standby Current	I_{CCS}			100			100			100	μA	V_{CS} = V_{CC} V_{IN} = 0 ~ V_{CC}
Output High Voltage	V_{OH}	2.4			2.4			2.4			V	I_{OH} = -1.0 mA
Output Low Voltage	V_{OL}			0.4			0.4			0.4	V	I_{OL} = 2.0 mA

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS						UNIT
		μPD446-2		μPD446-1		μPD446		
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Chip Enable Access Time	t_{ACS}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		75		100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Enable to Output in LZ	t_{CLZ}	10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	10		10		10		ns
Chip Disable to Output in HZ	t_{CHZ}		60		75		100	ns
Output Disable to Output in HZ	t_{OHZ}		60		75		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS						UNIT
		μPD446-2		μPD446-1		μPD446		
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	120		150		200		ns
Chip Enable to End of Write	t_{CW}	100		125		170		ns
Address Valid to End of Write	t_{AW}	100		125		170		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulsewidth	t_{WP}	100		125		170		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to End of Write	t_{DW}	60		75		100		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in HZ	t_{WHZ}		60		75		100	ns
Output Active from End of Write	t_{OW}	20		20		20		ns

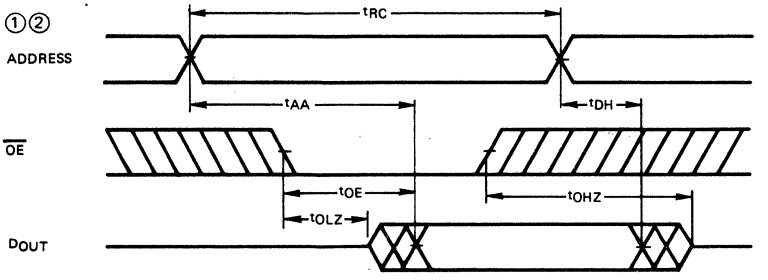
LOW V_{CC} DATA RETENTION

T_a = 0°C to 70°C

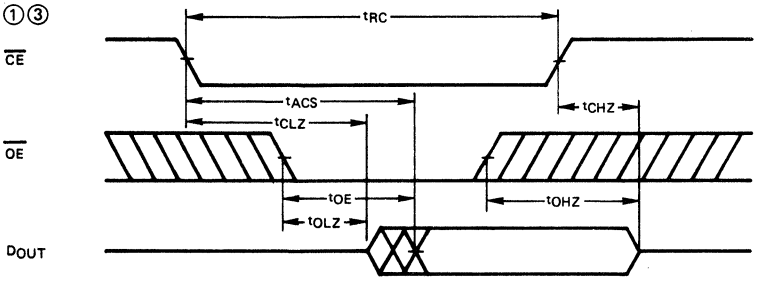
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
VCC for Data Retention	V_{CCDR}	V_{IN} = 0 ~ V_{CC}, $V_{\overline{CE}}$ = V_{CC}	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, V_{IN} = 0 ~ V_{CC} $V_{\overline{CE}}$ = V_{CC}		0.1	10	μA
Chip Deselection to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

TIMING WAVEFORMS

READ CYCLE (1)



READ CYCLE (2)



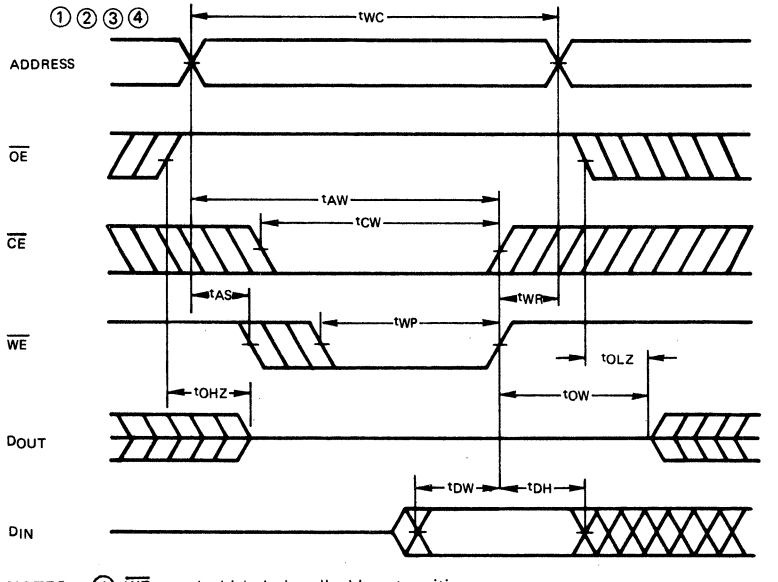
NOTES:

① $\overline{WE}$ is high for read cycles.

② Device is continuously selected, $\overline{CE} = V_{IL}$.

③ Address valid prior to or coincident with $\overline{CE}$ transition low.

WRITE CYCLE (1)



NOTES:

① $\overline{WE}$ must be high during all address transition.

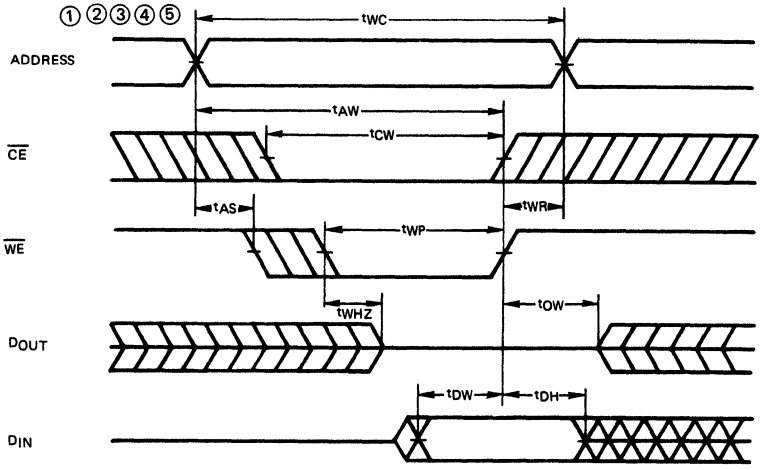
② A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.

③ t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

④ If the CS low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.

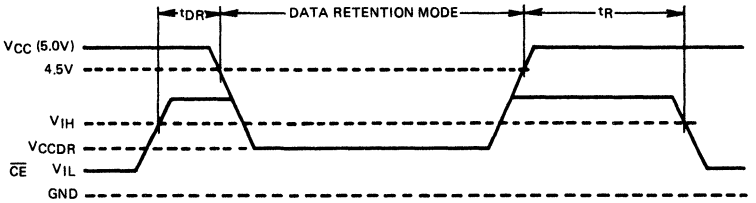
TIMING WAVEFORMS (CONT.)

WRITE CYCLE (2)



Notes:
① $\overline{WE}$ must be high during all address transition.
② A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
③ t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
④ If the CS low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.
⑤ $\overline{OE}$ is continuously low ($\overline{OE}$ – V_{IL}).

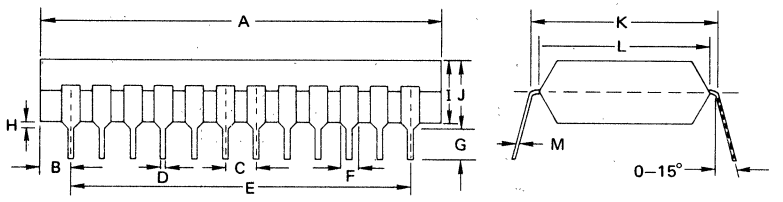
LOW V_{CC} DATA RETENTION TIMING CHART



AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF

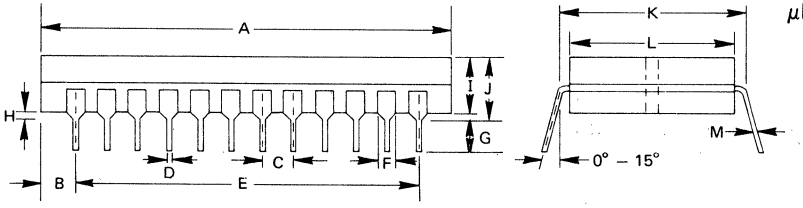
PACKAGE OUTLINE
μPD446C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD446D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$