DATA SHEET

ELPIDA

MOS INTEGRATED CIRCUIT

μPD4516161D

16M-bit Synchronous DRAM
2-banks, LVTTL

Description

The μPD4516161D is high-speed 16,777,216-bit synchronous dynamic random-access memory, organized as 524,288 words × 16 bits × 2 banks respectively.

The synchronous DRAMs achieved high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).

This product is packaged in 50-pin TSOP (II).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11
- Byte control by LDQM and UDQM
- Programmable Wrap sequence: Sequential / Interleave
- Programmable burst length: 1, 2, 4, 8 and full page
- /CAS latency: 3
- CBR (Auto) refresh and self refresh
- ×16 organization
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible
- 2,048 refresh cycles / 32 ms
- Burst termination by Burst stop command and Precharge command

Ordering Information

Part number	Organization (word × bit × bank)	Clock frequency MHz (MAX.)	Package
μPD4516161DG5-A70-9NF	512K × 16 × 2	143	50-pin PLASTIC TSOP (II) (10.16mm(400))
μPD4516161DG5-A75-9NF		133	
μPD4516161DG5-A80-9NF		125	
μPD4516161DG5-A10-9NF		100	

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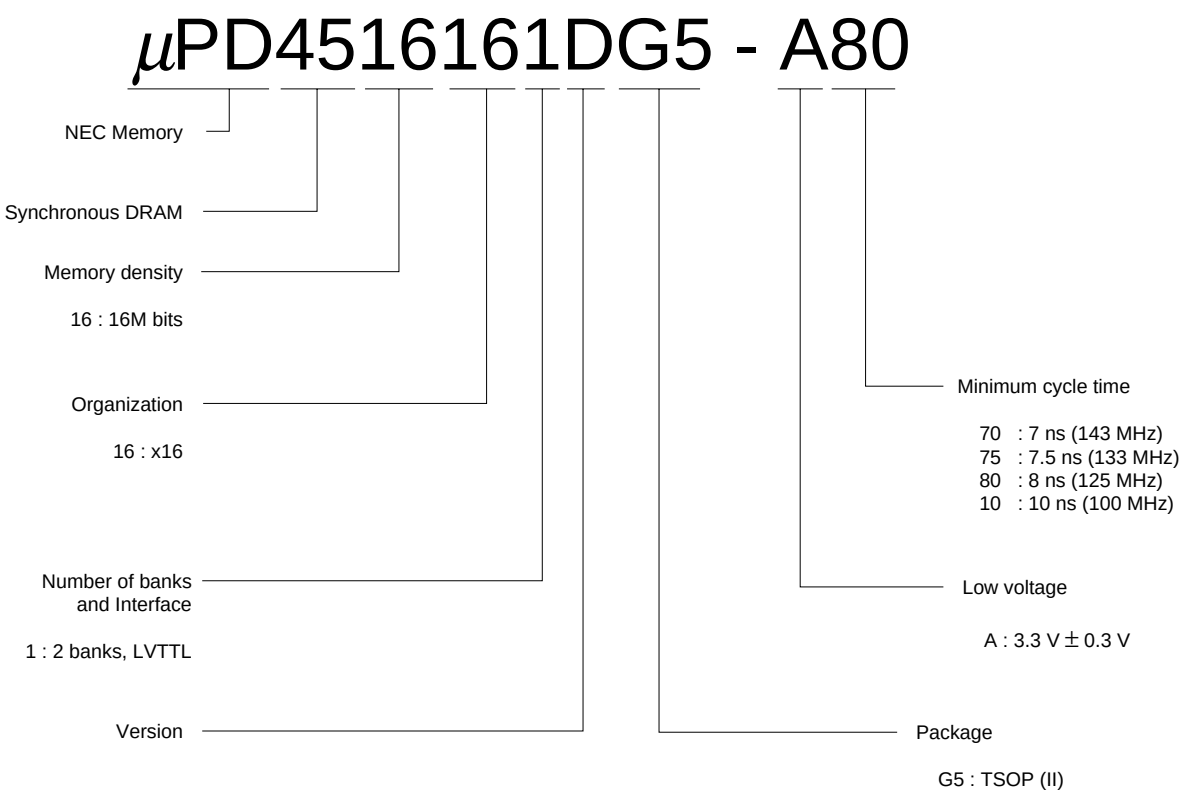
Not all devices/types available in every country. Please check with local Elpida Memory, Inc. for availability and additional information.

Document No. E0143N10 (Ver.1.0)
(Previous No. M14888EJ2V0DS00)
Date Published May 2001 CP (K)
Printed in Japan

Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

Part Number


μPD4516161DG5 - A80
NEC Memory
Synchronous DRAM
Memory density
16 : 16M bits
Organization
16 : x16
Number of banks and Interface
1 : 2 banks, LVTTL
Version
Package
G5 : TSOP (II)
Low voltage
A : 3.3 V ± 0.3 V
Minimum cycle time
70 : 7 ns (143 MHz)
75 : 7.5 ns (133 MHz)
80 : 8 ns (125 MHz)
10 : 10 ns (100 MHz)

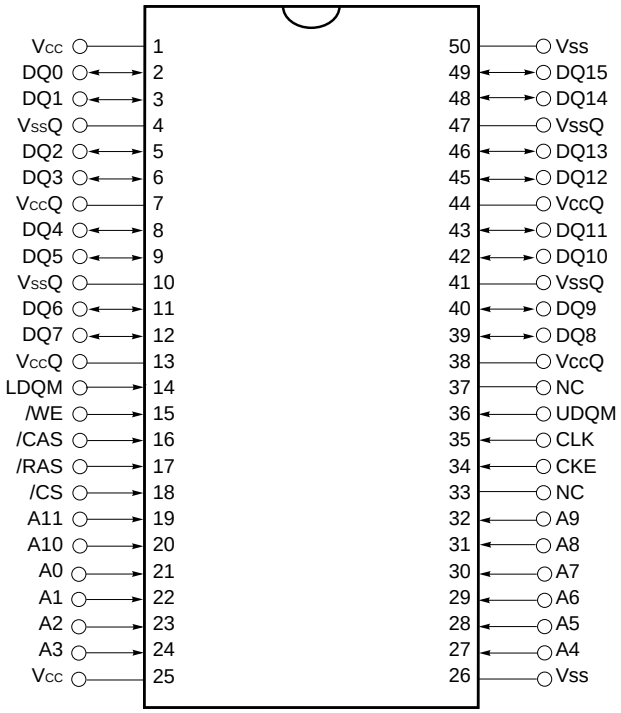
Pin Configuration

/xxx indicates active low signal.

[μPD4516161DG5]

50-pin PLASTIC TSOP (II) (10.16mm (400))

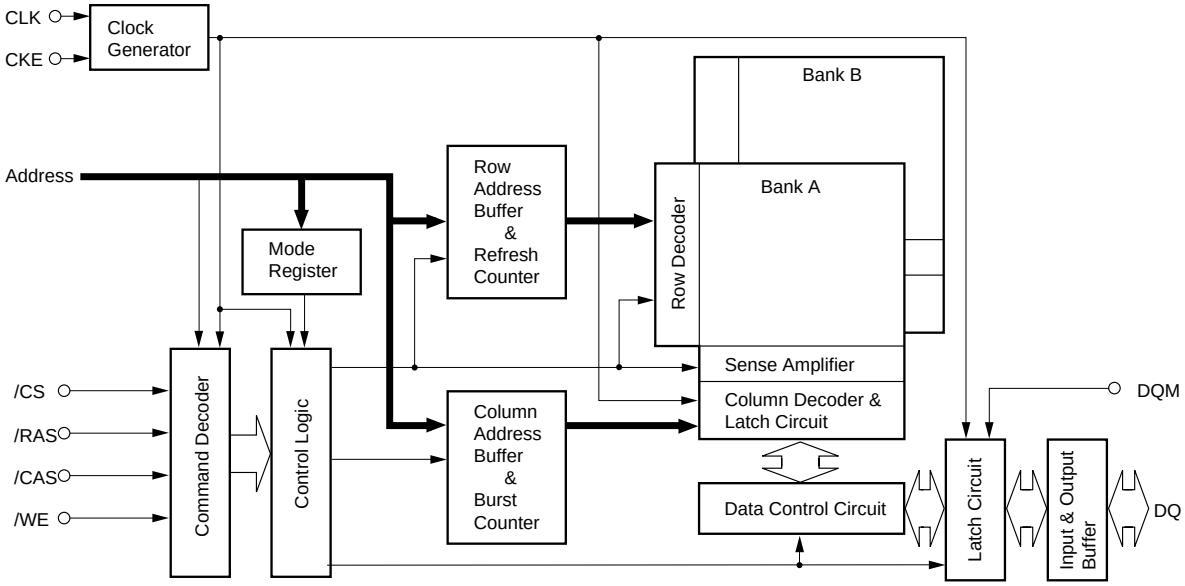
512K words × 16 bits × 2 banks



A0 to A11 [Note] : Address inputs
DQ0 to DQ15 : Data inputs / outputs
CLK : Clock input
CKE : Clock enable
/CS : Chip select
/RAS : Row address strobe
/CAS : Column address strobe
/WE : Write enable
LDQM : Lower DQ mask enable
UDQM : Upper DQ mask enable
VCC : Supply voltage
VSS : Ground
VCCQ : Supply voltage for DQ
VSSQ : Ground for DQ
NC : No connection

Note A0 to A10 : Row address inputs
A0 to A7 : Column address inputs
A11 : Bank select

Block Diagram



CONTENTS

1. Input / Output Pin Function

Pin name	Input / Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the μPD4516161D suspends operation. When the μPD4516161D is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
/CS	Input	/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.
/RAS, /CAS, /WE	Input	/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A11	Input	Row Address is determined by A0 - A10 at the CLK (clock) rising edge in the activate command cycle. It does not depend on the bit organization. Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. A11 is the bank select signal (BS). In command cycle, A11 low selects bank A and A11 high selects bank B. A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precharged; when A10 is low, only the bank selected by A11 is precharged. When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.
UDQM, LDQM	Input	UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ15	Input / Output	DQ pins have the same function as I/O pins on a conventional DRAM.
V_{CC}, V_{SS}, $V_{CC}Q$, $V_{SS}Q$	(Power supply)	V_{CC} and V_{SS} are power supply pins for internal circuits. $V_{CC}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.

2. Commands

Mode register set command

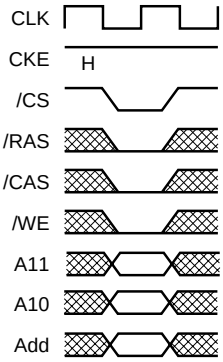
(/CS, /RAS, /CAS, /WE = Low)

The μPD4516161D has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state.

During 2 CLK (t_{RSC}) following this command, the μPD4516161D cannot accept any other commands.

Fig.1 Mode register set command



Activate command

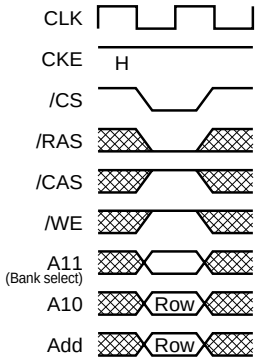
(/CS, /RAS = Low, /CAS, /WE = High)

The μPD4516161D has two banks, each with 2,048 rows.

This command activates the bank selected by A11(BS) and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's /RAS falling.

Fig.2 Row address strobe and bank activate command



Precharge command

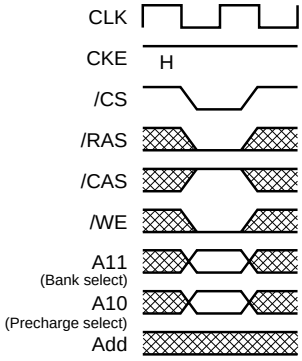
(/CS, /RAS, /WE = Low, /CAS = High)

This command begins precharge operation of the bank selected by A11(BS). When A10 is High, both banks are precharged, regardless of A11. When A10 is Low, only the bank selected by A11 is precharged. A11 low selects bank A and A11 high selects bank B.

After this command, the μPD4516161D can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

This command corresponds to a conventional DRAM's /RAS rising.

Fig.3 Precharge command

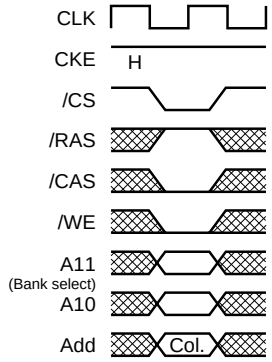


Write command

(/CS, /CAS, /WE = Low, /RAS = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can be input with this command with subsequent data on following clocks.

Fig.4 Column address and write command

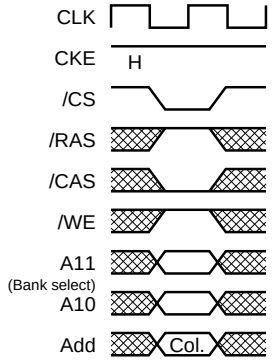


Read command

(/CS, /CAS = Low, /RAS, /WE = High)

Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.

Fig.5 Column address and read command



CBR (auto) refresh command

(/CS, /RAS, /CAS = Low, /WE, CKE = High)

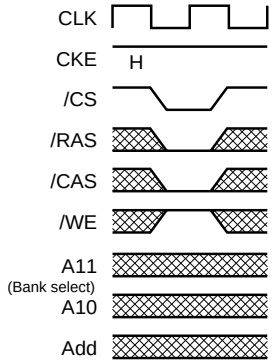
This command is a request to begin the CBR (auto) refresh operation. The refresh address is generated internally.

Before executing CBR (auto) refresh, both banks must be precharged.

After this cycle, both banks will be in the idle (precharged) state and ready for a row activate command.

During t_{RC} period (from refresh command to refresh or activate command), the μPD4516161D cannot accept any other command.

Fig.6 CBR (auto) refresh command



Self refresh entry command

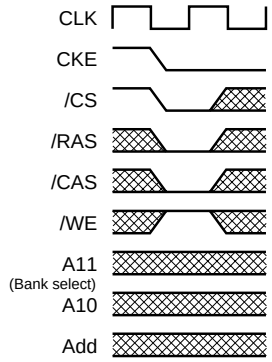
(/CS, /RAS, /CAS, CKE = Low, /WE = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the μPD4516161D exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, both banks must be precharged.

Fig.7 Self refresh entry command

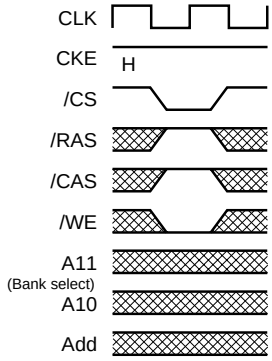


Burst stop command

(/CS, /WE = Low, /RAS, /CAS = High)

This command terminates the current burst operation.

Fig.8 Burst stop command in Full Page Mode

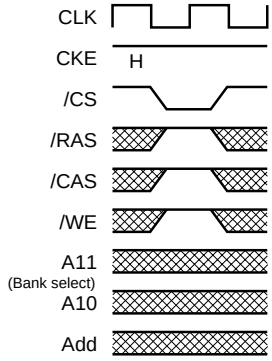


No operation

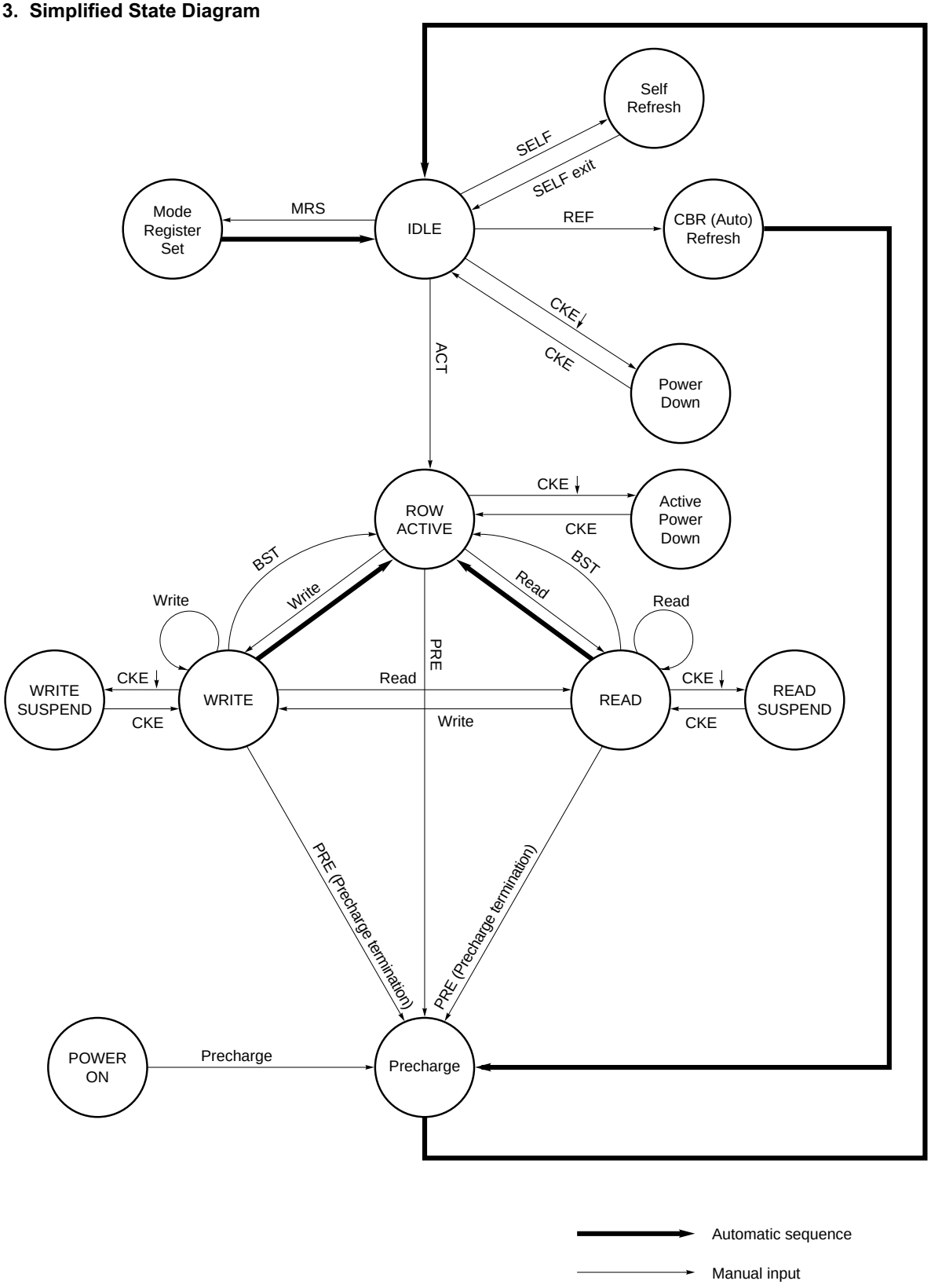
(/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.

Fig.9 No operation



3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	A11	A10	A9 - A0
		n – 1	n							
Device deselect	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop	BST	H	×	L	H	H	L	×	×	×
Read	READ	H	×	L	H	L	H	V	L	V
Write	WRIT	H	×	L	H	L	L	V	L	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge both banks	PALL	H	×	L	L	H	L	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	V

Remark H = High level, L = Low level, × = High or Low level (Don't care), V = Valid data input

4.2 DQM Truth Table

Function	Symbol	CKE		DQM	
		n – 1	n	U	L
Data write / output enable	ENB	H	×	L	
Data mask / output disable	MASK	H	×	H	
Upper byte write enable / output enable	ENBU	H	×	L	×
Lower byte write enable / output enable	ENBL	H	×	×	L
Upper byte write inhibit / output disable	MASKU	H	×	H	×
Lower byte write inhibit / output disable	MASKL	H	×	×	H

Remark H = High level, L = Low level, × = High or Low level (Don't care)

4.3 CKE Truth Table

Current state	Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	Address
			n – 1	n					
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend mode		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	CBR (auto) refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Idle	Power down entry		H	L	×	×	×	×	×
Power down	Power down exit		L	H	×	×	×	×	×

Remark H = High level, L = Low level, × = High or Low level (Don't care)

4.4 Operative Command Table [Note1]

(1/2)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop or power down	3
	L	H	H	×	×	NOP or BST	Nop or power down	3
	L	H	L	H	BA, CA, A10	READ	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF/SELF	CBR (auto) refresh or self refresh	5
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	×	×	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ	Begin read : Determine AP	6
	L	H	L	L	BA, CA, A10	WRIT	Begin write : Determine AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Precharge	7
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ	Terminate burst, new read : Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT	Terminate burst, start write : Determine AP	8, 9
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, precharging	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ	Terminate burst, start read : Determine AP	8, 9
	L	H	L	L	BA, CA, A10	WRIT	Terminate burst, new write : Determine AP	8
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, precharging	10
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/2)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	×	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	×	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	×	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	×	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA, CA, A10	READ	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4, 11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	×	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	×	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ	Start read	9
	L	H	L	L	BA, CA, A10	WRIT	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	×	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	×	×	×	×	DESL	Nop → Enter idle after t_{RC}	
	L	H	H	×	×	NOP/BST	Nop → Enter idle after t_{RC}	
	L	H	L	×	×	READ/WRIT	ILLEGAL	
	L	L	H	×	×	ACT/PRE/PALL	ILLEGAL	
	L	L	L	×	×	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop → Enter idle after t_{RSC}	
	L	H	H	H	×	NOP	Nop → Enter idle after t_{RSC}	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	×	×	READ/WRIT	ILLEGAL	
	L	L	×	×	×	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Notes 1. H = High level, L = Low level, × = High or Low level (Don't care), V = Valid data input

2. All entries assume that CKE was active (High level) during the preceding clock cycle.

3. If both banks are idle, and CKE is inactive (Low level), μPD4516161D will enter Power down mode. All input buffers except CKE will be disabled.

4. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

5. If both banks are idle, and CKE is inactive (Low level), μPD4516161D will enter Self refresh mode. All input buffers except CKE will be disabled.

6. Illegal if t_{RCD} is not satisfied.

7. Illegal if t_{RAS} is not satisfied.

8. Must satisfy burst interrupt condition.

9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

10. Must mask preceding data which don't satisfy t_{DPL}.

11. Illegal if t_{RRD} is not satisfied.

4.5 Command Truth Table for CKE [Note1]

Current State	CKE		/CS	/RAS	/CAS	/WE	Address	Action	Notes
	n – 1	n							
Self refresh	H	×	×	×	×	×	×	INVALID, CLK (n – 1) would exit self refresh	
	L	H	H	×	×	×	×	Self refresh recovery	
	L	H	L	H	H	×	×	Self refresh recovery	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Maintain self refresh	
Self refresh recovery	H	H	H	×	×	×	×	Idle after t_{RC}	
	H	H	L	H	H	×	×	Idle after t_{RC}	
	H	H	L	H	L	×	×	ILLEGAL	
	H	H	L	L	×	×	×	ILLEGAL	
	H	L	H	×	×	×	×	ILLEGAL	
	H	L	L	H	H	×	×	ILLEGAL	
	H	L	L	H	L	×	×	ILLEGAL	
	H	L	L	L	×	×	×	ILLEGAL	
Power down	H	×	×	×	×	×		INVALID, CLK (n – 1) would exit power down	
	L	H	×	×	×	×	×	EXIT power down → Idle	
	L	L	×	×	×	×	×	Maintain power down mode	
Both banks idle	H	H	H	×	×	×		Refer to operations in Operative Command Table	
	H	H	L	H	×	×		Refer to operations in Operative Command Table	
	H	H	L	L	H	×		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	×	CBR (auto) refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	×	×	×		Refer to operations in Operative Command Table	
	H	L	L	H	×	×		Refer to operations in Operative Command Table	
	H	L	L	L	H	×		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	×	Self refresh	2
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	×	×	×	×	×	×	Power down	2
Row active	H	×	×	×	×	×		Refer to operations in Operative Command Table	
	L	×	×	×	×	×		Power down	3
Any state other than listed above	H	H	×	×	×	×	×	Refer to operations in Operative Command Table	
	H	L	×	×	×	×	×	Begin clock suspend next cycle	3
	L	H	×	×	×	×	×	Exit clock suspend next cycle	
	L	L	×	×	×	×	×	Maintain clock suspend	

Notes 1. H = High level, L = Low level, × = High or Low level (Don't care)

2. Self refresh can be entered only from the both banks idle state. Power down can be entered from the both banks idle state or row active state.

3. Must be legal command as defined in Operative Command Table.

4.6 Command Truth Table for Two Banks Operation [Note1, 2]

/CS	/RAS	/CAS	/WE	BA	A10	A9 - A0	Action	"FROM" State [Note3]	"TO" State [Note4]
H	×	×	×	×	×	×	NOP	Any	Any
L	H	H	H	×	×	×	NOP	Any	Any
L	H	H	L	×	×	×	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	L	CA	Read	(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	L	CA	Write	(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	H	L	×	H	×	Precharge	(R/W/A/I)0(I/A)1	I0I1
				×	H	×		(R/W/A/I)1(I/A)0	I1I0
				H	L	×		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	×		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	×		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	×		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	×	×	×	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes 1. Logic level abbreviations

H: High level, L: low level, ×: High or Low level (Don't care)

Pin name abbreviation

BA: Bank address (A11)

2. State abbreviations

I = Idle

A = Row active

R = Read with No precharge (No precharge is posted)

W = Write with No precharge (No precharge is posted)

Any = Any State

X0Y1 = Y1X0 = Bank A is in state "X", Bank B is in state "Y"

(X/Y)0Z1 = Z1(X/Y)0 = Bank A is in state "X" or "Y". Bank B is in state "Z"

3. If the μPD4516161D is in a state other than above listed the "From State" column, the command is illegal.

4. The state listed under "To" might not be entered on the next clock cycle. Timing restrictions apply.

5. Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 100 μs or longer pause must precede any signal toggling.

(2) After the pause, both banks must be precharged using the Precharge command (The Precharge both banks command is convenient).

(3) Once the precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed. After the mode register set cycle, t_{RSC} (2 CLK minimum) pause must be satisfied as well.

(4) Tow or more CBR(Auto) refresh must be performed.

Remarks 1. The sequence of Mode register programming and Refresh above may be transposed.

2. CKE and DQM must be held high until the Precharge command is issued to ensure data bus Hi-Z.

6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or until the device loses power.

The mode register has four fields;

Options : A11 through A7
/CAS latency : A6 through A4
Wrap type : A3
Burst length : A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters to be set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The table on page 33 shows the relationship of /CAS latency to the clock period and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. The table on the page 21 shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Only the sequential burst supports the full page length.

7. Mode Register

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	1								Reserved Test Set
x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write
x	0	0	0	0	LTMODE			WT	BL			Mode Register Set

x = Don't care

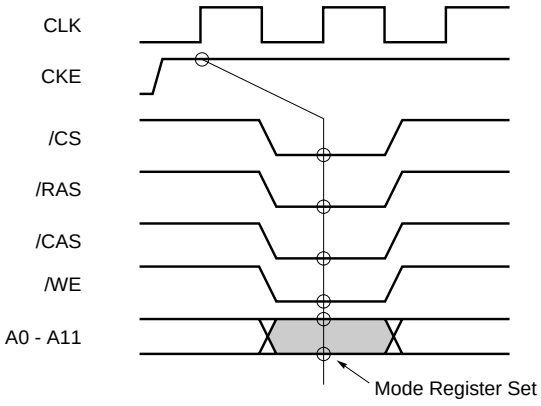
	Bits2-0	WT = 0	WT = 1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

	Bits6-4	/CAS latency
Latency mode	000	R
	001	R
	010	R
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Mode Register Set Timing



7.1 Burst Length and Sequence

[Burst of Two]

Starting address (column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting address (column address A1 - A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting address (column address A2 - A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of sequential addressing, with the length being 256.

8. Address Bits of Bank-Select and Precharge

Row

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

(Activate command)

A11	Result
0	**Select Bank A “Activate” command**
1	**Select Bank B “Activate” command**

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

(Precharge command)

A10	A11	Result
0	0	**Precharge Bank A**
0	1	**Precharge Bank B**
1	x	**Precharge Both Banks**

x : Don’t care

A10	Result
0	**disables Auto-Precharge (End of Burst)**

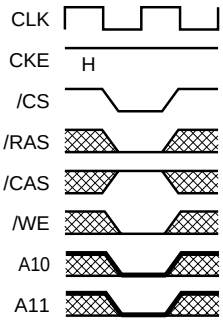
Col.

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

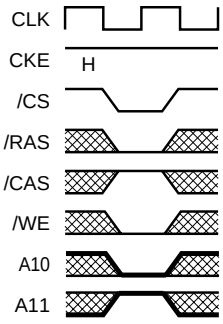
(/CAS strobes)

A11	Result
0	**enables Read/Write commands for Bank A**
1	**enables Read/Write commands for Bank B**

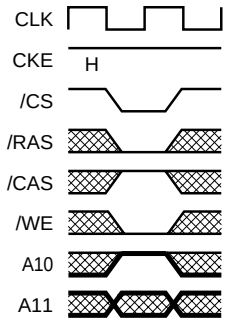
Precharge for Bank A



Precharge for Bank B



Precharge for Both banks



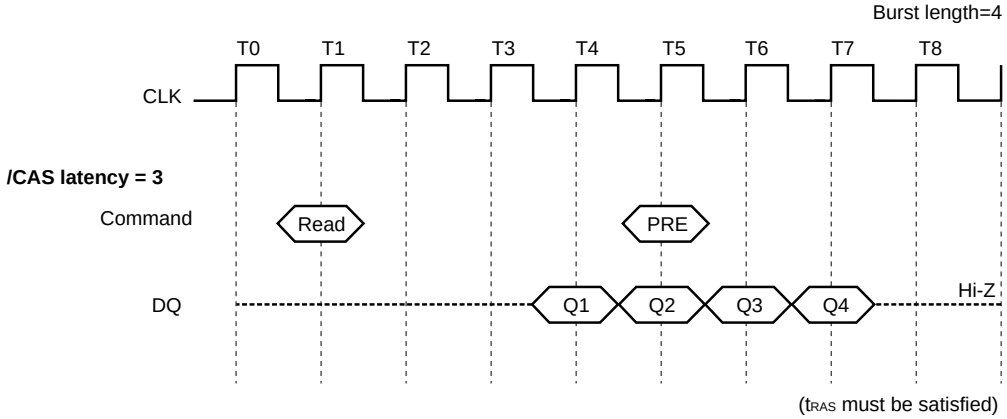
9. Precharge

The precharge command can be issued anytime after $t_{RAS\ (MIN.)}$ is satisfied.

Soon after the precharge command is issued, precharge operation performed. The synchronous DRAM enters the idle state after t_{RP} is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.

/CAS latency = 3: Two clocks earlier than the last read data.



In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}" must be satisfied. The $t_{DPL\ (MIN.)}$ specification defines the earliest time that a precharge command can be issued. The minimum number of clocks is calculated by dividing $t_{DPL\ (MIN.)}$ by the clock cycle time.

In summary, the precharge command can be issued relative to the reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

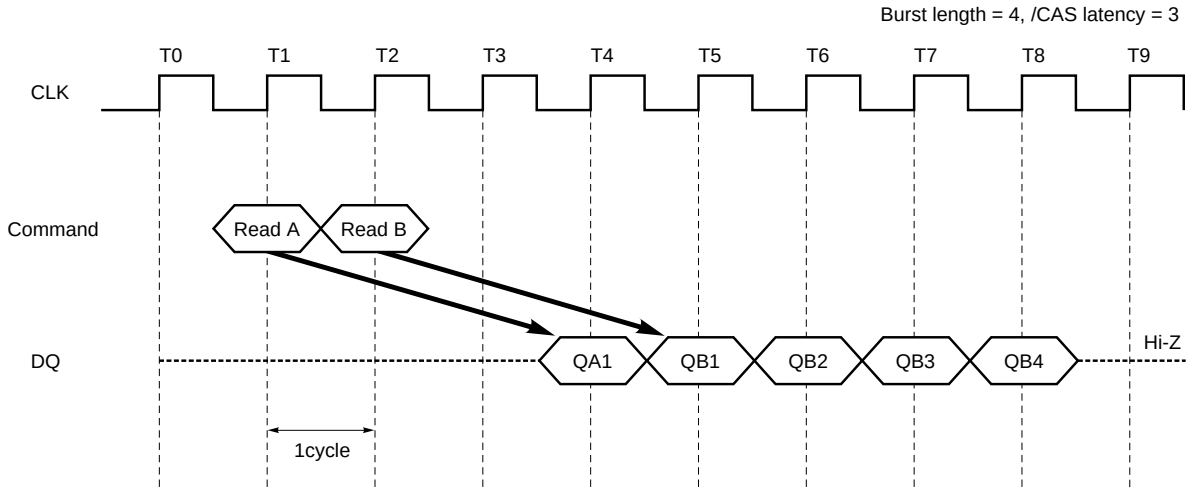
/CAS latency	Read	Write
3	–2	$+t_{DPL\ (MIN.)}$

10. Read / Write Command Interval

10.1 Read to Read Command Interval

When a new Read command is issued during a read cycle, it will be effective after the /CAS latency, even if the previous read operation has not completed. READ will be interrupted by another READ.

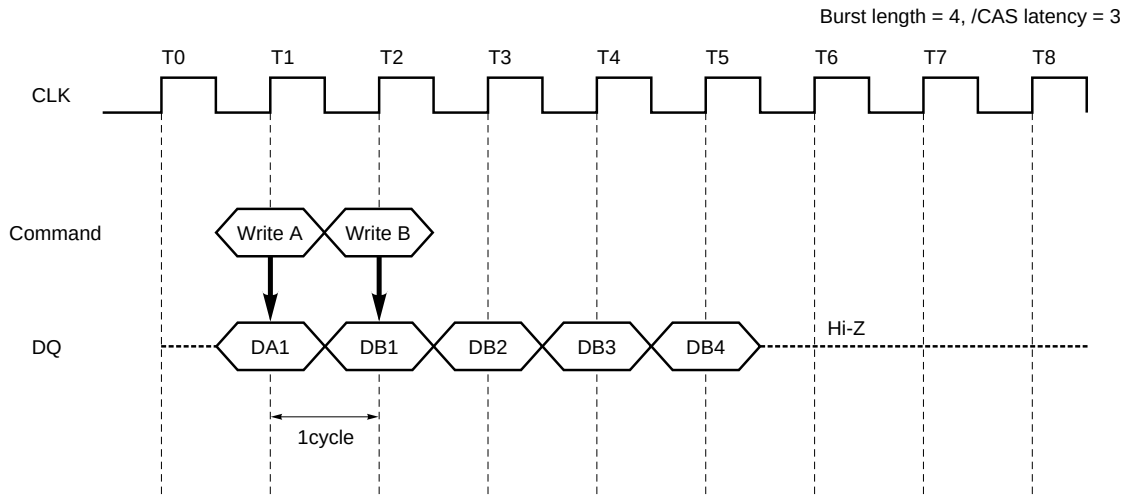
The interval between the commands is 1 cycle minimum. Each read command can be issued in every clock without any restriction.



10.2 Write to Write Command Interval

When a new Write command is issued during a write cycle, the previous burst will be terminated and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each write command can be issued in every clock without any restriction.

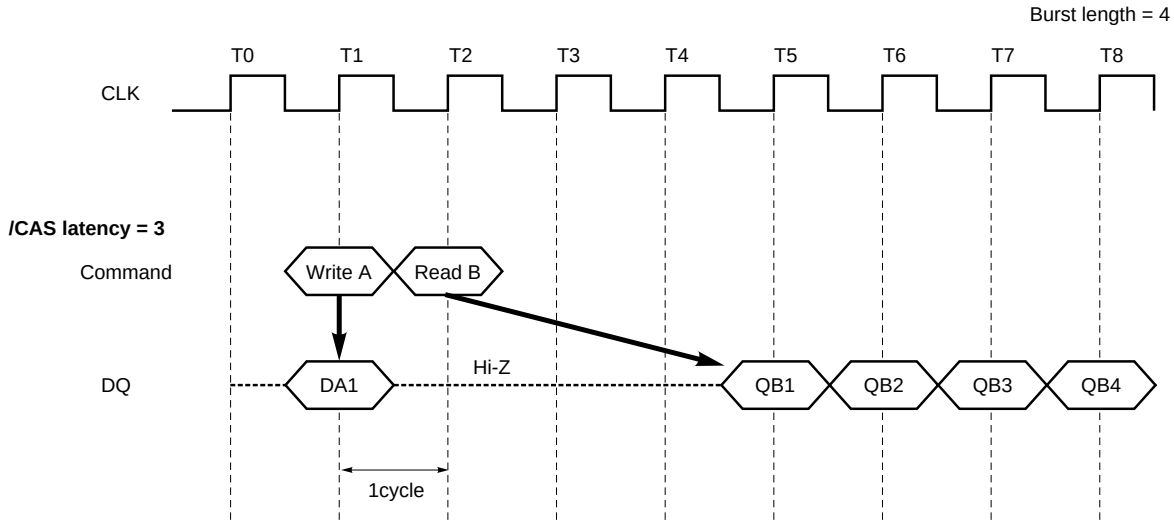


10.3 Write to Read Command Interval

The write command to Read command interval is a minimum of 1 cycle.

Only the write data preceding Read command will be written.

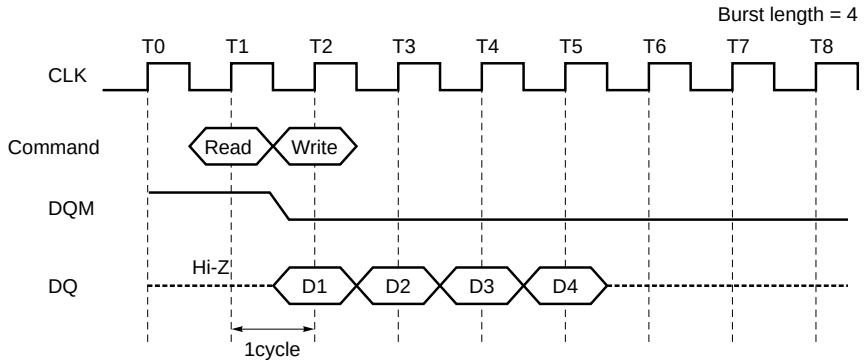
The data bus must be in high-impedance at least one cycle prior to the first DOUT.



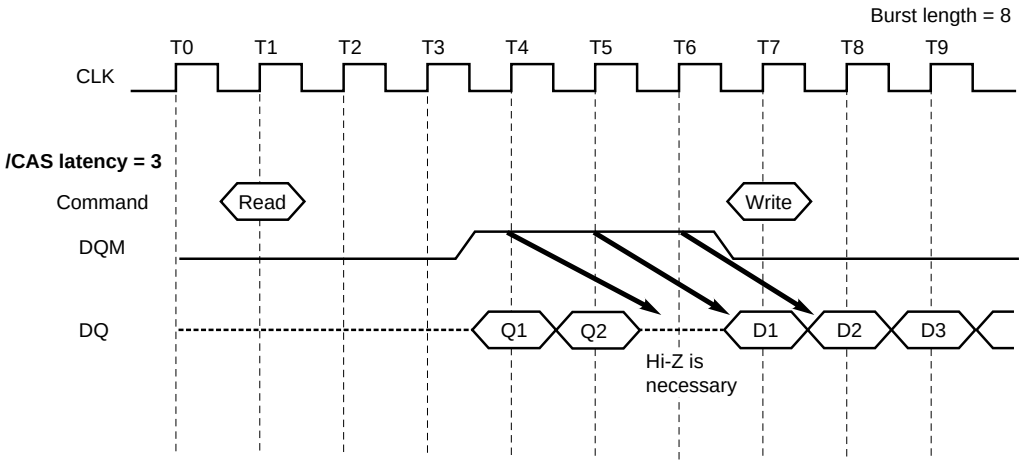
10.4 Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The data bus be Hi-Z using DQM before WRITE.



READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.

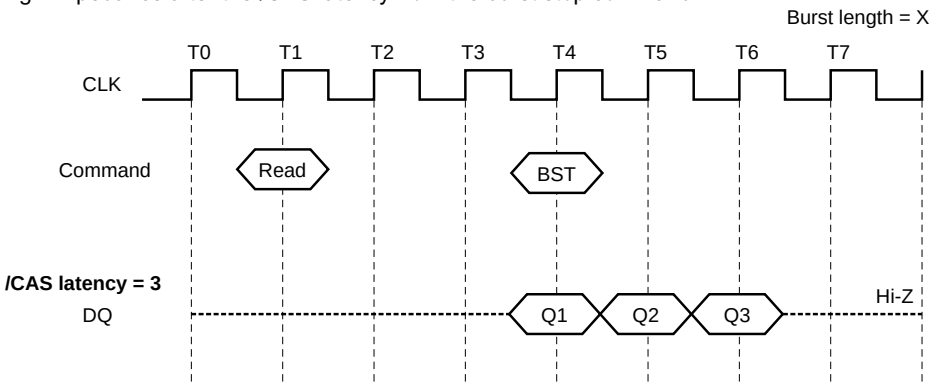


11. Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

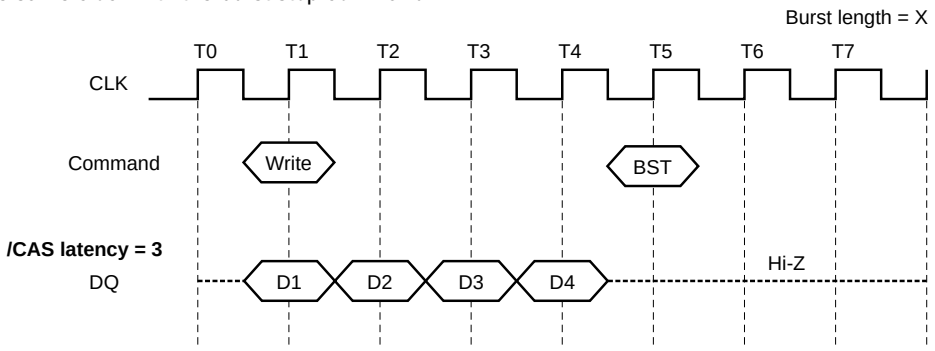
11.1 Burst Stop Command

During a read burst, when the burst stop command is issued, the burst read outputs are terminated and the data bus goes to high-impedance after the /CAS latency from the burst stop command.



Remark BST : Burst stop command

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to Hi-Z at the same clock with the burst stop command.



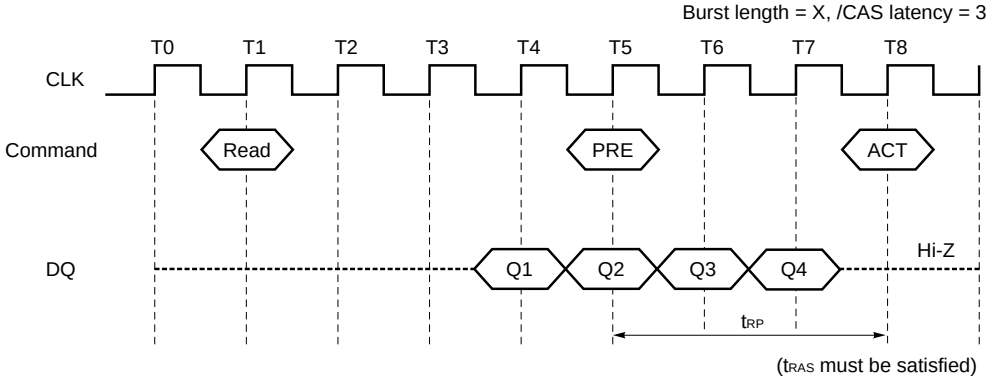
Remark BST : Burst stop command

11.2 Precharge Termination

11.2.1 Precharge Termination in READ Cycle

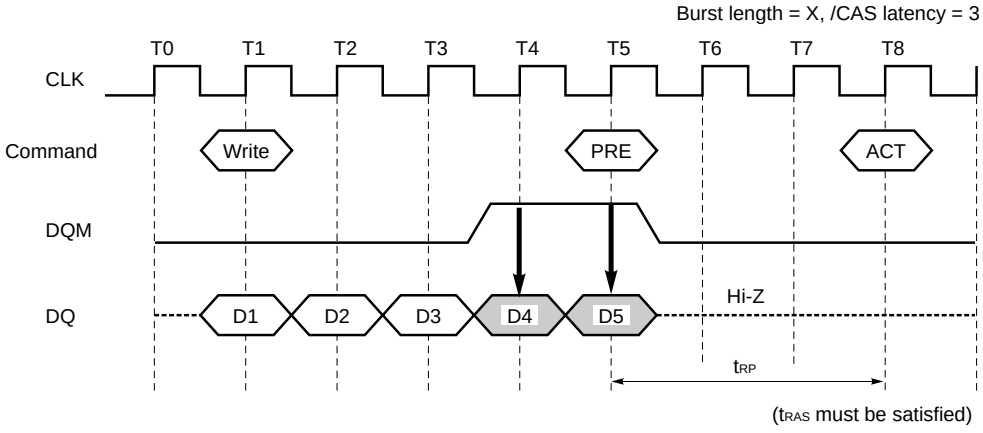
During a read cycle, the burst read operation can be terminated by a precharge command.
When the precharge command is issued, the burst read operation is terminated and precharge starts.
The same bank can be activated again after t_{RP} from the precharge command.

When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.



11.2.2 Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation can be terminated by a precharge command.
When the precharge command is issued, the burst write operation is terminated and precharge starts.
The same bank can be activated again after $t_{RP(MIN.)}$ from the precharge command.
When /CAS latency is 3, the write data written 2 clock prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock and one clock before the precharge command. To prevent this from happening, DQM must be high at the same clock and one clock before the precharge command. This will mask the invalid data.



12. Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and CBR (auto) Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}, $V_{CC}Q$		−0.5 to +4.6	V
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		−55 to + 125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}, $V_{CC}Q$		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC}+0.3 Note1	V
Low level input voltage	V_{IL}		−0.3 Note2		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Notes 1. $V_{IH\ (MAX.)} = V_{CC} + 2.0$ V (Pulse width ≤ 3 ns)

2. $V_{IL\ (MIN.)} = -2.0$ V (Pulse width ≤ 3 ns)

Pin Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11	2.5		4	pF
	C_{I2}	CLK, CKE, /CS, /RAS, /CAS, /WE, UDQM, LDQM	2.5		4	
Data input / output capacitance	$C_{I/O}$	DQ0 - DQ15	4		6	pF

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	/CAS latency	Grade	Max.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, I/O = 0 mA, One bank active	CL = 3	-A70	140	mA	1
				-A75	130		
				-A80	120		
				-A10	120		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			3	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			2		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			25	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.			6		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			3	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			2		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			30	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.			15		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA, Both banks active	CL=3	-A70	140	mA	2
				-A75	130		
				-A80	120		
				-A10	100		
CBR (auto) refresh current	I_{CC5}	$t_{CK} = t_{CK\ (MIN.)}$ t_{RC} = 100 ns		-A70	90	mA	3
				-A75	90		
				-A80	90		
				-A10	90		
		$t_{CK} = t_{CK\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$		-A70	140		
				-A75	130		
				-A80	120		
				-A10	120		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V			1	mA	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured condition that addresses are changed only one time during t_{CK} (MIN.).

2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured condition that addresses are changed only one time during t_{CK} (MIN.).

3. I_{CC5} is measured on condition that addresses are changed only one time during t_{CK} (MIN.).

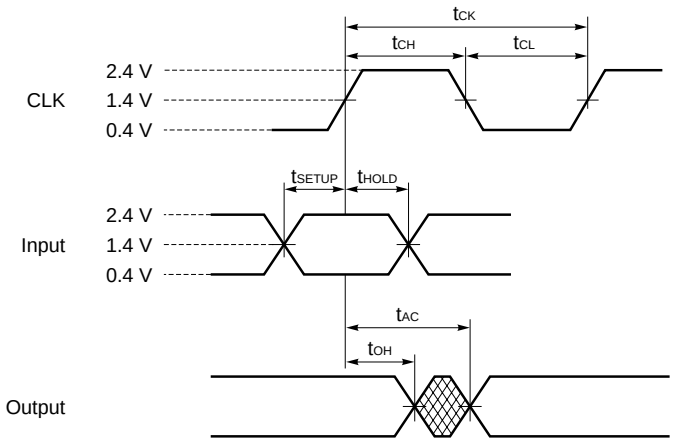
DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Note
Input leakage current	$I_{I(L)}$	$0 \le V_I \le V_{CC}Q$, $V_{CC}Q = V_{CC}$ All other pins not under test = 0 V	–1.0		+1.0	μA	
Output leakage current	$I_{O(L)}$	$0 \le V_O \le V_{CC}Q$, D_{OUT} is disabled	–1.5		+1.5	μA	
High level output voltage	V_{OH}	I_O = –4 mA	2.4			V	
Low level output voltage	V_{OL}	I_O = +4 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

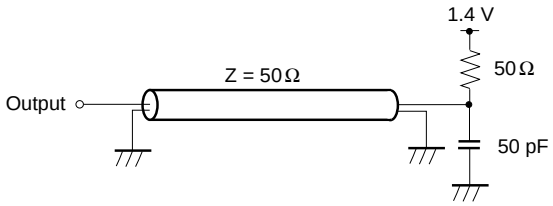
Parameter	Value	Unit
AC high level input voltage / low level input voltage	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Transition time (Input rise and fall time)	1	ns
Output timing measurement reference level	1.4	V



Synchronous Characteristics

Parameter		Symbol	-A70		-A75		-A80		-A10		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	7	(143 MHz)	7.5	(133 MHz)	8	(125 MHz)	10	(100 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		5.4		5.4		6		6	ns	1
CLK high level width		t_{CH}	2.5		2.5		3		3		ns	
CLK low level width		t_{CL}	2.5		2.5		3		3		ns	
Data-out hold time		t_{OH}	2		2		2		2		ns	1
Data-out low-impedance time		t_{LZ}	0		0		0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t_{HZ3}	2	5.4	2	5.4	2	6	2	6	ns	
Data-in setup time		t_{DS}	2		2		2		2		ns	
Data-in hold time		t_{DH}	1		1		1		1		ns	
Address setup time		t_{AS}	2		2		2		2		ns	
Address hold time		t_{AH}	1		1		1		1		ns	
CKE setup time		t_{CKS}	2		2		2		2		ns	
CKE hold time		t_{CKH}	1		1		1		1		ns	
CKE setup time (Power down exit)		t_{CKSP}	2		2		2		2		ns	
Command (/CS, /RAS, /CAS, /WE, DQM) setup time		t_{CMS}	2		2		2		2		ns	
Command (/CS, /RAS, /CAS, /WE, DQM) hold time		t_{CMH}	1		1		1		1		ns	

Notes 1. Output load



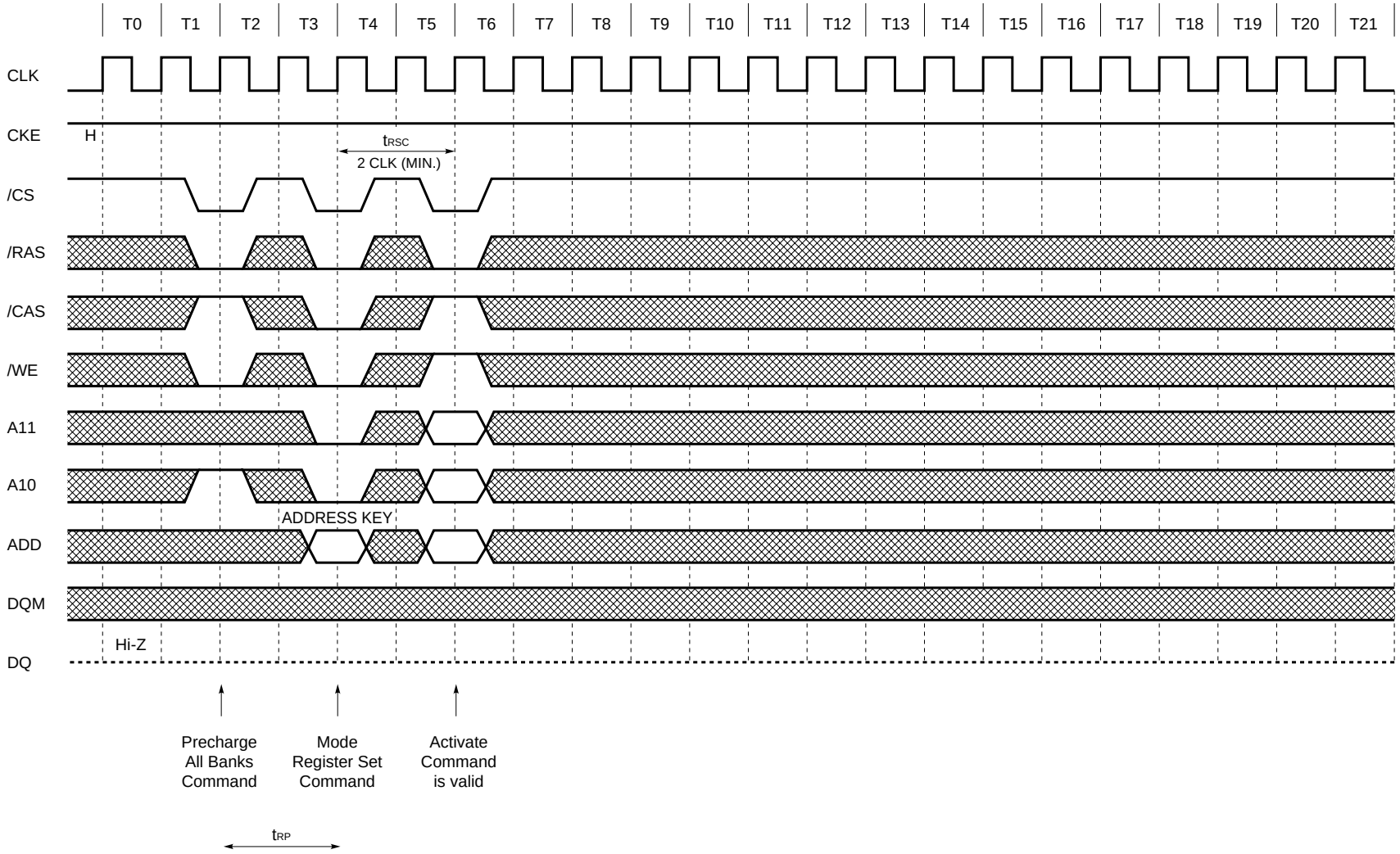
Asynchronous Characteristics

Parameter	Symbol	-A70		-A75		-A80		-A10		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
ACT to REF/ACT command period (operation)	t_{RC}	67.5		67.5		72		80		ns	
ACT to PRE command period	t_{RAS}	45	10,000	45	10,000	48	10,000	50	10,000	ns	
PRE to ACT command period	t_{RP}	21		22.5		24		30		ns	
Delay time ACT to READ/WRITE command	t_{RCD}	21		22.5		24		30		ns	
ACT (one) to ACT (another) command period	t_{RRD}	14		15		16		20		ns	
Data-in to PRE command period	t_{DPL}	2		2		2		2		CLK	
Mode register set cycle time	t_{RSC}	2		2		2		2		CLK	
Transition time	t_T	0.5	30	0.5	30	0.5	30	1	30	ns	
Refresh time (2,048 refresh cycles)	t_{REF}		32		32		32		32	ms	

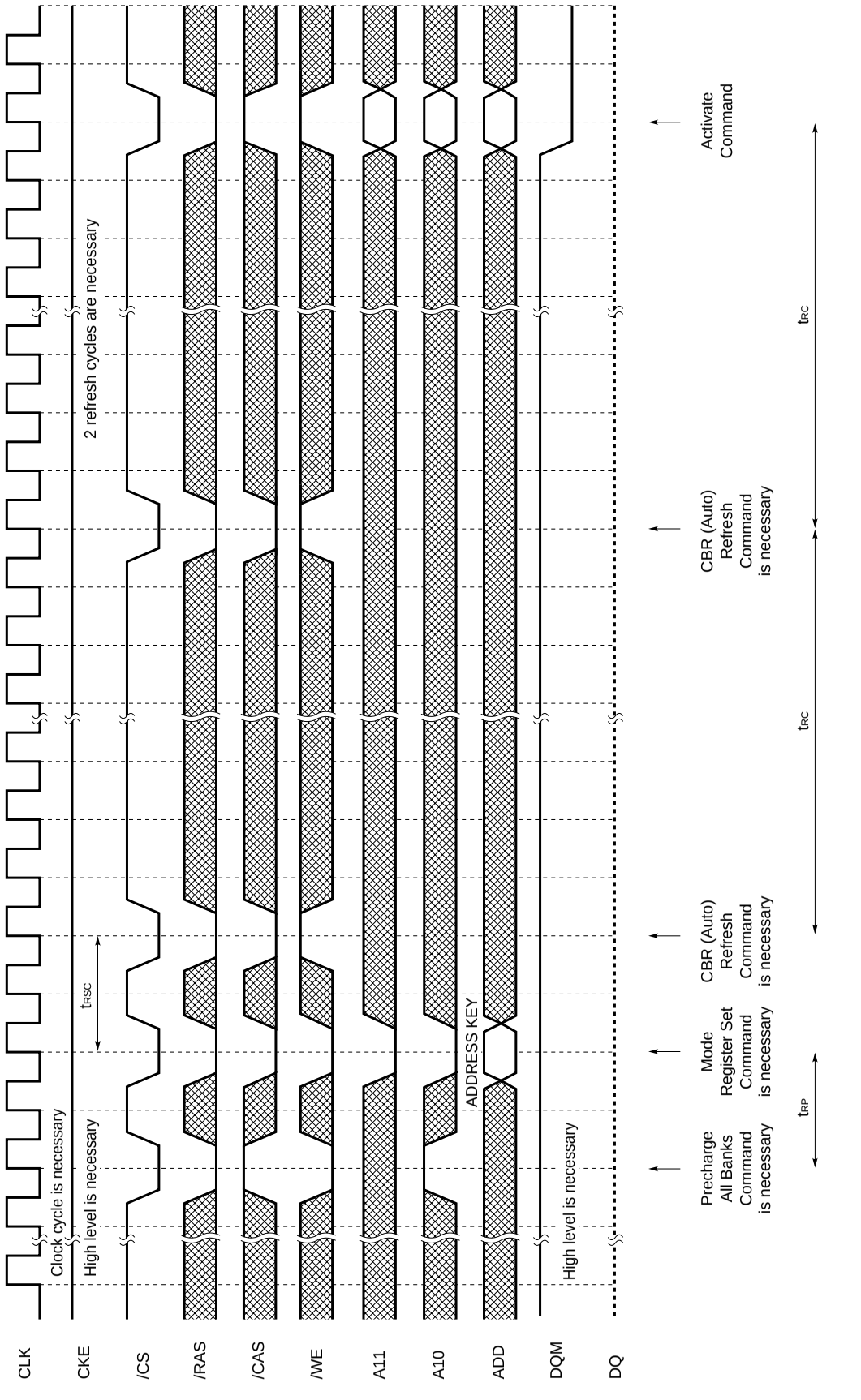
Relationship between Frequency and Latency

Speed version	-70	-75	-80	-10
Clock cycle time [ns]	7	7.5	8	10
Frequency [MHz]	143	133	125	100
/CAS latency	3	3	3	3
[t_{RCD}]	3	3	3	3
/RAS latency (/CAS latency + [t_{RCD}])	6	6	6	6
[t_{RC}]	10	9	9	8
[t_{RAS}]	7	6	6	5
[t_{RRD}]	2	2	2	2
[t_{RP}]	3	3	3	3
[t_{DPL}]	2	2	2	2
[t_{RSC}]	2	2	2	2

12.1 Mode Register Set

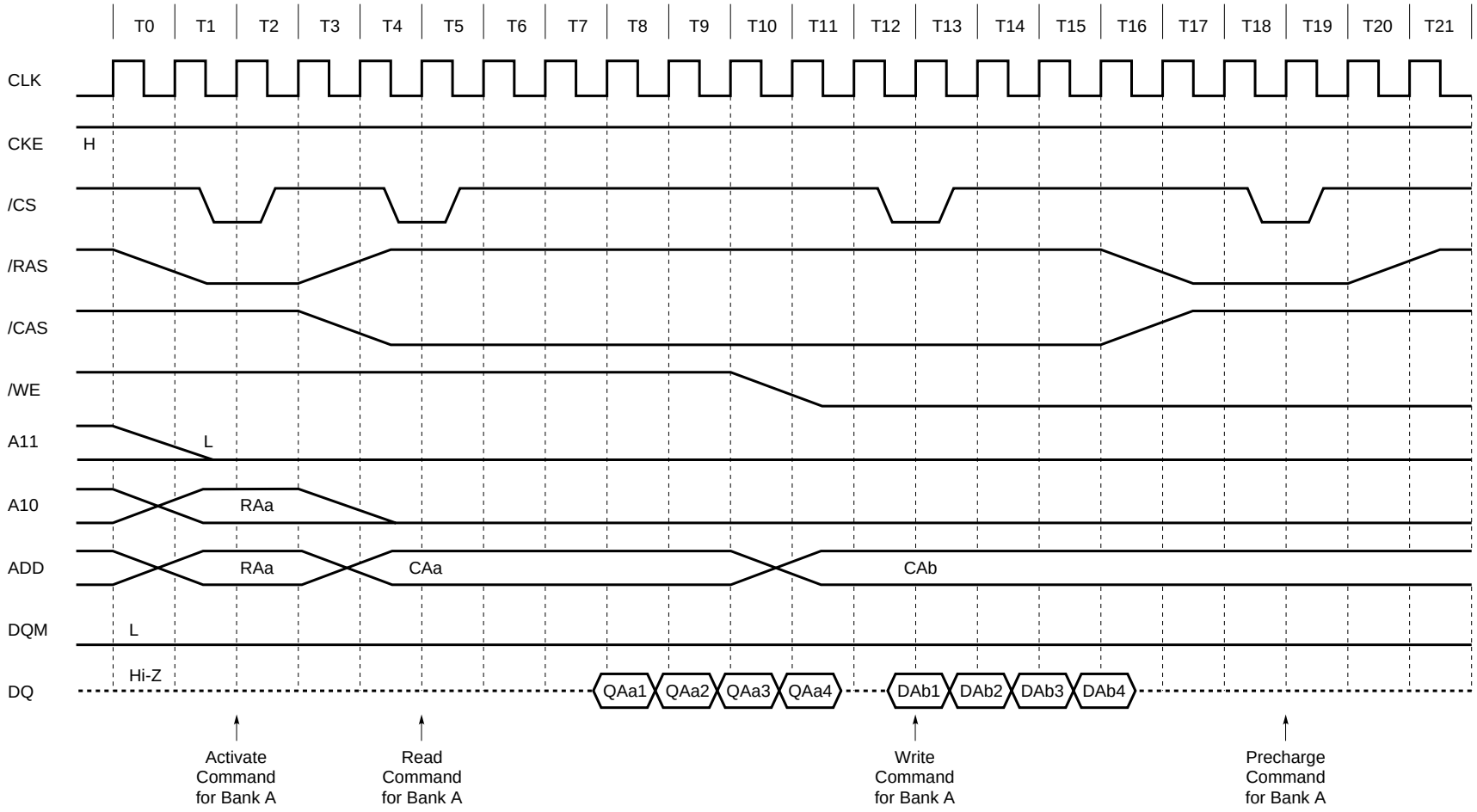


12.2 Power On Sequence and CBR (Auto) Refresh

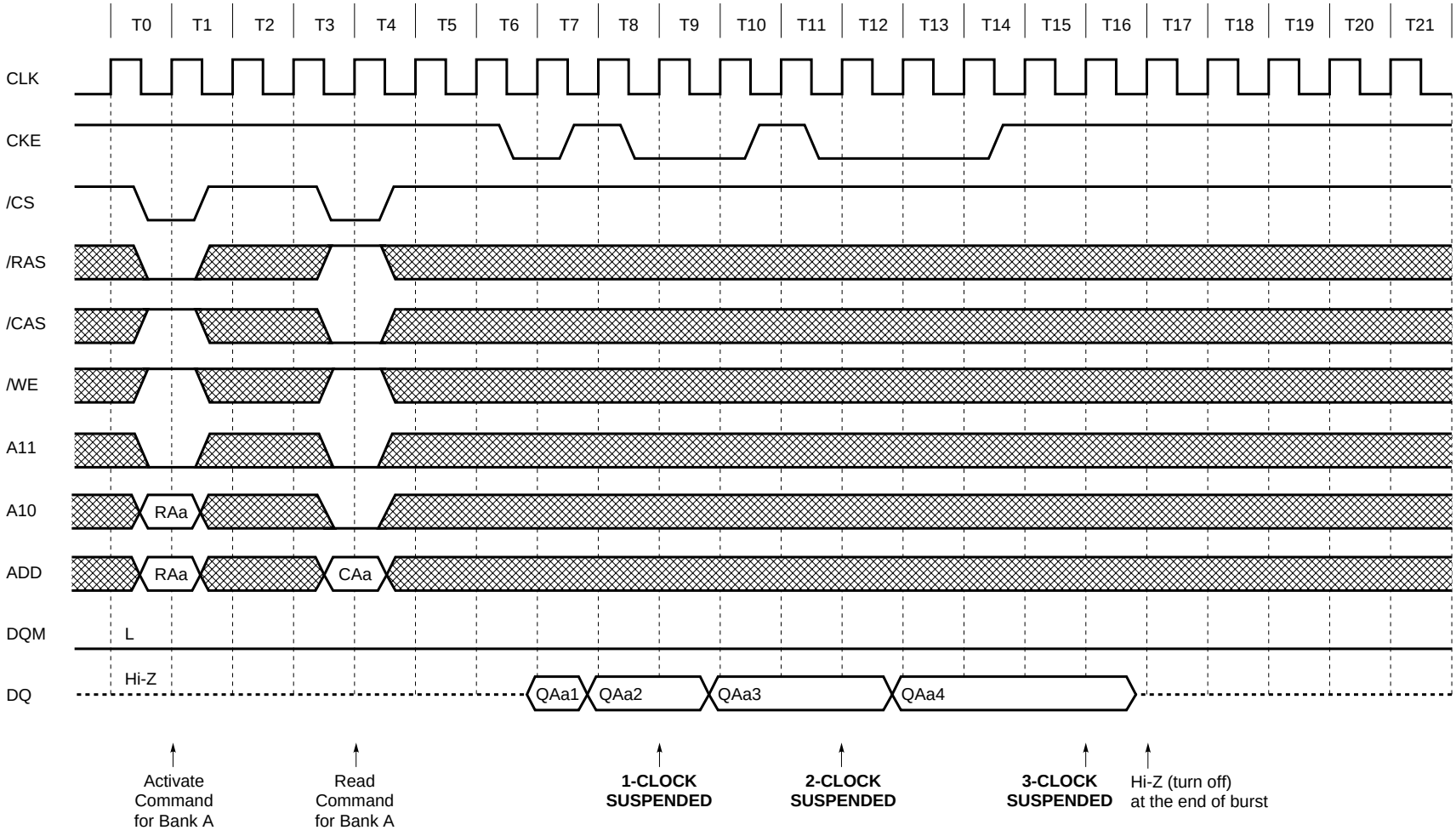


12.3 /CS Function (Burst Length = 4, /CAS Latency = 3)

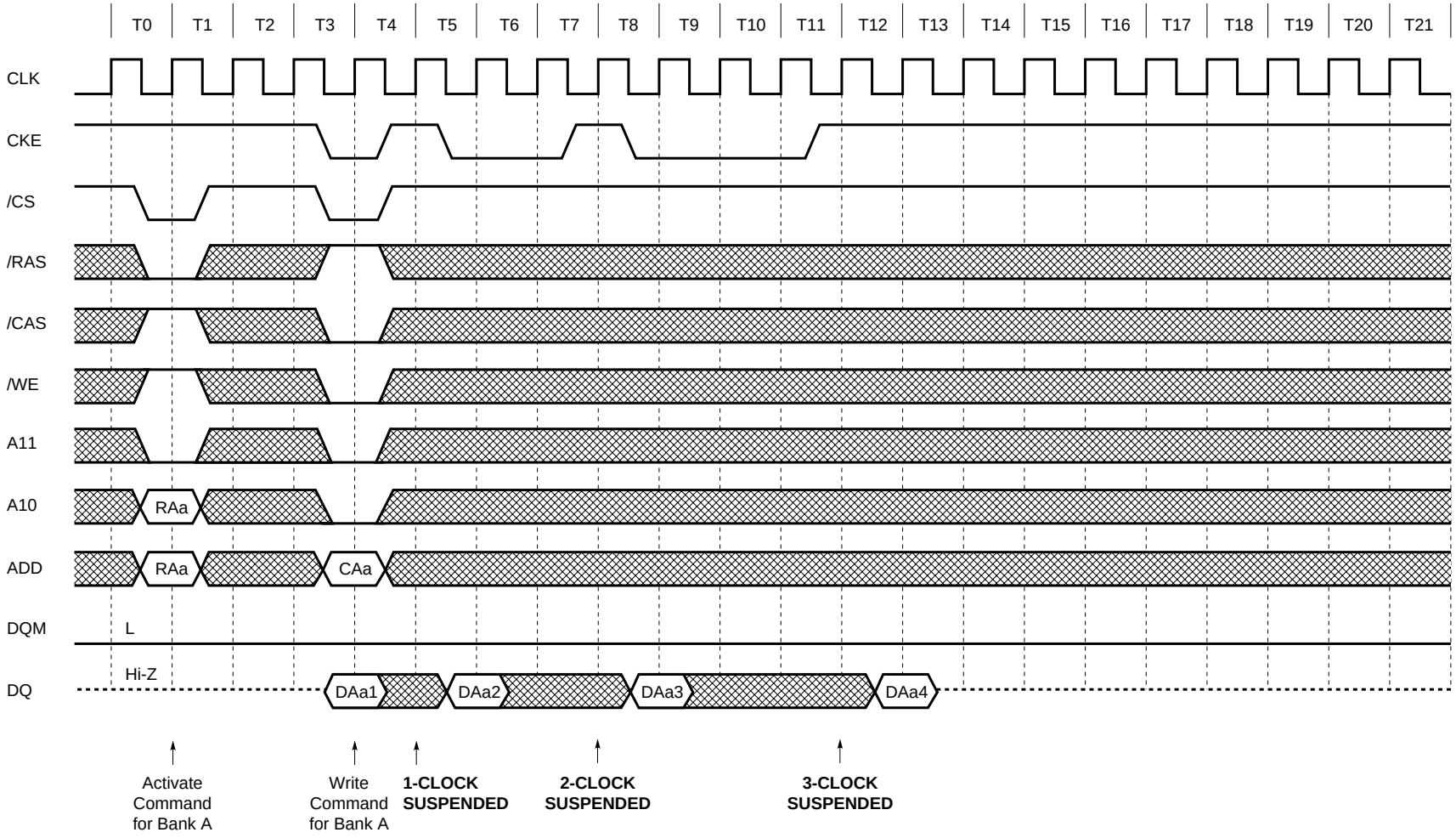
Only /CS signal needs to be issued at minimum rate



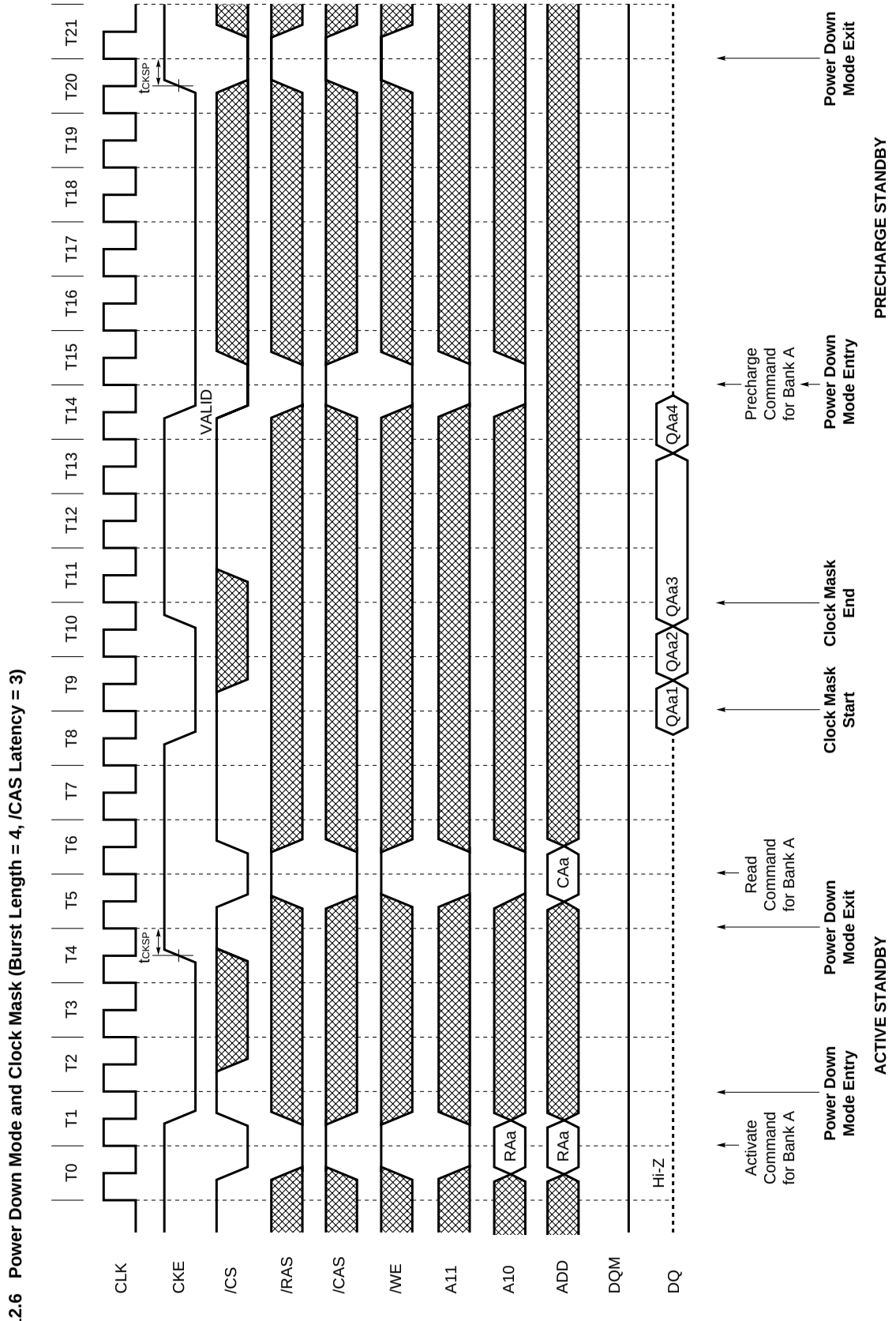
12.4 Clock Suspension during Burst Read (using CKE Function) (Burst Length = 4, /CAS Latency = 3)



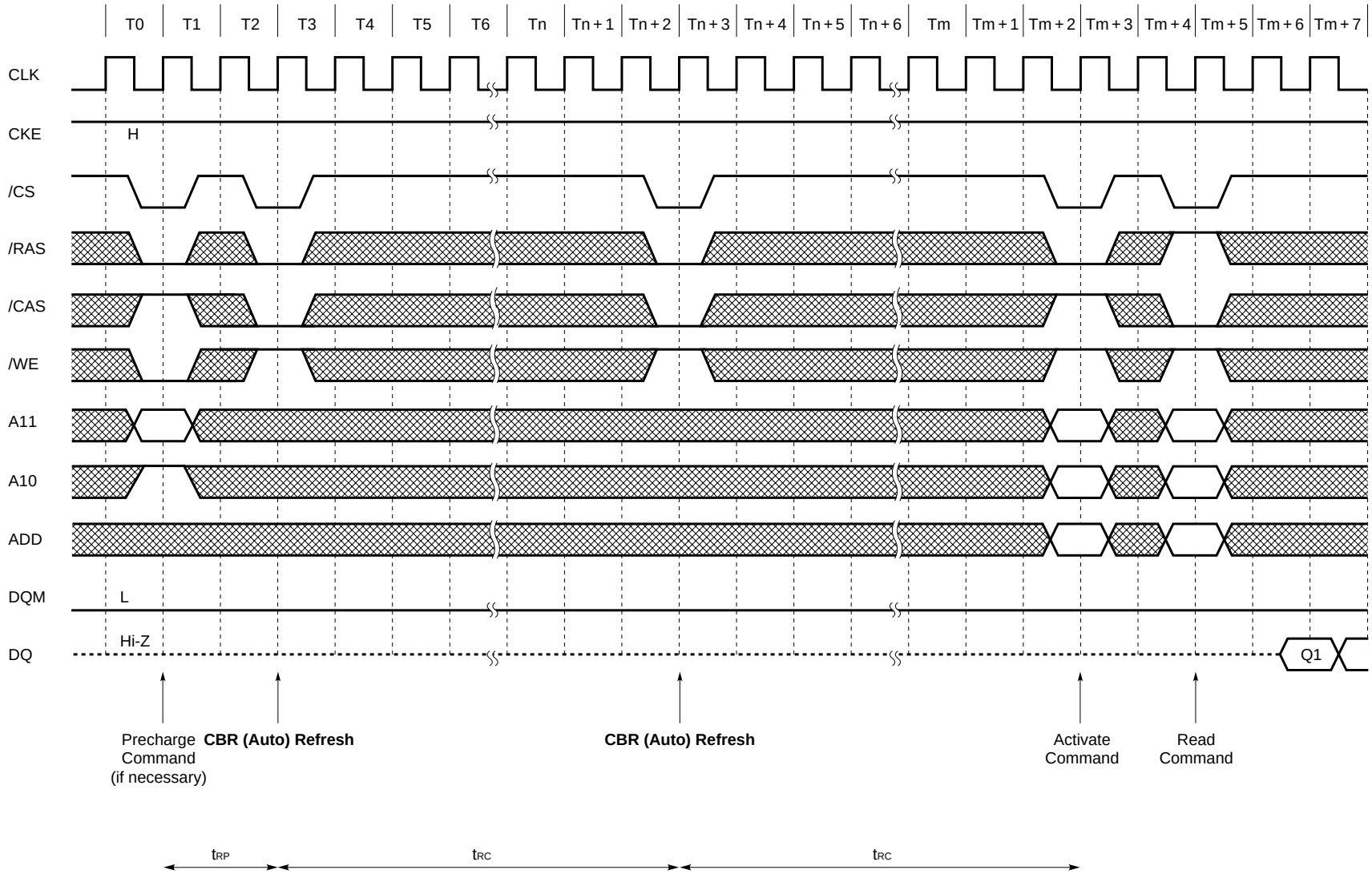
12.5 Clock Suspension during Burst Write (using CKE Function) (Burst Length = 4, /CAS Latency = 3)



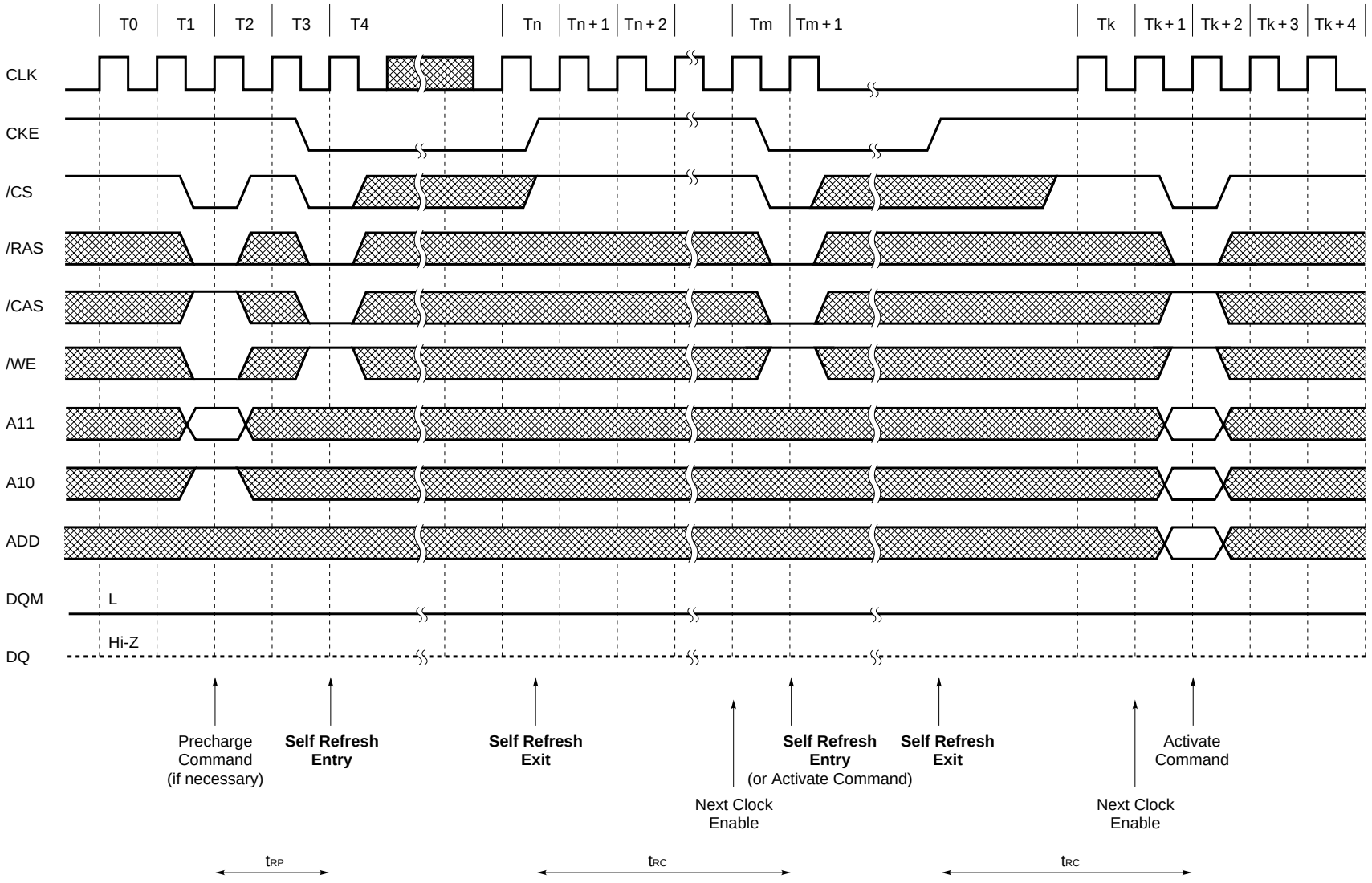
12.6 Power Down Mode and Clock Mask (Burst Length = 4, /CAS Latency = 3)



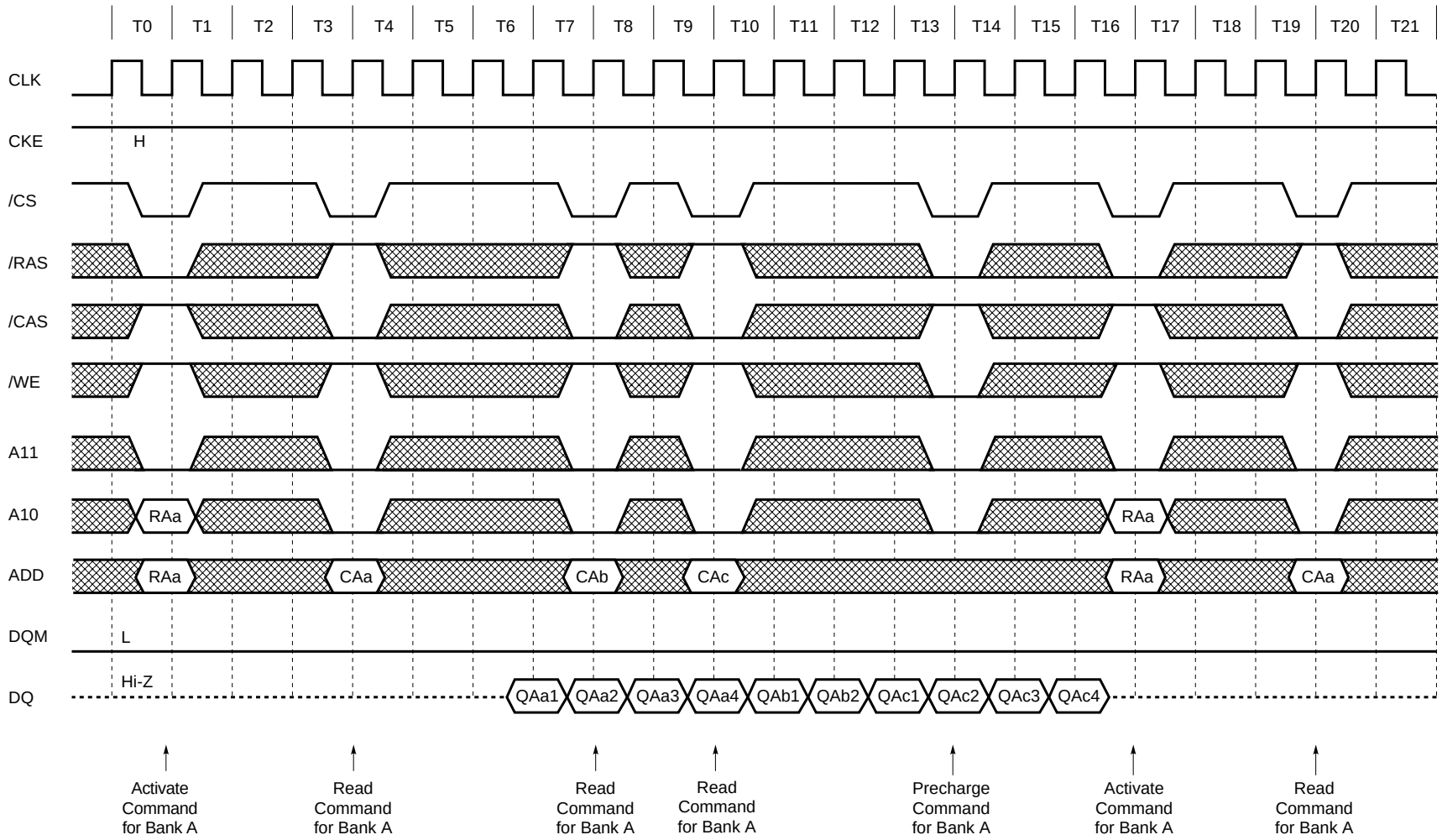
12.7 CBR (Auto) Refresh



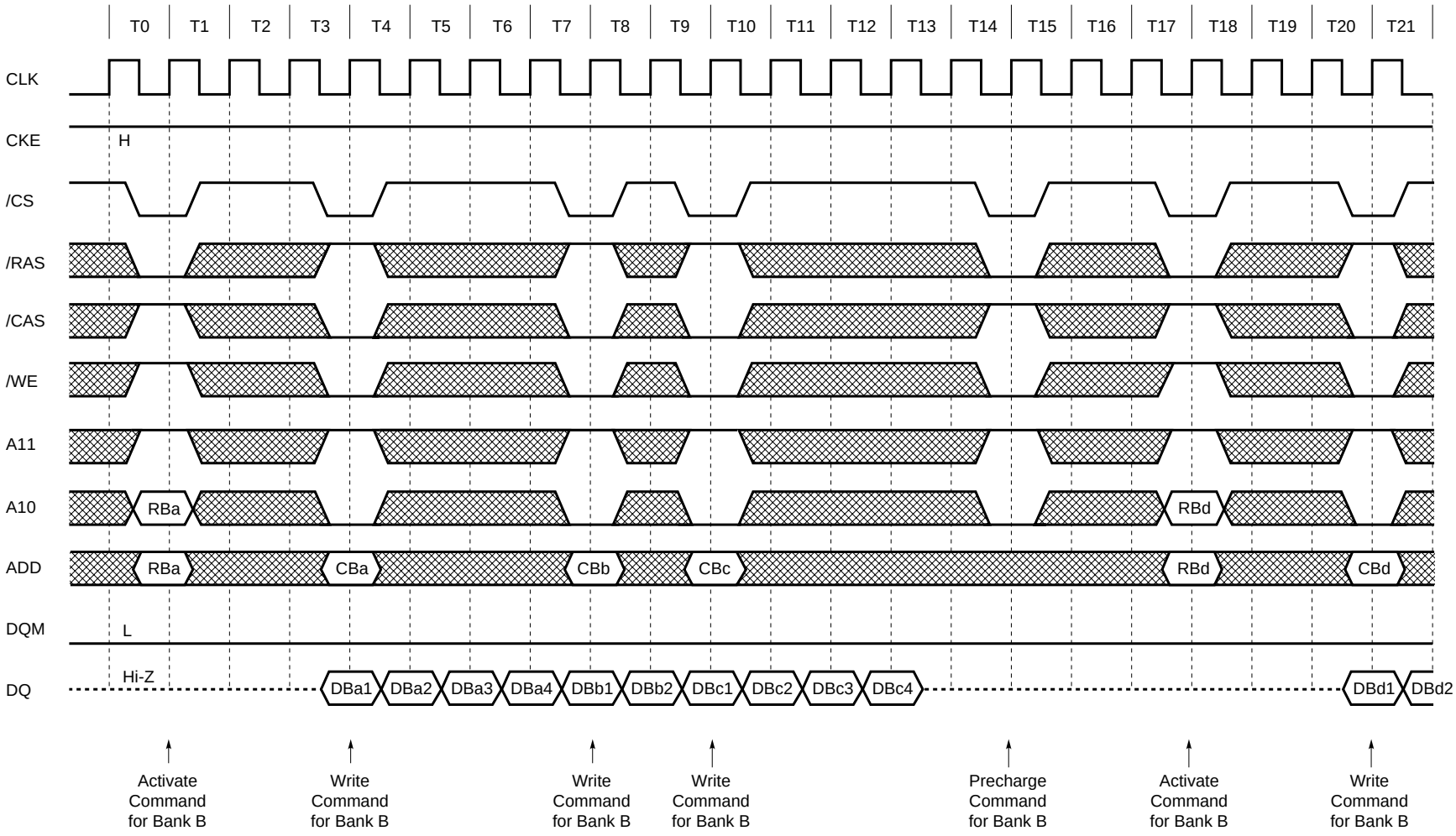
12.8 Self Refresh (Entry and Exit)



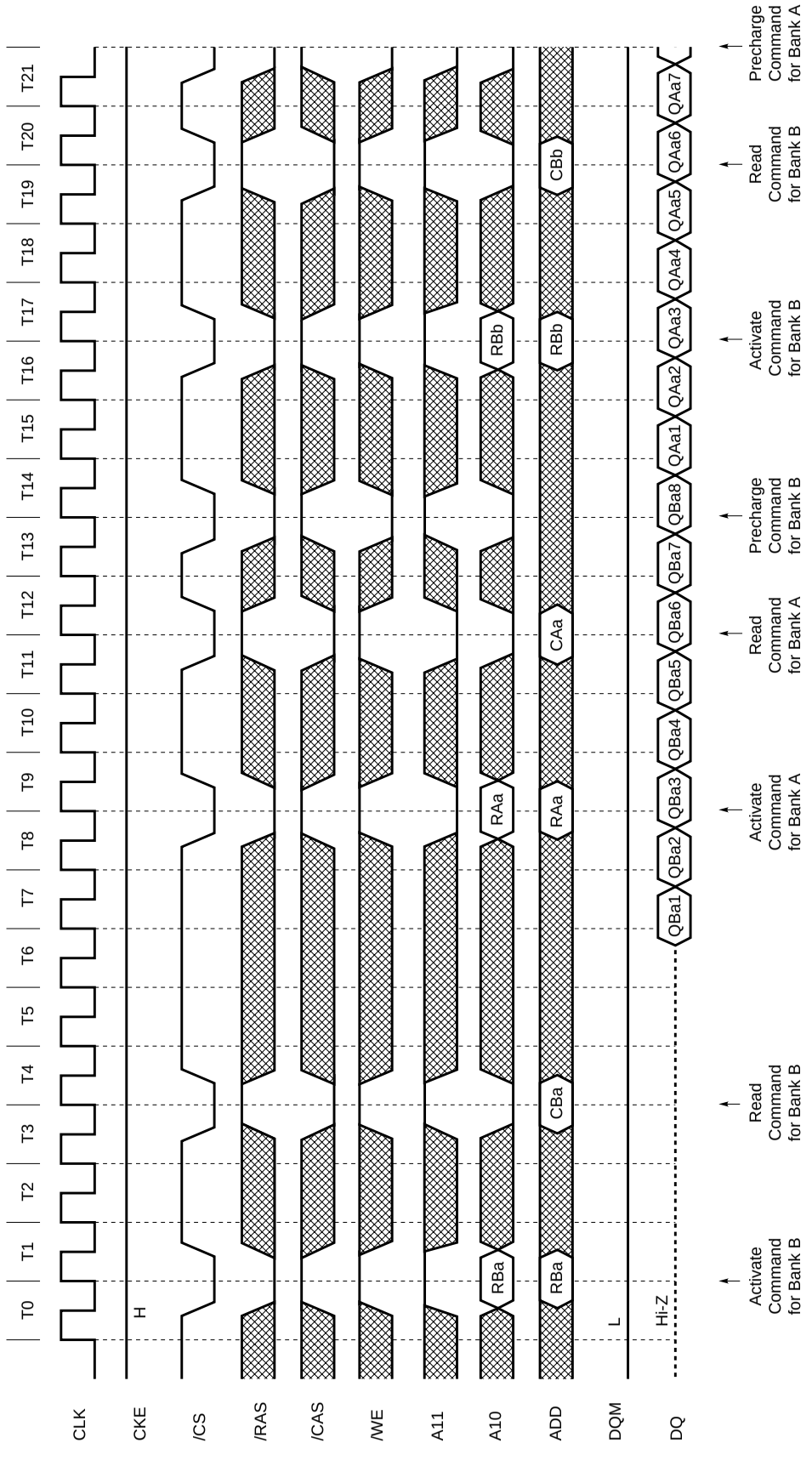
12.9 Random Column Read (Page with Same Bank) (Burst Length = 4, /CAS Latency = 3)



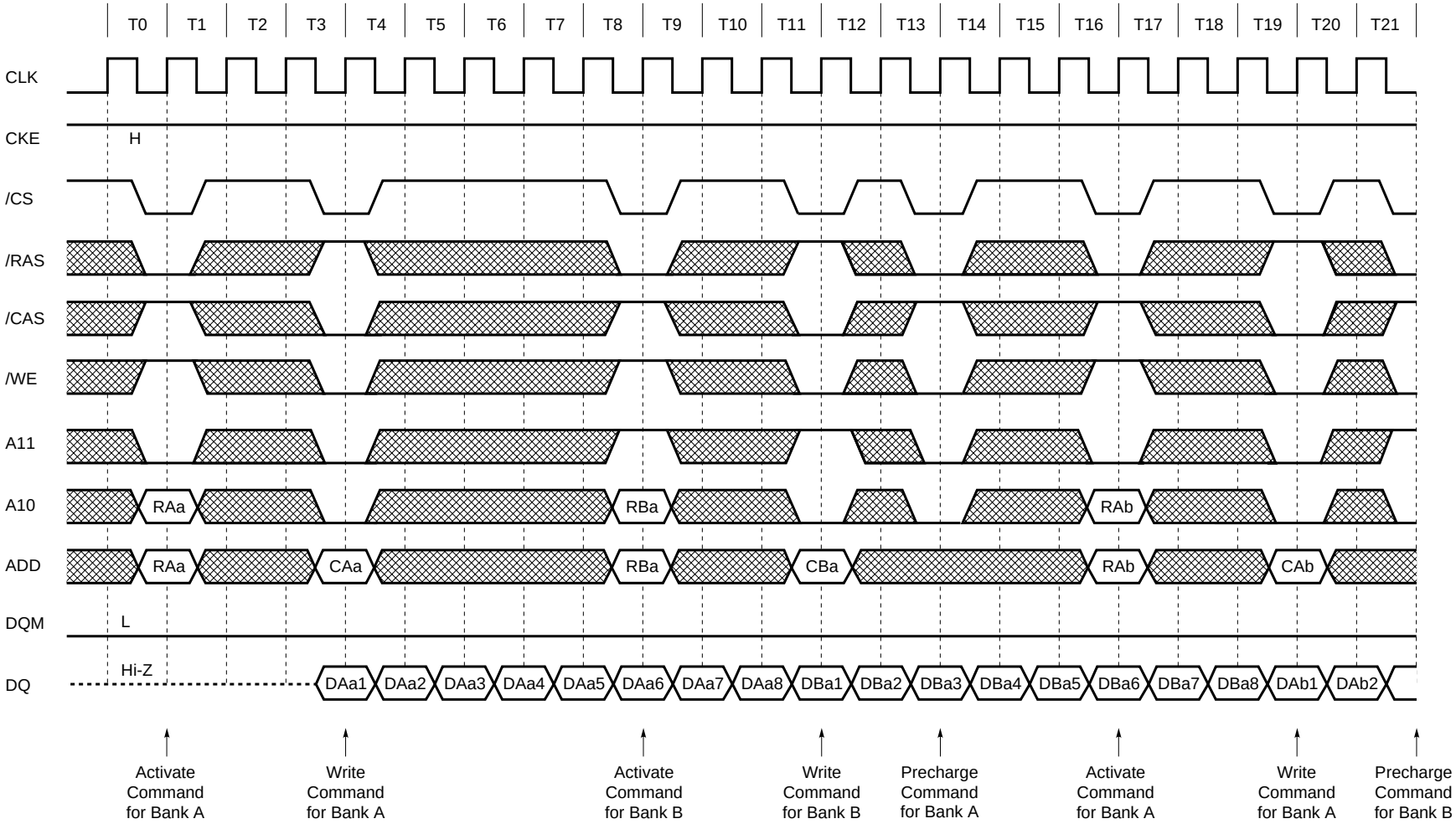
12.10 Random Column Write (Page with Same Bank) (Burst Length = 4, /CAS Latency = 3)



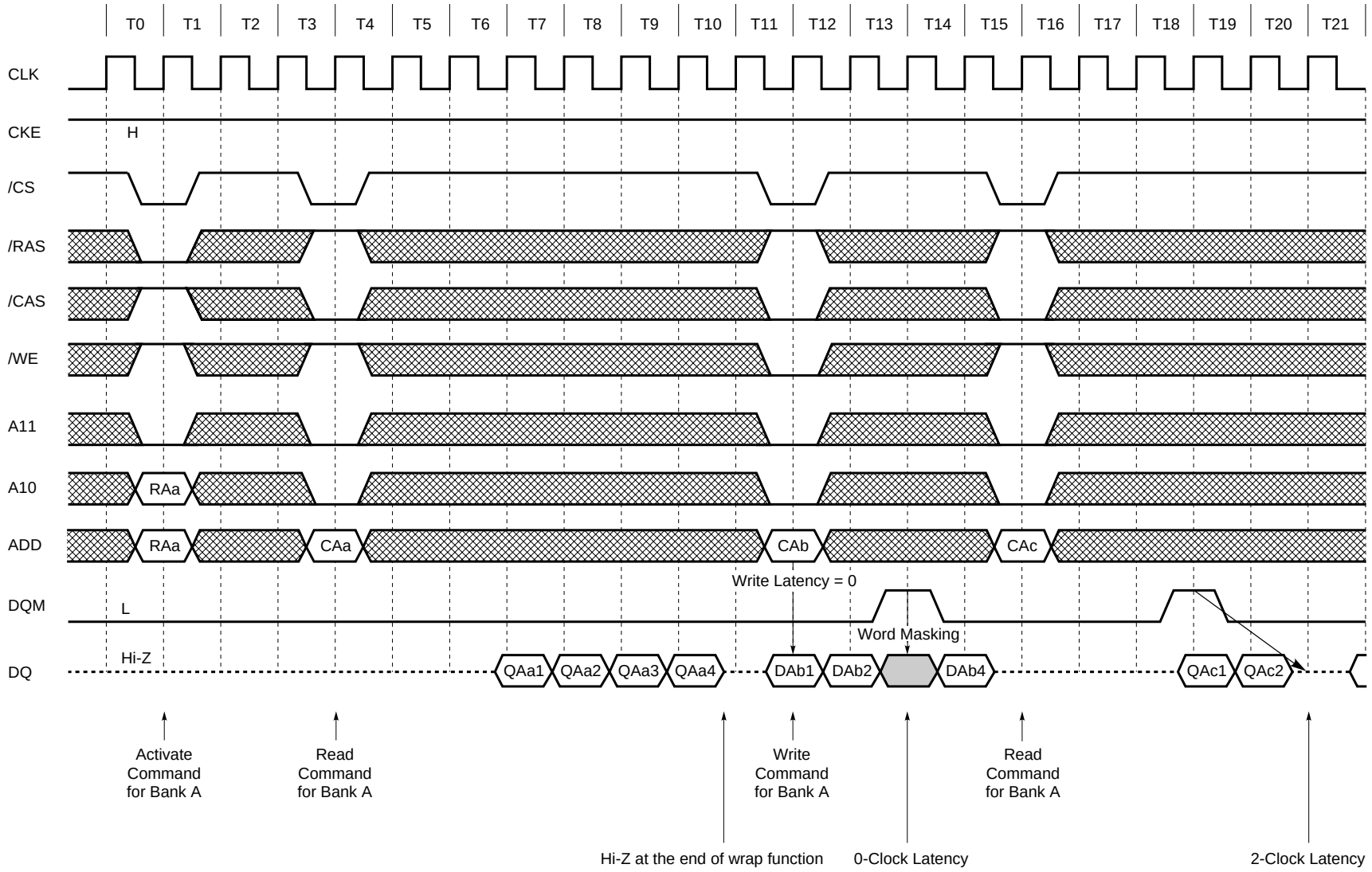
12.11 Random Row Read (Ping-Pong Banks) (Burst Length = 8, /CAS Latency = 3)



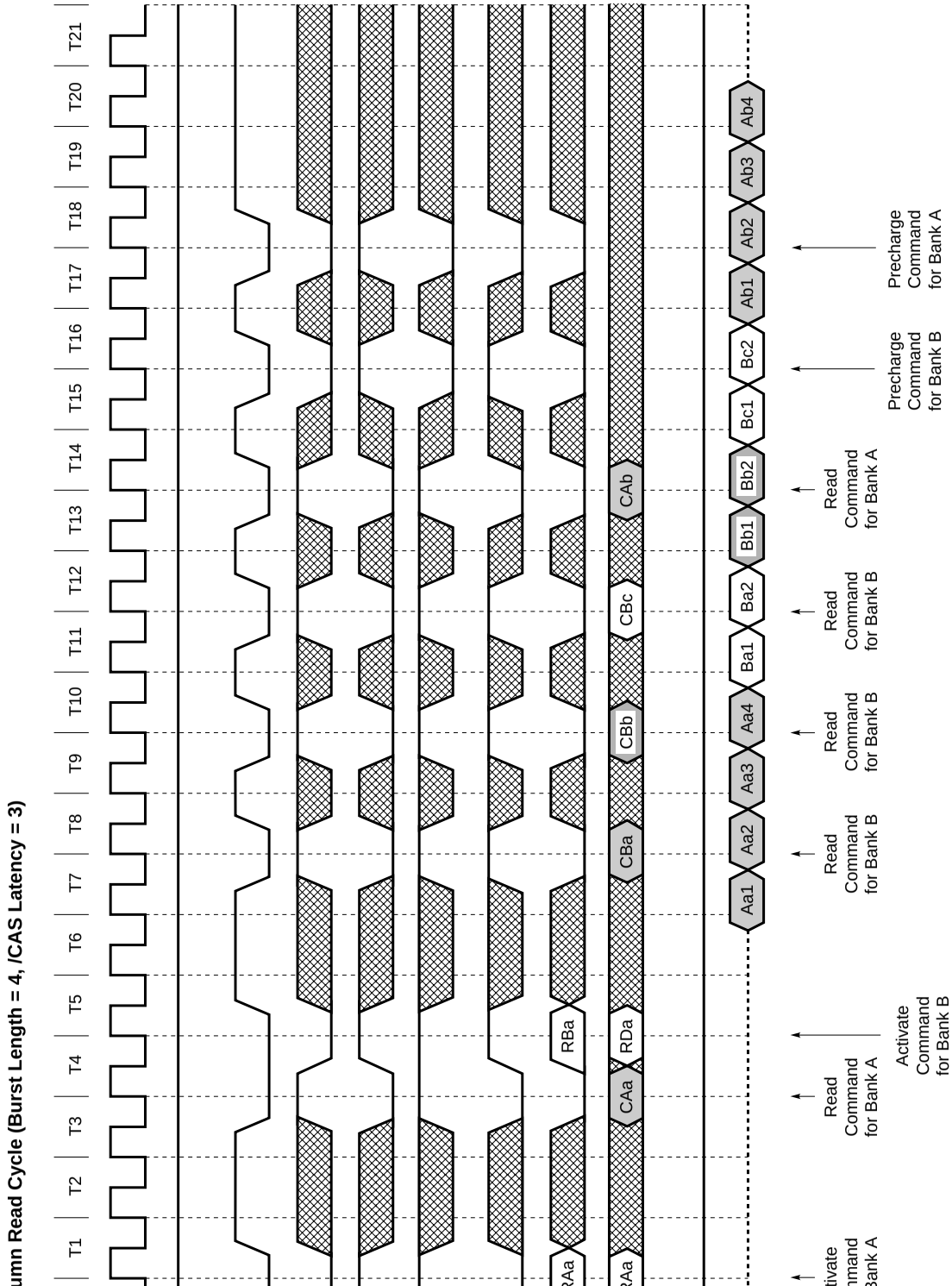
12.12 Random Row Write (Ping-Pong Banks) (Burst Length = 8, /CAS Latency = 3)



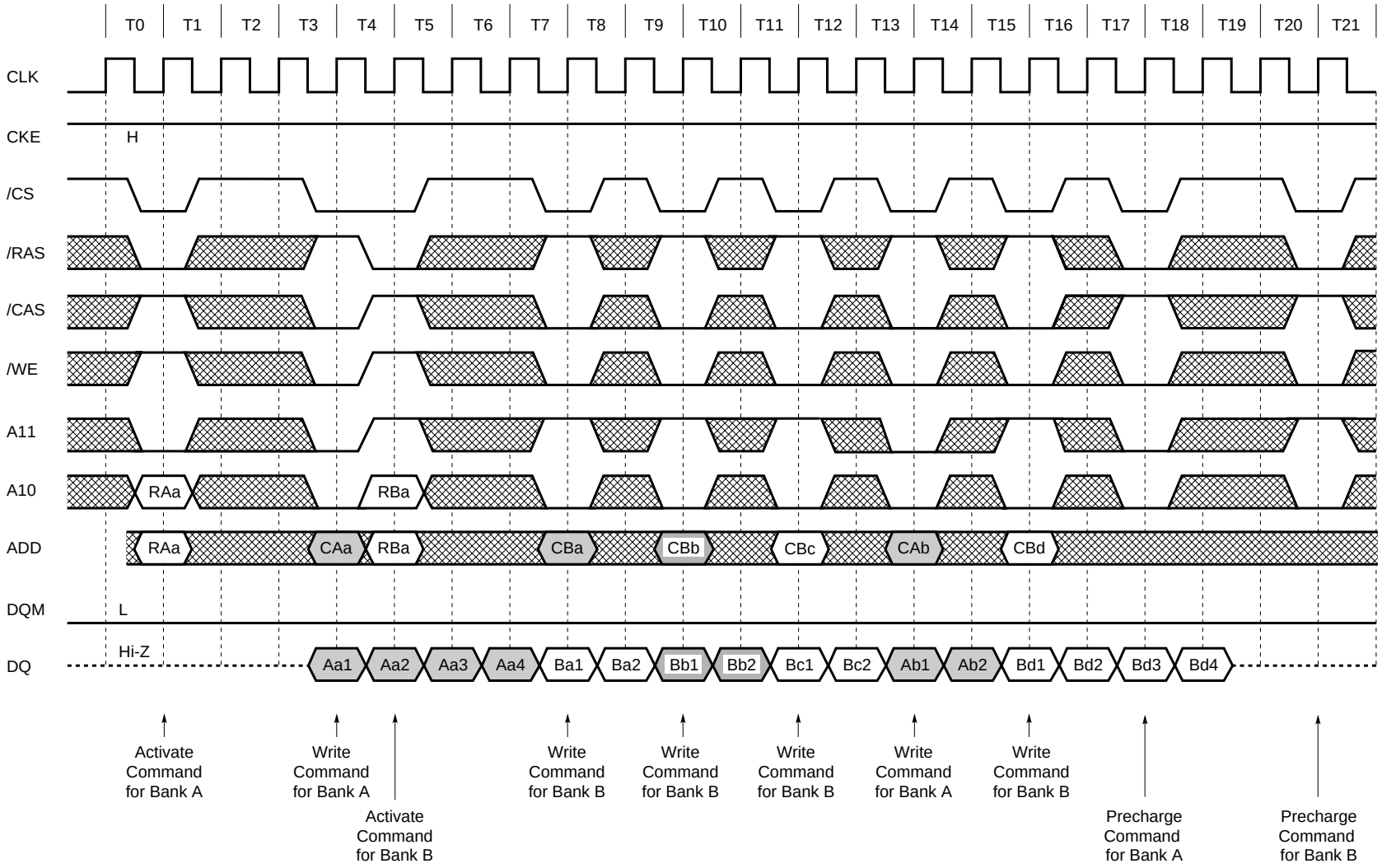
12.13 Read and Write (Burst Length = 4, /CAS Latency = 3)



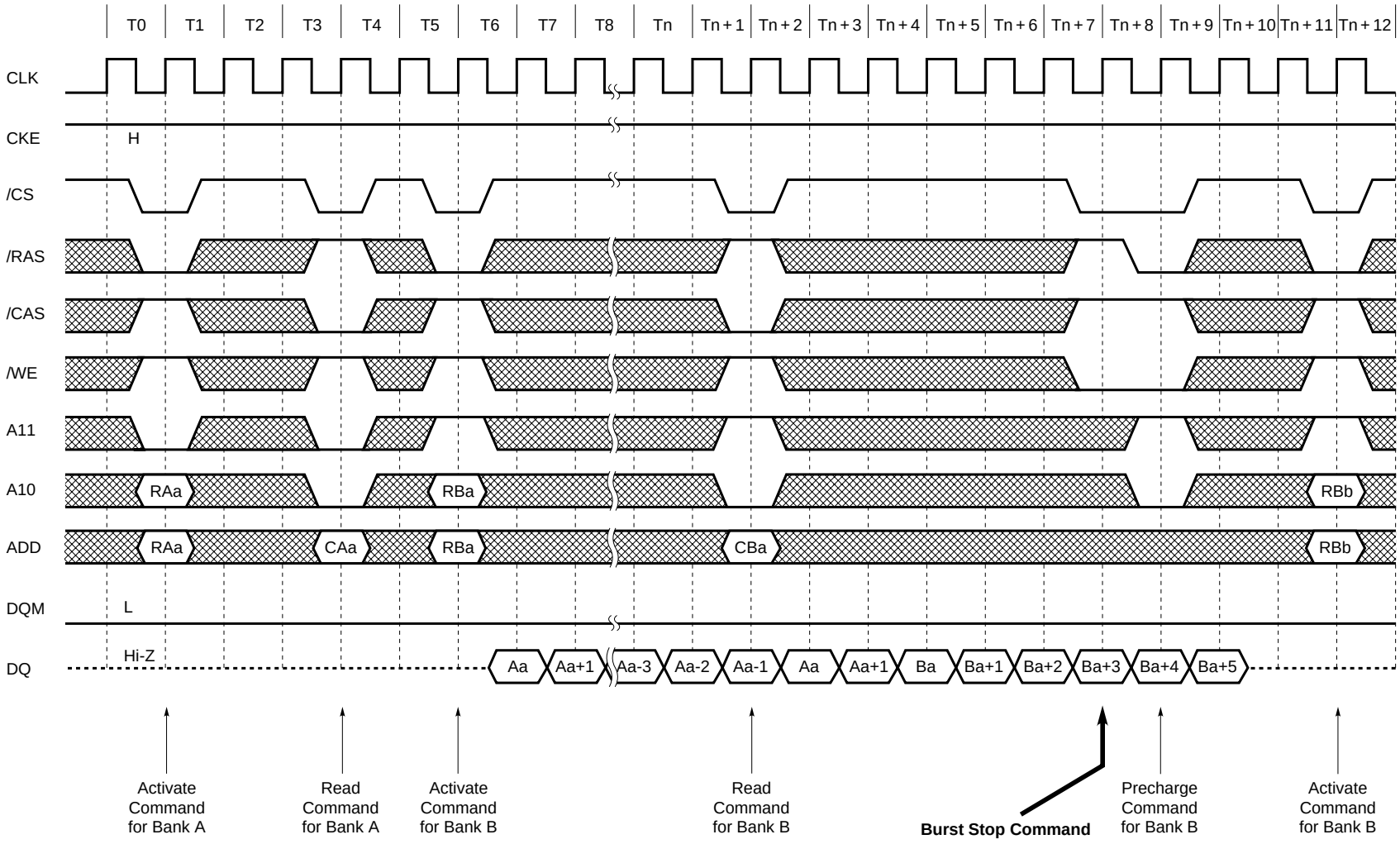
12.14 Interleaved Column Read Cycle (Burst Length = 4, /CAS Latency = 3)



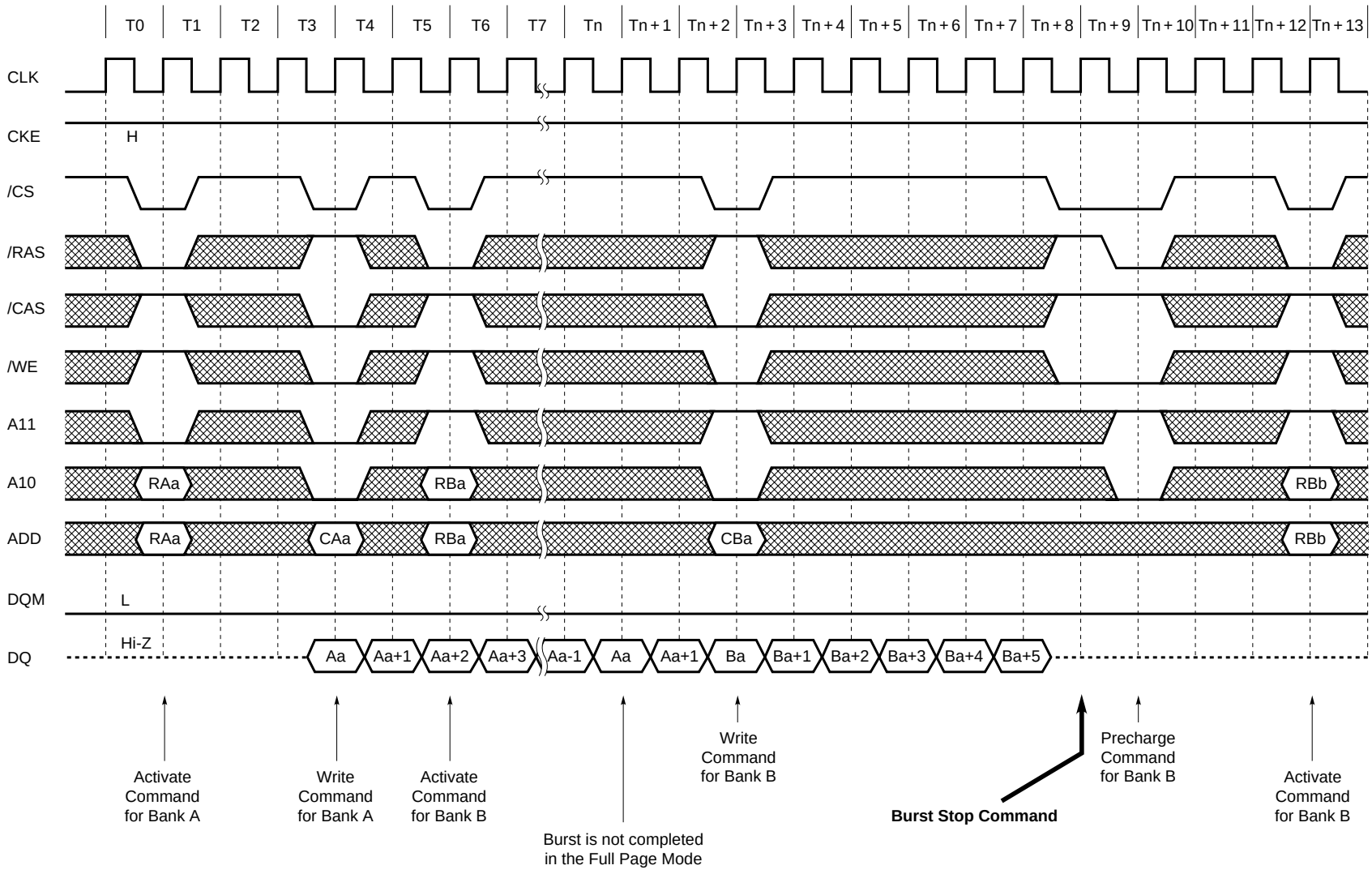
12.15 Interleaved Column Write Cycle (Burst Length = 4, /CAS Latency = 3)



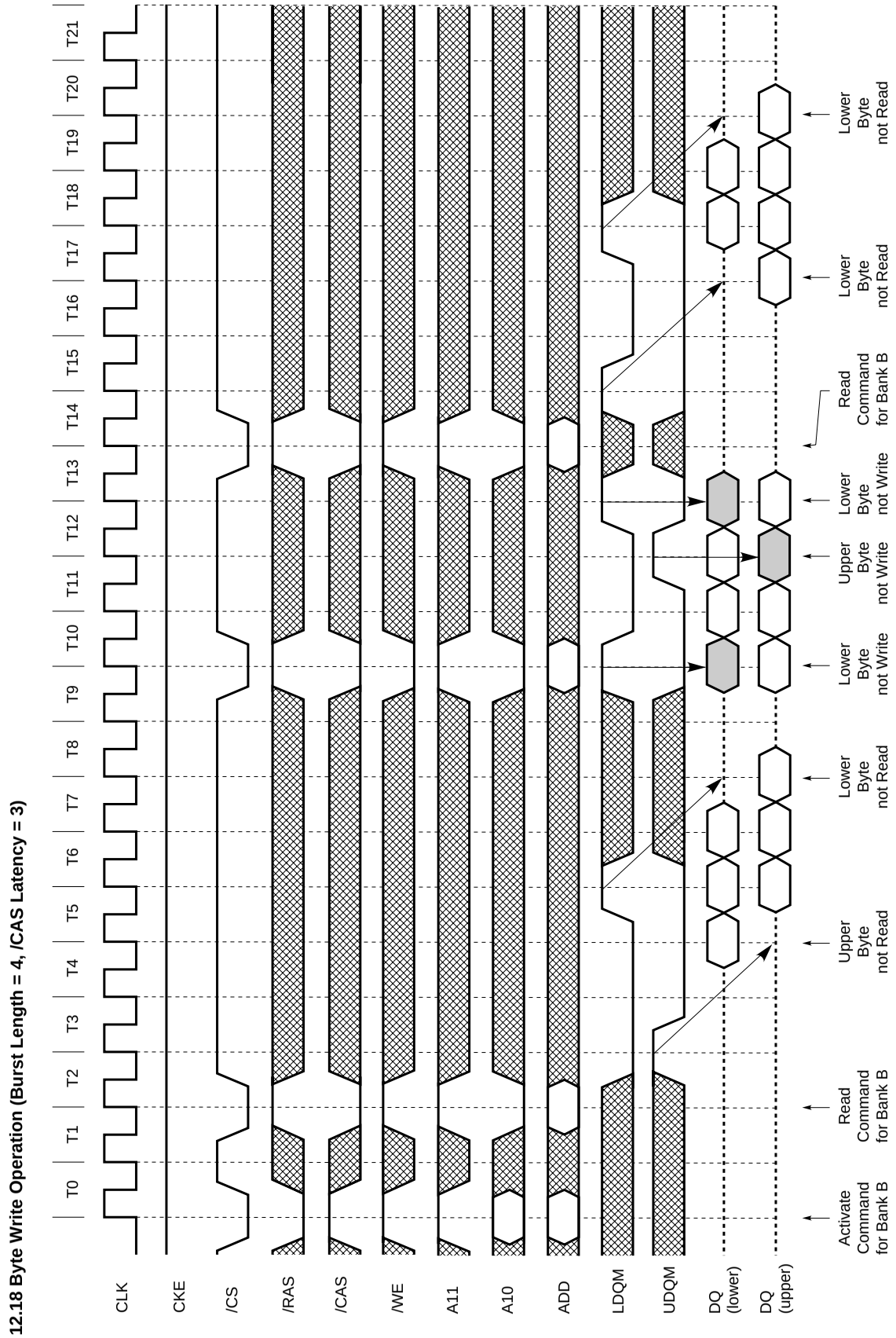
12.16 Full Page Read Cycle (/CAS latency = 3)



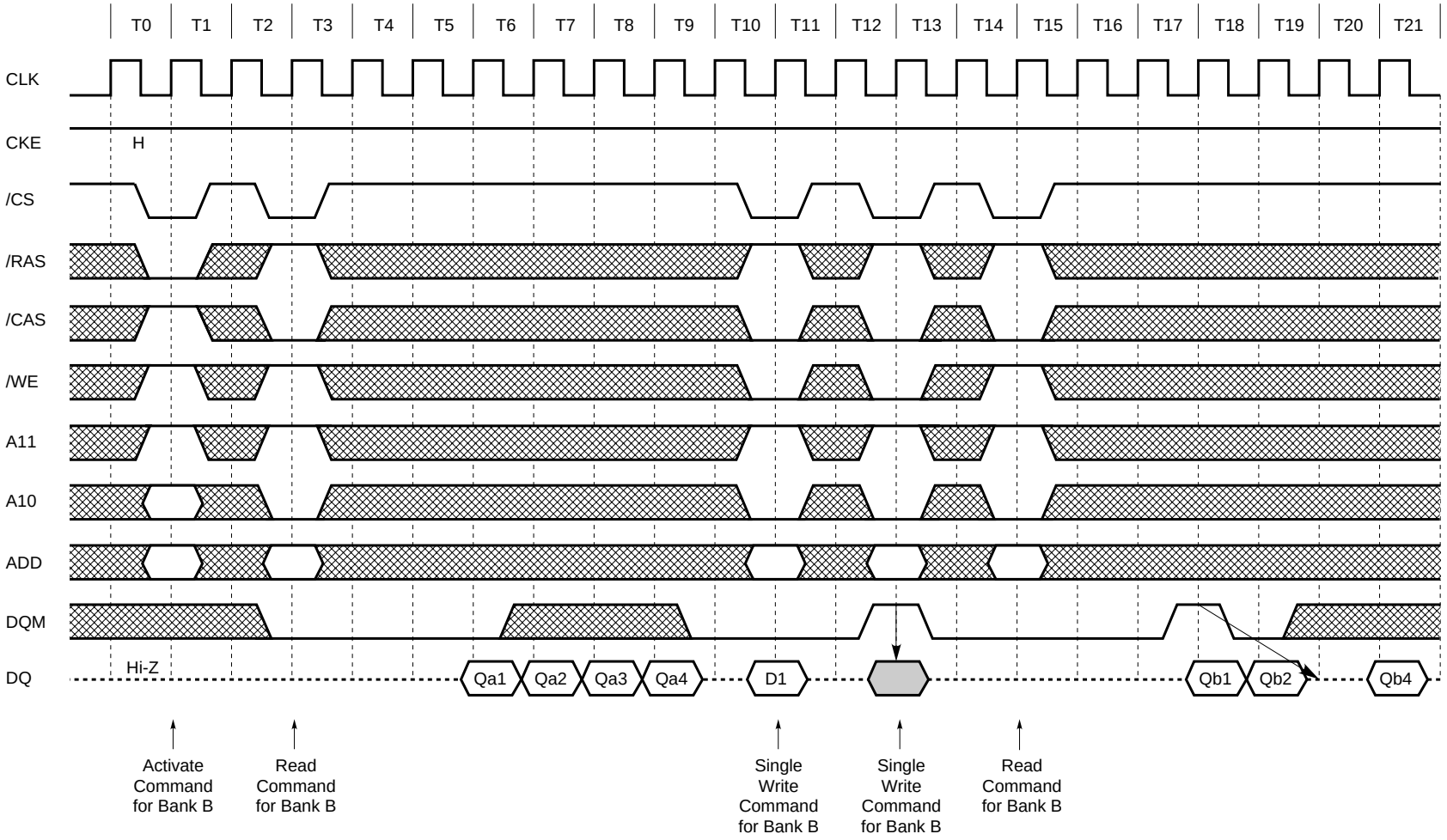
12.17 Full Page Write Cycle (/CAS Latency = 3)



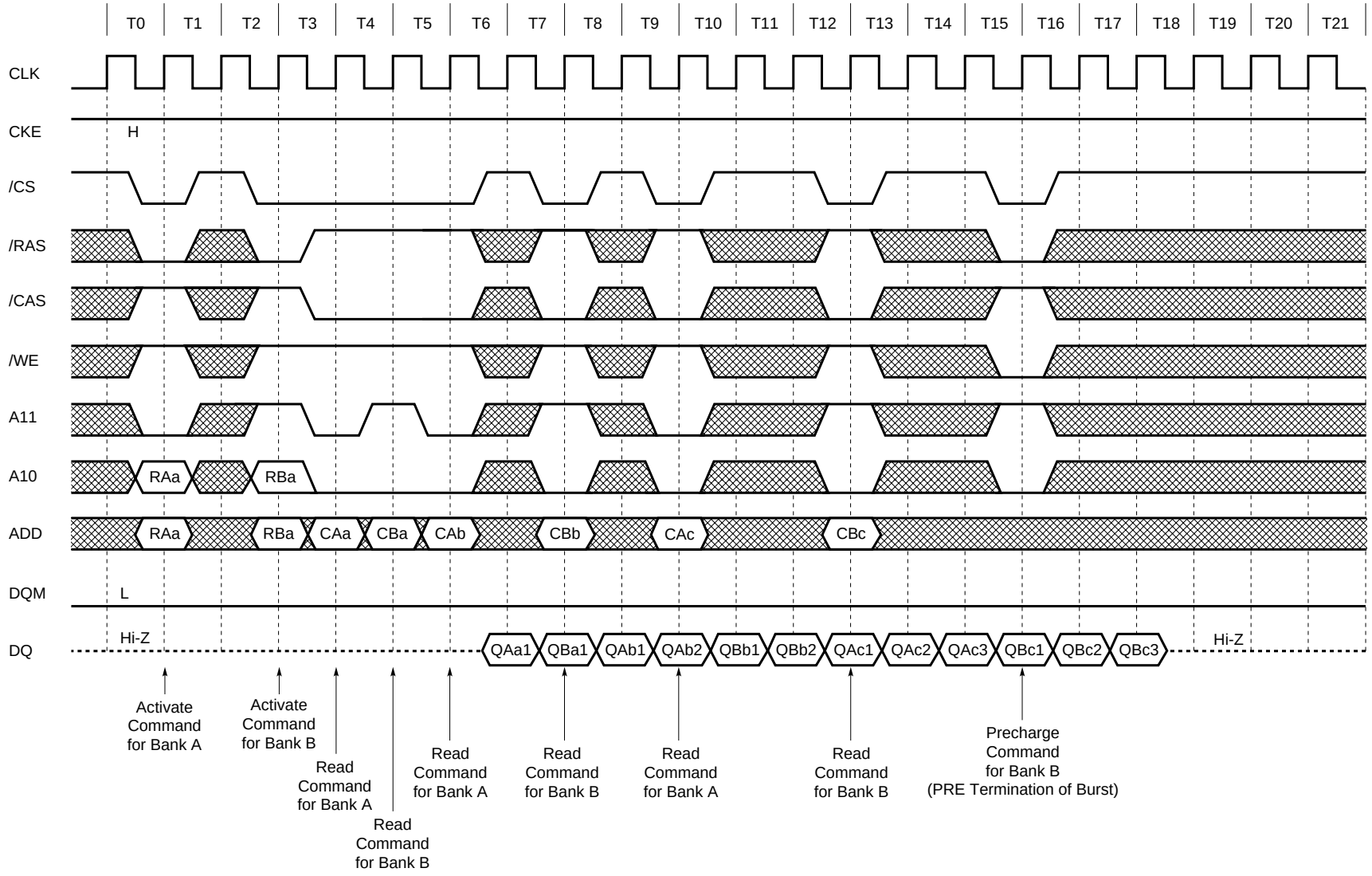
12.18 Byte Write Operation (Burst Length = 4, /CAS Latency = 3)



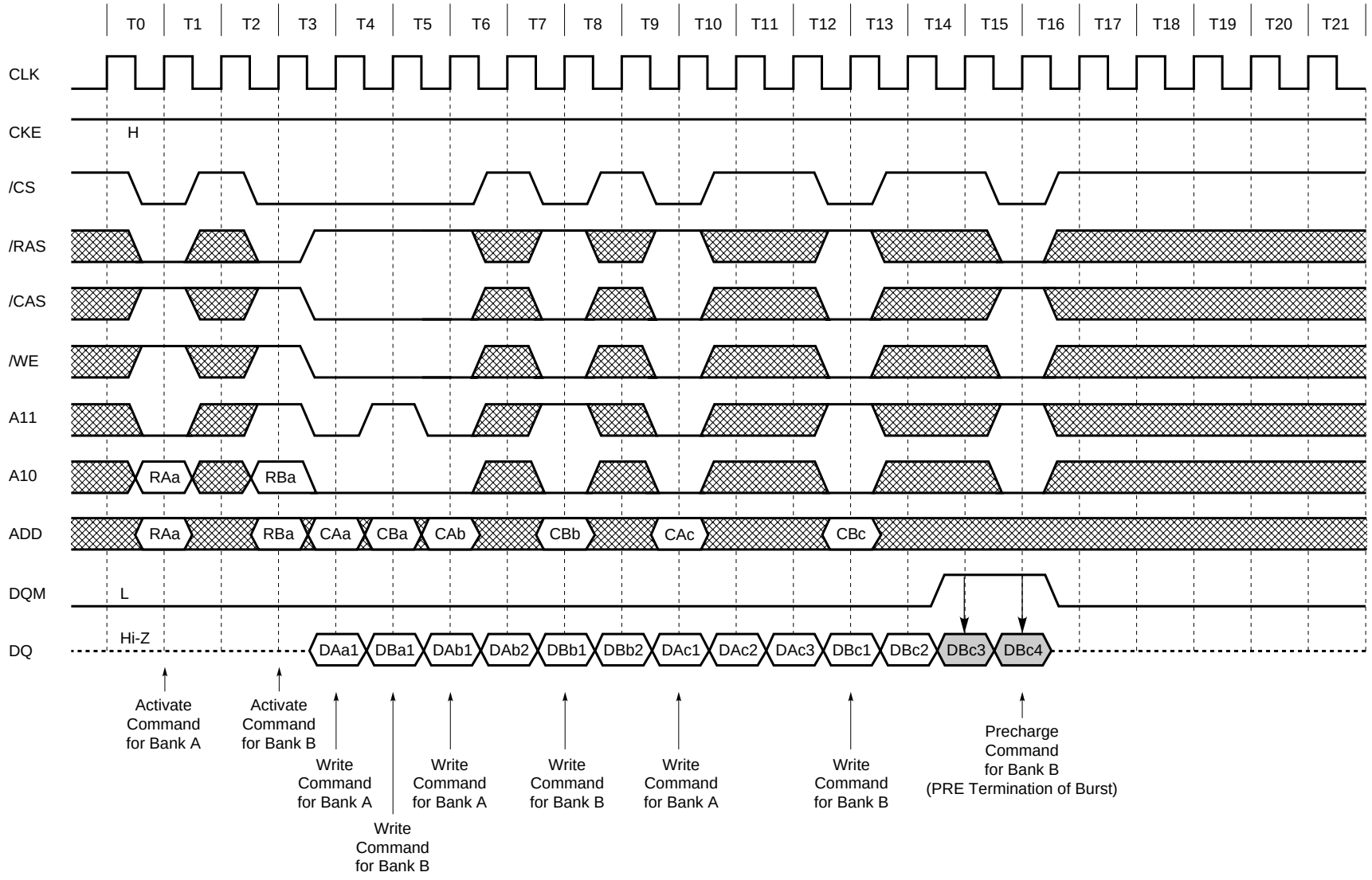
12.19 Burst Read and Single Write (Option) (Burst Length = 4, /CAS Latency = 3)



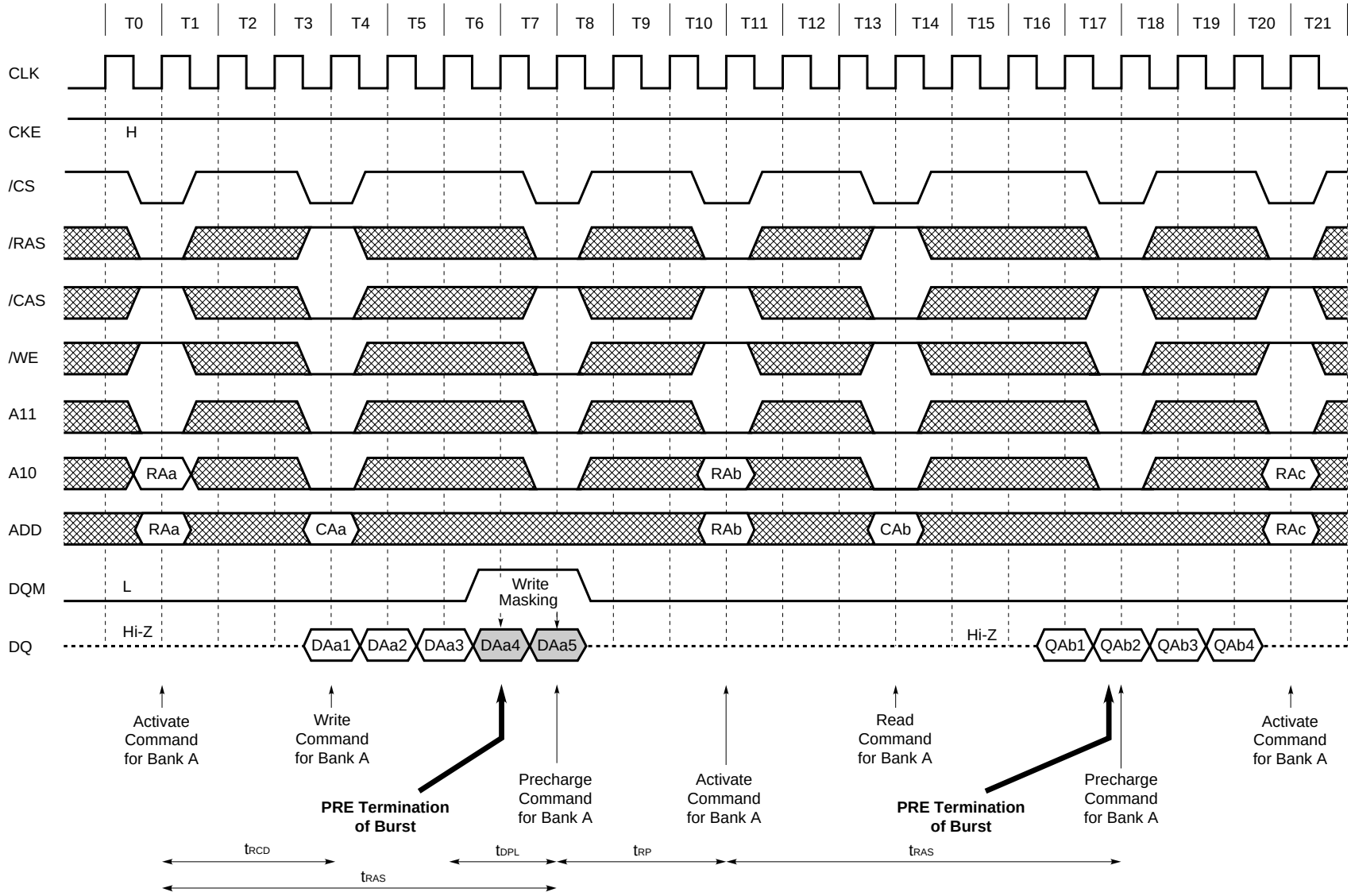
12.20 Full Page Random Column Read (Burst Length = Full Page, /CAS Latency = 3)



12.21 Full Page Random Column Write (Burst Length = Full Page, /CAS Latency = 3)

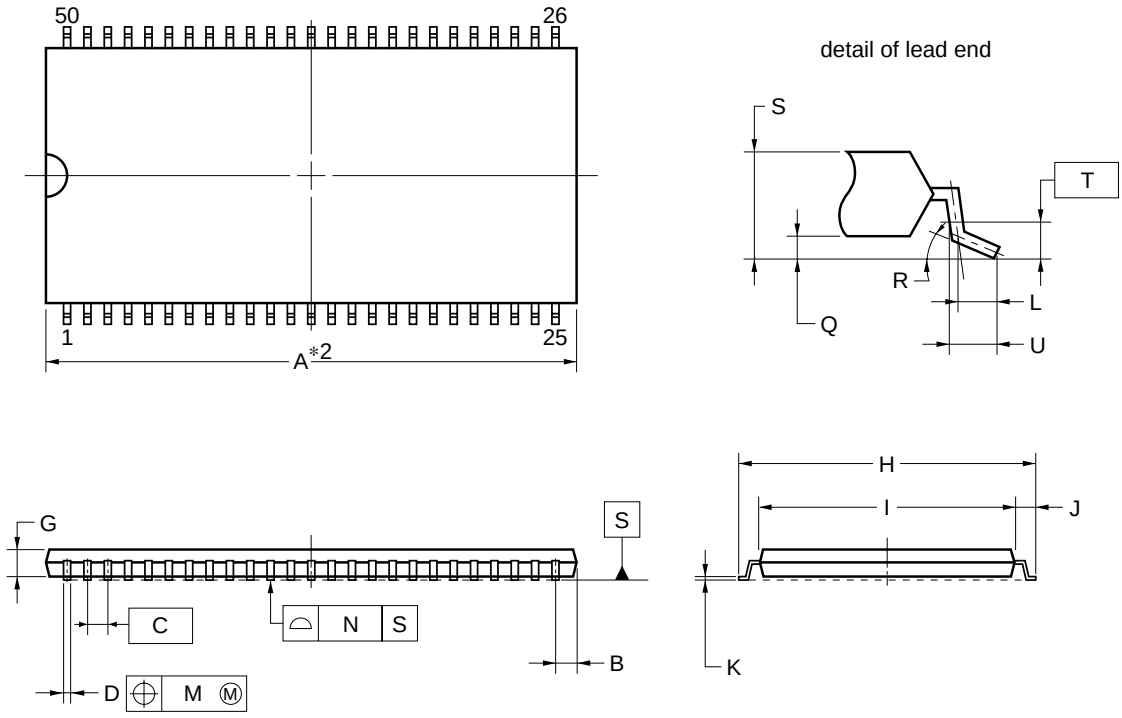


12.22 PRE (Precharge) Termination of Burst (Burst Length = 8, /CAS Latency = 3)



13. Package Drawing

50-PIN PLASTIC TSOP(II) (10.16 mm (400))



NOTES

1. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.
2. ∗2. Dimension “A” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

ITEM	MILLIMETERS
A	20.86±0.04
B	1.0 MAX.
C	0.8 (T.P.)
D	$0.32^{+0.08}_{-0.07}$
G	1.0±0.05
H	11.76±0.2
I	10.11±0.04
J	0.825±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5
M	0.13
N	0.10
Q	0.1±0.05
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.
T	0.25 (T.P.)
U	0.60±0.15

S50G5-80-9NF-1

14. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD4516161D.

Type of Surface Mount Device

μPD4516161DG5 : 50-pin Plastic TSOP (II) (10.16 mm(400))

15. Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
NEC Corporation (M14888E)				
1st edition / May 2000	-	-	-	-
2nd edition / Dec. 2000	p.1	p.1	Addition	-A70
	p.2	p.2		
	p.30	p.30		
	p.32	p.32		
	p.33	p.33		
Elpida Memory, Inc. (E0143N)				
Ver.1.0 / May. 2001	-	-	-	Republished by Elpida Memory, Inc.
	p.33	p.33	Modification	-A70

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of December, 2000. The information is subject to change without notice. For actual design-in, refer to the latest publications of Elpida's data sheets or data books, etc., for the most up-to-date specifications of Elpida semiconductor products. Not all products and/or types are available in every country. Please check with an Elpida Memory, Inc. for availability and additional information.**
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  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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M8E 00.4