

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

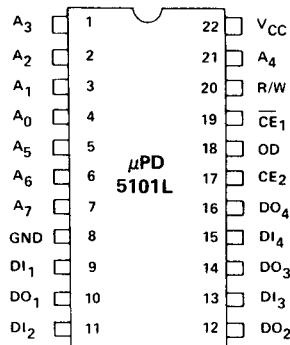
All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables (\overline{CE}_1 , CE_2) are provided, with the devices being selected when \overline{CE}_1 is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving \overline{CE}_1 high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

- FEATURES**
- Directly TTL Compatible – All Inputs and Outputs
 - Three-State Output
 - Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
 - Single +5V Power Supply
 - CE_2 Controls Unconditional Standby Mode
 - For operation at +3V Power Supply, Contact the NEC Sales Office.

PIN CONFIGURATION

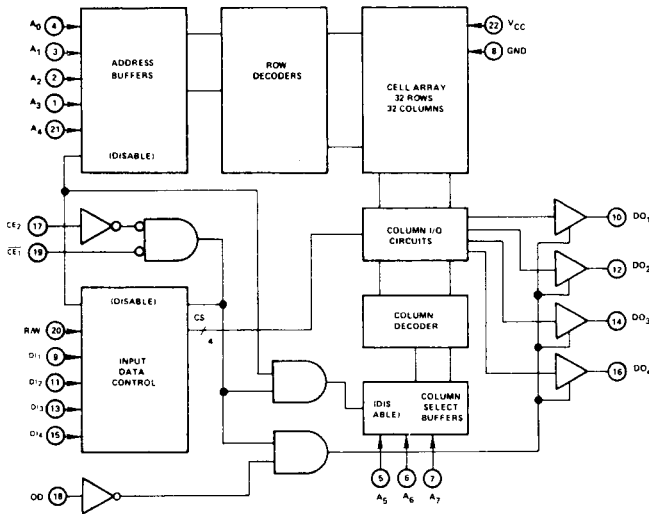


PIN NAMES

DI ₁ – DI ₄	Data Input
A ₀ – A ₇	Address Inputs
R/W	Read/Write Input
CE ₁ , CE ₂	Chip Enables
OD	Output Disable
DO ₁ – DO ₄	Data Output
VCC	Power (+5V)

μPD5101L

BLOCK DIAGRAM



Operating Temperature 0°C to +70°C
 Storage Temperature -40°C to +125°C
 Voltage On Any Pin With Respect to Ground -0.3 Volts to V_{CC} +0.3 Volts
 Power Supply Voltage -0.3 to +7.0 Volts
 T_a = 25°C

ABSOLUTE MAXIMUM RATINGS*

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input High Leakage	I _{LH} ②			1	μA	V _{IN} = V _{CC}
Input Low Leakage	I _{LI} ②			-1	μA	V _{IN} = 0V
Output High Leakage	I _{OH} ②			1	μA	$\overline{CE}_1 = 2.2V, V_{OUT} = V_{CC}$
Output Low Leakage	I _{OL} ②			-1	μA	$\overline{CE}_1 = 2.2V, V_{OUT} = 0.0V$
Operating Current	I _{CC1}			22	mA	V _{IN} = V _{CC} Except \overline{CE}_1 ≤ 0.65V, Outputs Open
Operating Current	I _{CC2}			27	mA	V _{IN} = 2.2V Except \overline{CE}_1 ≤ 0.65V, Outputs Open
Standby Current	I _{CCL} ②			10	μA	V _{IN} = 0 to 5.25V CE ₂ ≤ 0.2V
Input Low Voltage	V _{IL}	-0.3		0.65	V	
Input High Voltage	V _{IH}		2.2	V _{CC}	V	
Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 2.0 mA
Output High Voltage	V _{OH1}	2.4			V	I _{OH} = -1.0 mA
Output High Voltage	V _{OH2}	3.5			V	I _{OH} = -100 μA

Notes: ① Typical values at T_a = 25°C and nominal supply voltage.

② Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (All Input Pins)	C _{IN}		4	8	pF	V _{IN} = 0V
Output Capacitance	C _{OUT}		8	12	pF	V _{OUT} = 0V

$T_a = 0^\circ\text{C to } 70^\circ\text{C}; V_{CC} = 5V \pm 5\%$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts Input rise and fall times: 20 ns Timing measurement reference level: 1.5 Volt Output load: I_{TTL} Gate and $C_L = 100\text{ pF}$
Access Time	t_A			650			450	ns	
Chip Enable (CE_1) to Output	t_{CO1}			600			400	ns	
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	
Output Disable to Output	t_{OD}			350			250	ns	
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{QH2}	0			0			ns	

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WRITE CYCLE

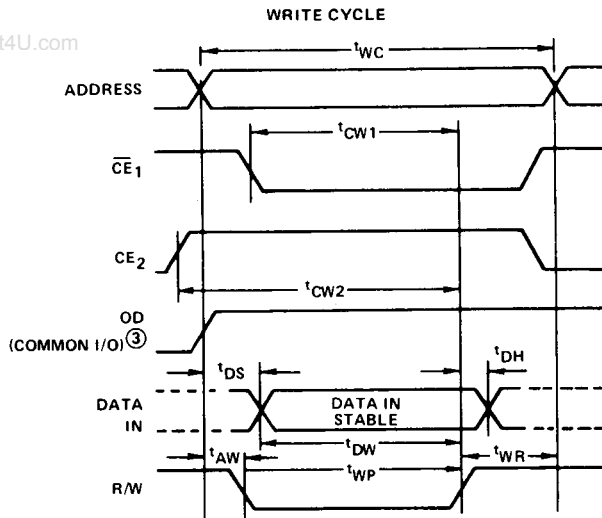
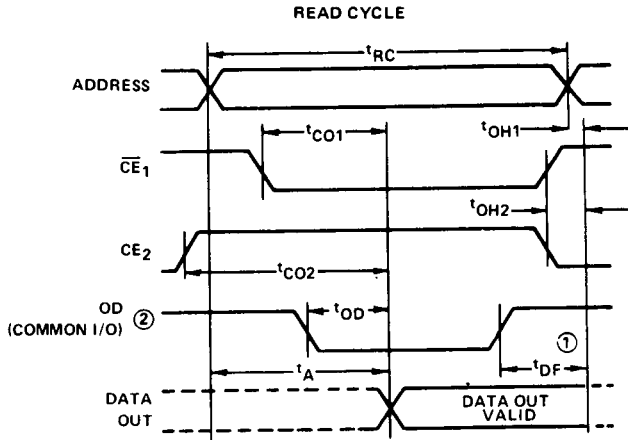
 $T_a = 0^\circ\text{C to } 70^\circ\text{C}; V_{CC} = 5V \pm 5\%$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts Input rise and fall times: 20 ns Timing measurement reference level: 1.5 Volt Output load: I_{TTL} Gate and $C_L = 100\text{ pF}$
Write Delay	t_{AW}	150			130			ns	
Chip Enable (CE_1) to Write	t_{CW1}	550			350			ns	
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	
Data Setup	t_{DW}	400			250			ns	
Data Hold	t_{DH}	100			50			ns	
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130			ns	

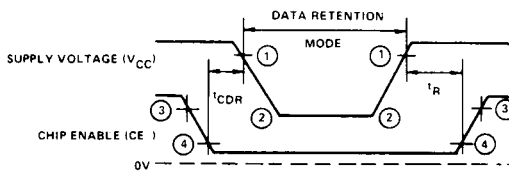
LOW V_{CC} DATA RETENTION CHARACTERISTICS $T_a = 0^\circ\text{C to } 70^\circ\text{C}$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	$V_{CCDR} = +2.0V$ $CE_2 \leq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC} ①			ns	

Note: ① t_{RC} = Read Cycle Time



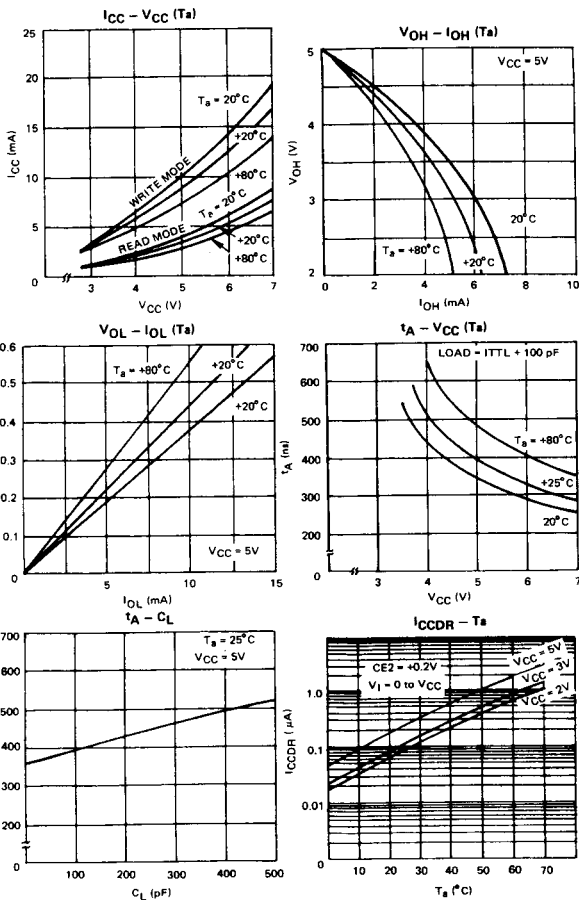
- Notes:
- ① Typical values are for $T_a = 25^\circ\text{C}$ and nominal supply voltage.
 - ② OD may be tied low for separate I/O operation.
 - ③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.



- Notes:
- ① 4.75V
 - ② V_{CCDR}
 - ③ V_{IH}
 - ④ 0.2V

LOW V_{CC} DATA RETENTION

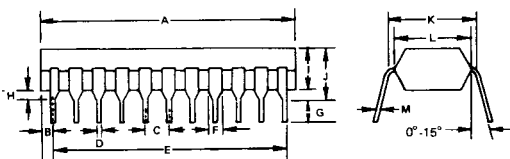
TYPICAL OPERATING CHARACTERISTICS



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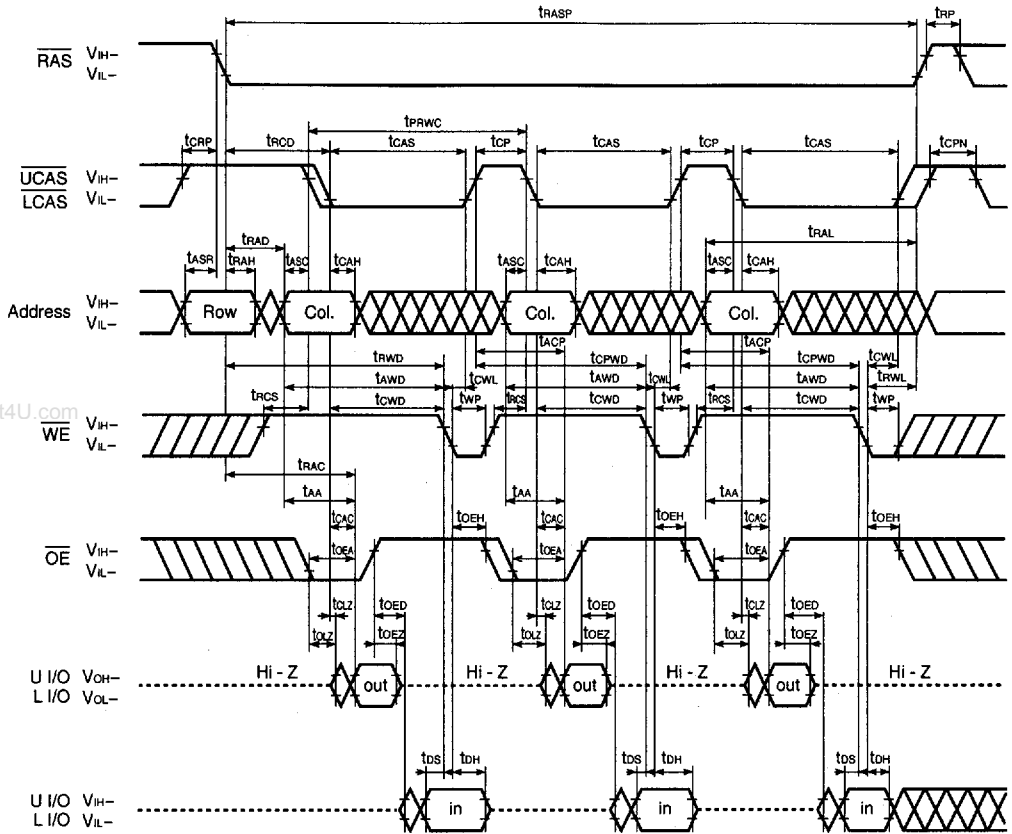
PACKAGE OUTLINE
μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 0.10	0.02 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	+0.10 0.05	+0.004 0.002

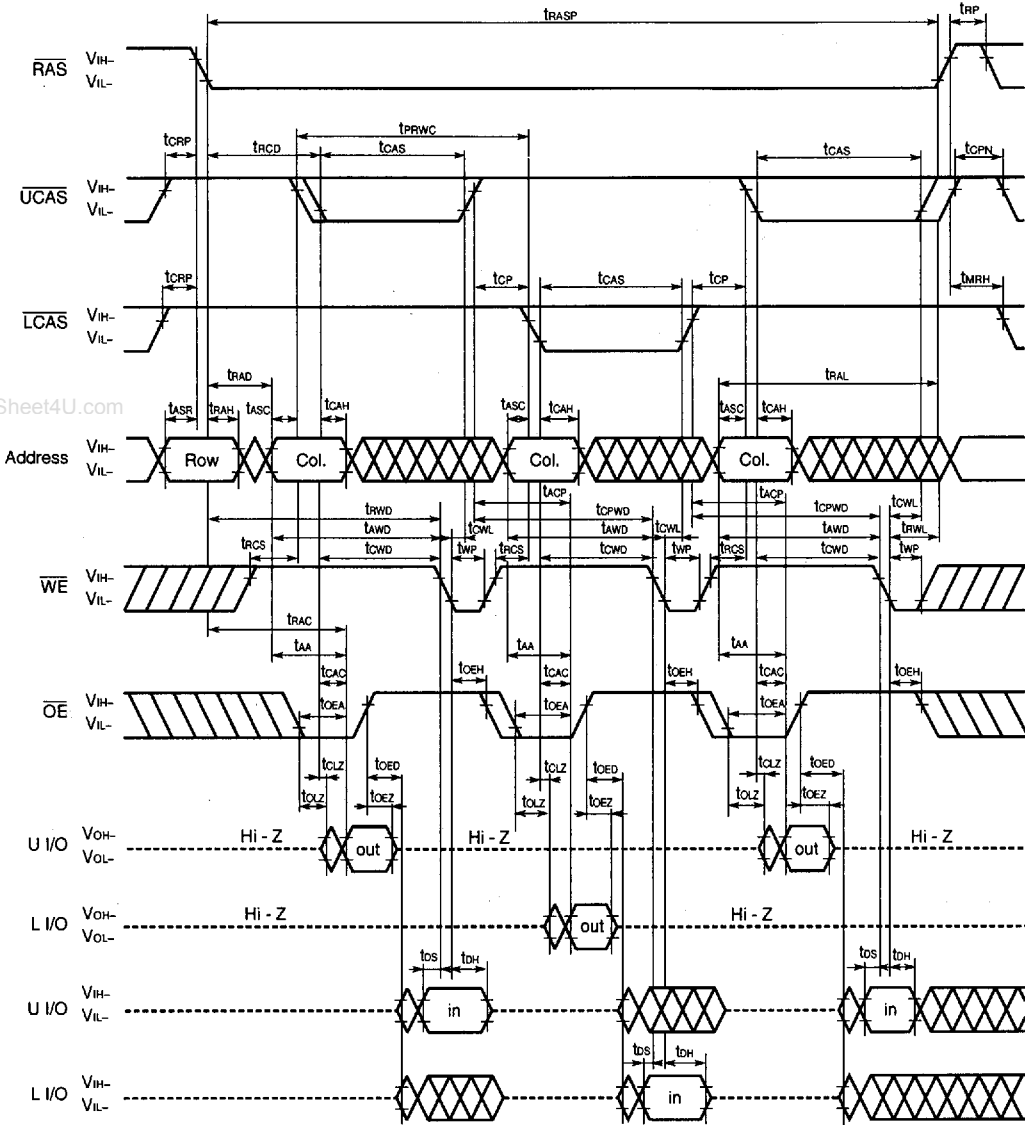
5101LDS-REV1-12-81-CAT

Fast Page Mode Read Modify Write Cycle



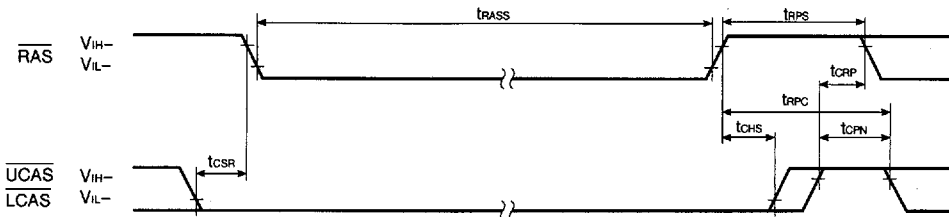
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

Fast Page Mode Byte Read Modify Write Cycle



- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
 2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

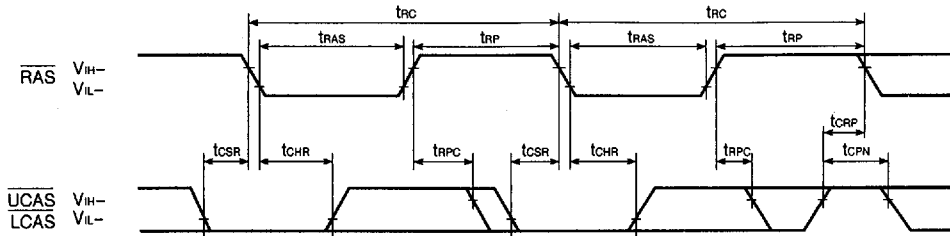
(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied. And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

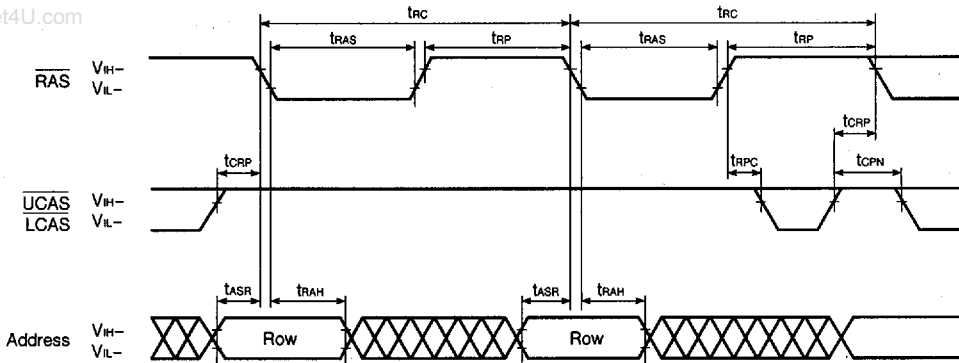
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



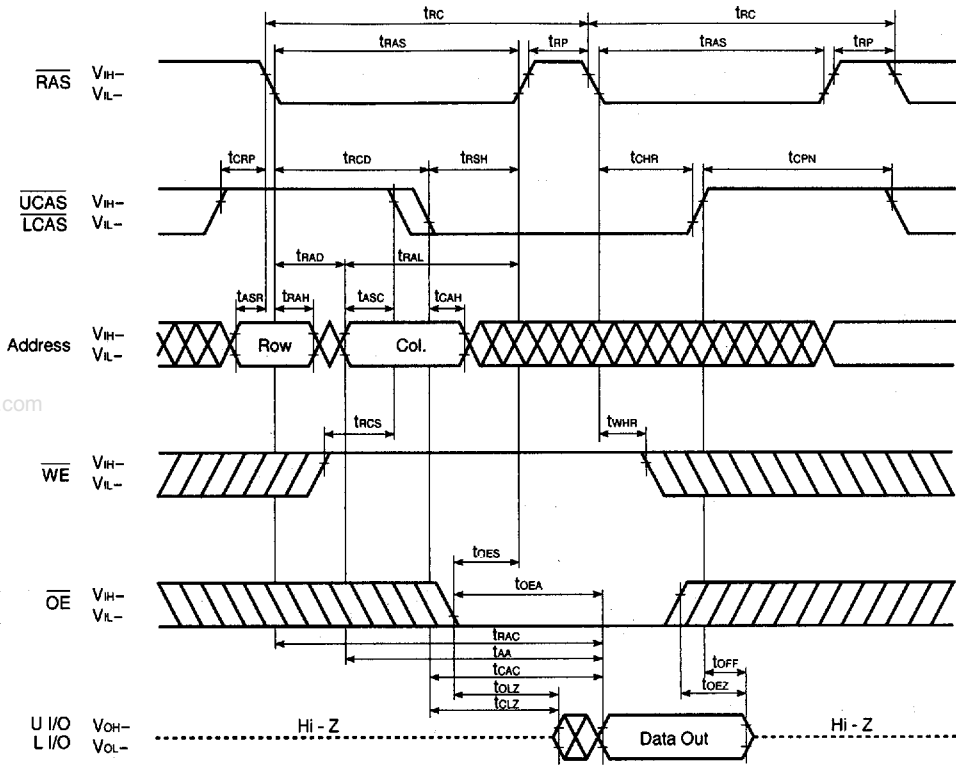
Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



Remark \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



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