EVACHIP-43

DESCRIPTION

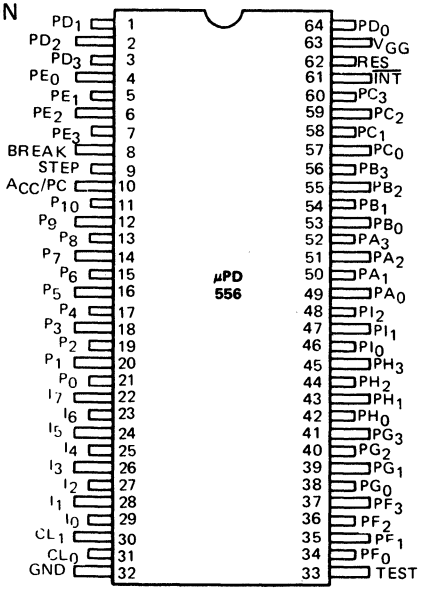
The μPD556 is an evaluation chip for the μCOM-43/44/45 single chip microcomputers. Designed to be used for both hardware and software debugging, the EVACHIP-43 is functionally equivalent to the μCOM-43, except that it does not contain on-chip ROM. Instead, it is able to address external memory. In addition, in order to facilitate debugging, the μPD556 is capable of displaying the contents of the internal accumulator and data pointer and of being single stepped.

When the μPD556 is being used to evaluate μCOM-44/45 designs, the external memory capacity should be restricted to that of the respective on-chip ROM and the instructions should be restricted to the 58 comprising the μCOM-44/45 instruction set.

FEATURES

- 4-bit Parallel Processor
- Full 80 Instruction Set of μCOM-43
- 10 μs Instruction Cycle
- Capable of addressing 2K x 8-bits of external program memory
- Single step capability
- Full Functionality of μCOM-43
- Single supply: -10V PMOS Technology
- Available in a 64-pin Ceramic Quad-in-Line Package

PIN CONFIGURATION

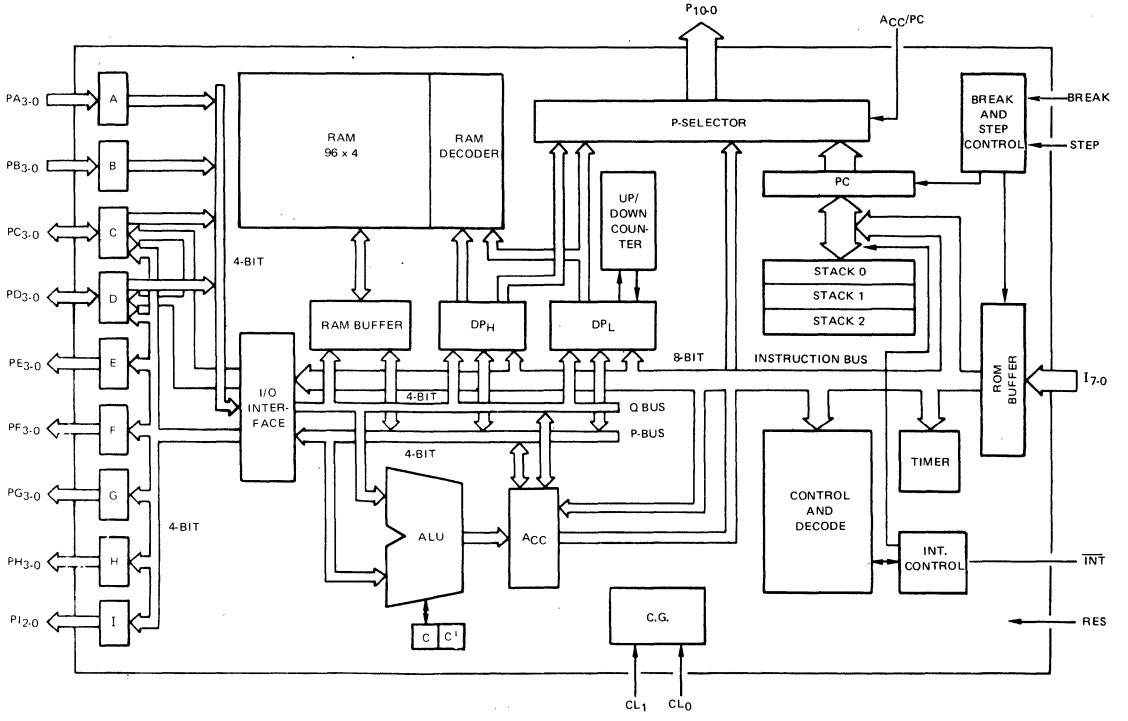


PIN NAMES

PF_0 - PF_3	Output Port F
PG_0 - PG_3	Output Port G
PH_0 - PH_3	Output Port H
PI_0 - PI_2	Output Port I
PA_0 - PA_3	Input Port A
PB_0 - PB_3	Input Port B
PC_0 - PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0 - PD_3	Input/Output Port D
PE_0 - PE_3	Output Port E
BREAK	Hold Input
STEP	Single Step Input
ACC/PC	Display A_{CC}/PC Input
P_0 - P_{10}	PC Output
I_0 - I_7	Instruction Input
CL_0 - CL_1	External Clock Source
TEST	Tied to V_{SS} (GND)

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
All Input Voltages	−15 to +0.3 Volts
All Output Voltages	−15 to +0.3 Volts
Output Current	−4 mA ①

Note: ① All output pins.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

DC CHARACTERISTICS ①

$T_a = -10$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		-2.0	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Input Low Voltage	V_{IL}	-4.3		V_{GG}	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Clock High Voltage	V_{OH}	0		-0.8	V	CL_0 Input
Clock Low Voltage	V_{OL}	-6.0		V_{GG}	V	CL_0 Input
Input Leakage Current High	I_{LIH}			+10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				+30	μA	A_{CC}/PC, $V_I = -1V$ Port C and D, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			-10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				-30	μA	A_{CC}/PC, $V_I = -11V$ Port C and D, $V_I = -11V$
Clock Input Leakage High	I_{LOH}			+200	μA	CL_0 Input, $V_{OH} = 0V$
Clock Input Leakage Low	I_{LOL}			-200	μA	CL_0 Input, $V_{OL} = -11V$
Output High Voltage	V_{OH1}			-1.0	V	Port C to I, P_{10} to P_0 $I_{OH} = -1.0$ mA
	V_{OH2}			-2.3	V	Port C to I, P_{10} to P_0 $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			-30	μA	Port C to I, P_{10} to P_0 $V_O = -11V$
Supply Current	I_{GG}		-30	-50	mA	

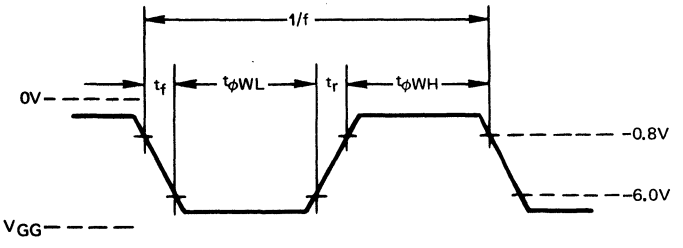
Note: ① Relative to $V_{SS} = 0V$

AC CHARACTERISTICS

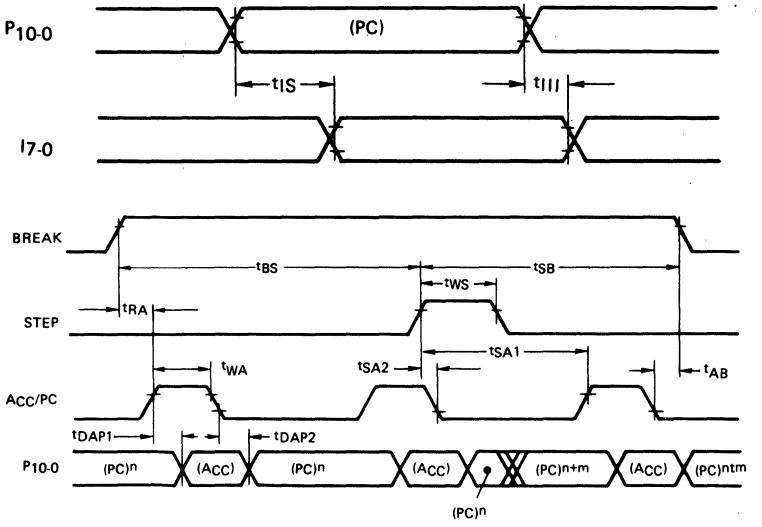
$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Frequency	f	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t\phi WH$	0.5		5.6	μs	
Clock Pulse Width Low	$t\phi WL$	0.5		5.6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	80			tcy	
STEP to RUN Interval	t_{SB}	80			tcy	
STEP Pulse Width	t_{WS}	12			tcy	
BREAK to A_{CC} Interval	t_{BA}	80			tcy	
A_{CC}/PC Pulse Width	t_{WA}	12			tcy	
STEP to A_{CC} Interval	t_{SA1}	80			tcy	
PC to STEP Overlap	t_{SA2}			2	tcy	
PC to RUN Interval	t_{AB}	0			μs	
A_{CC}/PC → P_{10}-P_0 Delay	t_{DAP1}			6	tcy	
	t_{DAP2}			6	tcy	

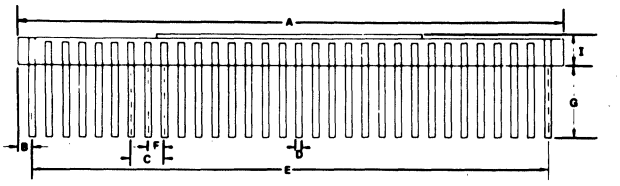
CLOCK WAVEFORM

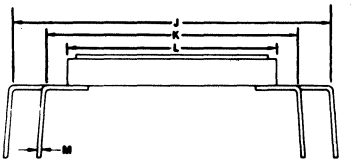


TIMING WAVEFORM



PACKAGE OUTLINE μPD556B





(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002