μPD5902T7K

CMOS Integrated Circuits High Power SPDT Switch

R09DS0046EJ0200
Rev.2.00
Nov 19, 2012

DESCRIPTION

The μPD5902T7K is a CMOS MMIC SPDT (Single Pole Double Throw) switch for GSM and UMTS/LTE main Antenna switching and other High Power RF switching applications up to +35 dBm.

This device can operate frequency from 0.05 to 6.0 GHz, having low insertion loss and high isolation.

This device is housed in a 12-pin plastic QFN (Quad Flat Non-Leaded) (T7K) package.

FEATURES

- Low control voltage : V_{cont} = 1.3 V MIN., V_{DD} = 2.3 V MIN.
- Low insertion loss : L_{ins} = 0.35/0.40 dB TYP. @ f = 1.0/2.0 GHz
- High isolation : ISL = 45/37 dB TYP. @ f = 1.0/2.0 GHz
- High Handling power : $P_{in\ (0.1dB)}$ = +38 dBm TYP. @f = 0.9/2.0 GHz
- High-density surface mounting : 12-pin plastic QFN (T7K) package (2.0 × 2.0 × 0.6 mm)
- No DC blocking capacitors required.

APPLICATIONS

- GSM and UMTS/LTE main Antenna switching etc.
- Other RF switching Applications.
- Antenna tuning Applications.

ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Supplying Form
μPD5902T7K-E2	μPD5902T7K-E2-A	12-pin plastic QFN (T7K) (Pb-Free)	5902	• Embossed tape 8 mm wide • Pin 10, 11 and 12 face the perforation side of the tape • Qty 3 kpcs/reel

Remark To order evaluation samples, please contact your nearby sales office.
Part number for sample order: μPD5902T7K-A

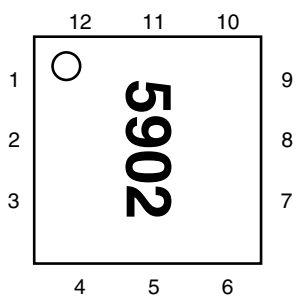
CAUTION

Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

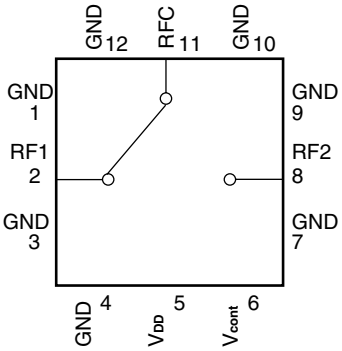
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

<R> PIN CONNECTIONS AND INTERNAL BLOCK DIAGRAM

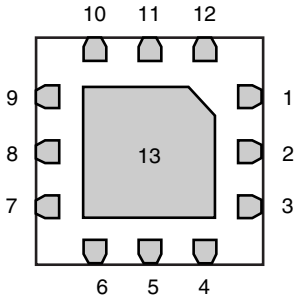
(Top View)



(Top View)



(Bottom View)



Pin No.	Pin Name
1	GND
2	RF1
3	GND
4	GND
5	V_{DD}
6	V_{cont}
7	GND
8	RF2
9	GND
10	GND
11	RFC
12	GND
13	GND

SW TRUTH TABLE

V_{cont}	RFC–RF1	RFC–RF2
High	ON	OFF
Low	OFF	ON

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	3.6	V
Control Voltage	V_{cont}	3.6	V
Input Power	P_{in}	+38	dBm
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

RECOMMENDED OPERATING RANGE (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Operating Frequency	f	0.05	–	6.0	GHz
Supply Voltage	V_{DD}	2.3	–	3.3	V
Control Voltage (High)	$V_{cont\ (H)}$ Note	1.3	–	V_{DD}	V
Control Voltage (Low)	$V_{cont\ (L)}$	0	–	0.4	V

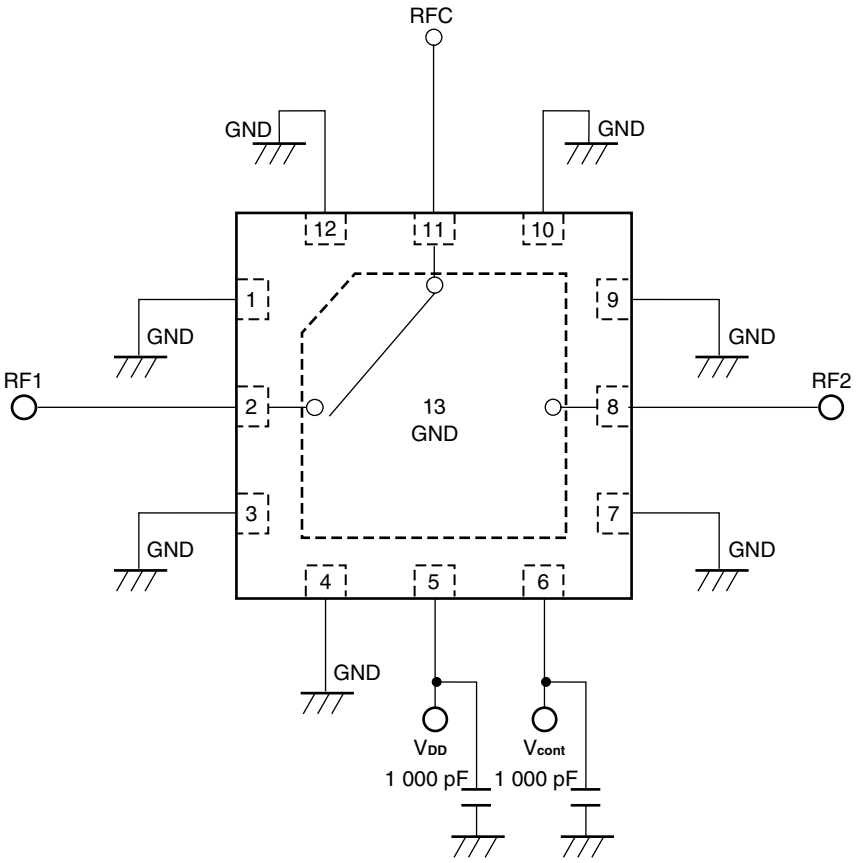
Note: $V_{cont} \leq V_{DD}$

ELECTRICAL CHARACTERISTICS
(T_A = +25°C, V_{DD} = 2.5 V, $V_{cont\ (H)}$ = 1.8 V, $V_{cont\ (L)}$ = 0 V, Z_0 = 50 Ω, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Insertion Loss	$L_{ins}1$	f = 0.05 to 0.5 GHz, P_{in} = 0 dBm	–	0.30	0.45	dB
	$L_{ins}2$	f = 0.5 to 1.0 GHz	–	0.35	0.50	
	$L_{ins}3$	f = 1.0 to 2.0 GHz	–	0.40	0.55	
	$L_{ins}4$	f = 2.0 to 2.7 GHz	–	0.45	0.75	
	$L_{ins}5$	f = 2.7 to 3.8 GHz	–	0.50	0.80	
	$L_{ins}6$	f = 3.8 to 6.0 GHz	–	0.60	0.95	
<R> Isolation (RFC – RF1,2)	ISL1	f = 0.05 to 0.5 GHz, P_{in} = 0 dBm	45	50	–	
	ISL2	f = 0.5 to 1.0 GHz	40	45	–	
	ISL3	f = 1.0 to 2.0 GHz	32	37	–	
	ISL4	f = 2.0 to 2.7 GHz	30	35	–	
	ISL5	f = 2.7 to 3.8 GHz	25	30	–	
	ISL6	f = 3.8 to 6.0 GHz	–	23	–	
Return Loss (RFC)	RL1	f = 0.05 to 3.8 GHz	15	18	–	
	RL2	f = 3.8 to 6.0 GHz	–	15	–	
Return Loss (RF1,2)	RL1	f = 0.05 to 3.8 GHz	15	18	–	
	RL2	f = 3.8 to 6.0 GHz	–	15	–	
0.1 dB Loss Compression Input Power	$P_{in(0.1dB)}1$	f = 0.9 GHz	+36.0	+38.0 **Note**	–	dBm
	$P_{in(0.1dB)}2$	f = 2.0 GHz	+36.0	+38.0 **Note**	–	
Harmonics	2f0	f = 0.9 GHz, P_{in} = +35 dBm	75	80	–	dBc
	3f0		70	75	–	
	2f0	f = 2.0 GHz, P_{in} = +33 dBm	75	85	–	
	3f0		70	80	–	
2nd Order Inter Modulation Distortion	IMD2	f = 835 MHz, P_{in} = +20 dBm f = 45 MHz, P_{in} = –15 dBm	–	–98	–93	dBm
		f = 1 950 MHz, P_{in} = +20 dBm f = 190MHz, P_{in} = –15 dBm	–	–105	–100	
3rd Order Inter Modulation Distortion	IMD3	f = 835 MHz, P_{in} = +20 dBm f = 790 MHz, P_{in} = –15 dBm	–	–110	–105	
		f = 1 950 MHz, P_{in} = +20 dBm f = 1 760 MHz, P_{in} = –15 dBm	–	–110	–105	
Input 3rd order Intercept Point	IIP_3	f = 2 500 MHz, P_{in} = +20 dBm f = 2 501 MHz, P_{in} = +20 dBm	65	70	–	dBm
Switch Control Speed	T_{sw}	50% CTL to 90/10%	–	2.0	5.0	μsec
Supply Current	I_{DD}	Active Mode No RF	–	130	250	μA
Control Current	I_{cont}(H)	V_{cont} : High No RF	–	–	1	
	I_{cont}(L)	V_{cont} : Low No RF	–	–	1	

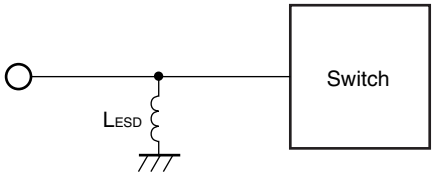
Note: Absolute Maximum Ratings

<R> EVALUATION CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

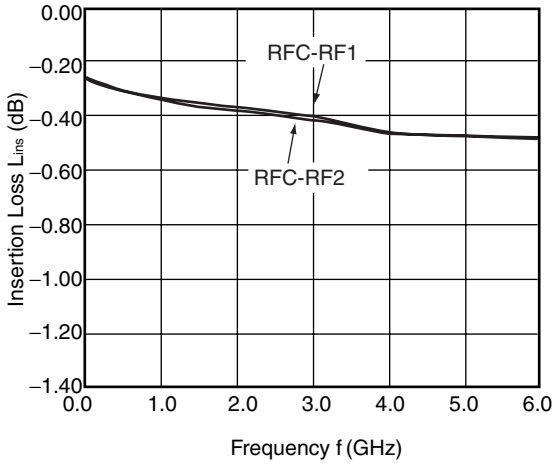
APPLICATION INFORMATION



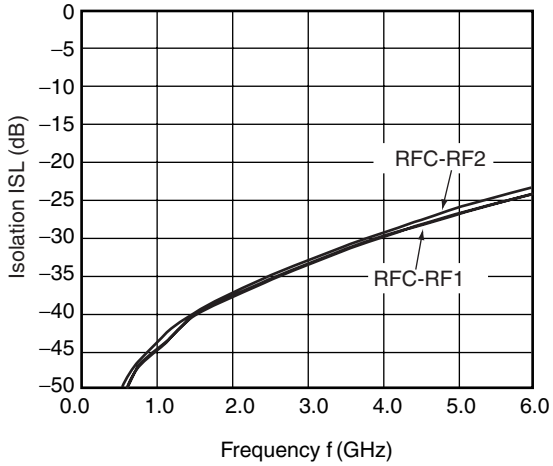
- L_{ESD} provides a means to increase the ESD protection on a specific RF port, typically the port attached to the antenna.

TYPICAL CHARACTERISTICS
(T_A = +25°C, V_{DD} = 2.5 V, $V_{cont\ (H)}$ = 1.8 V, $V_{cont\ (L)}$ = 0 V, Z_0 = 50 Ω, unless otherwise specified)

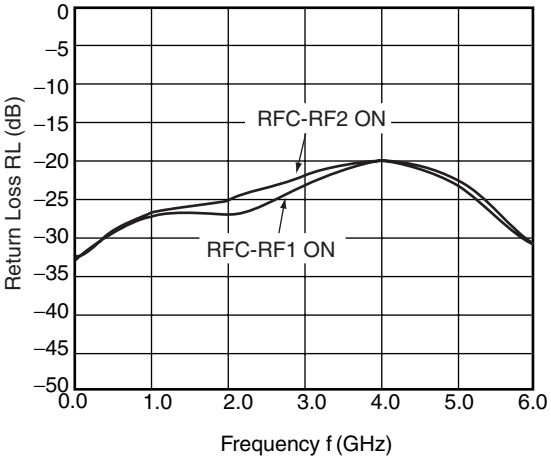
RFC-RF1/RF2
INSERTION LOSS vs. FREQUENCY



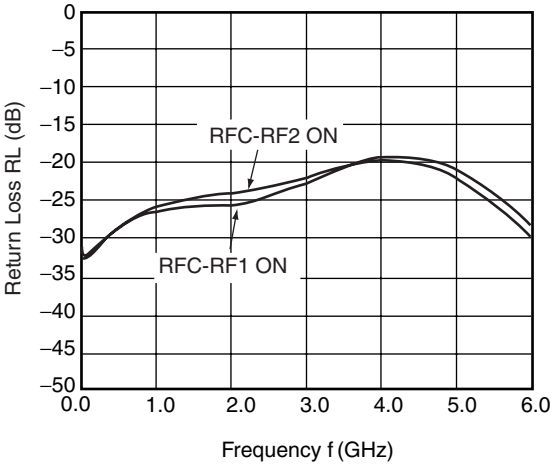
RFC-RF1/RF2
ISOLATION vs. FREQUENCY



RFC
RETURN LOSS vs. FREQUENCY

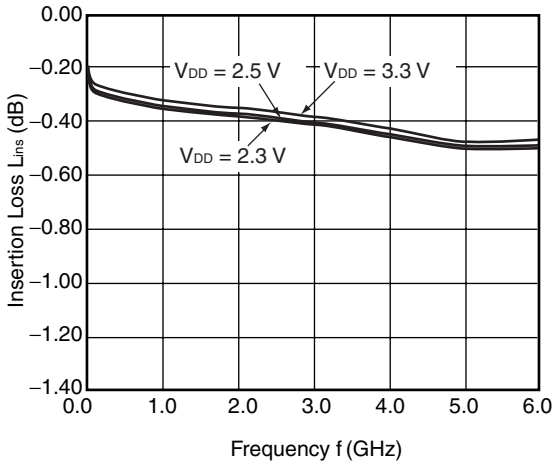


RF1/RF2
RETURN LOSS vs.FREQUENCY

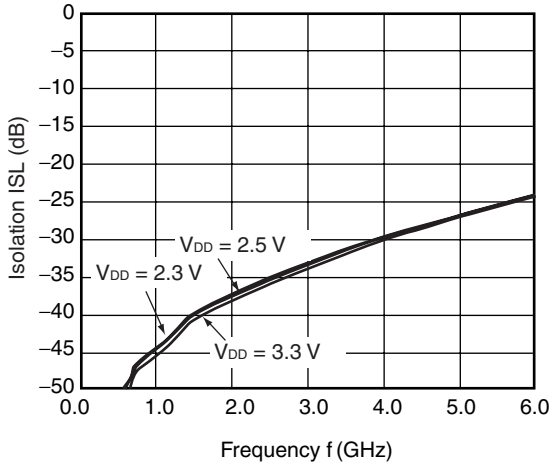


Remark The graphs indicate nominal characteristics.

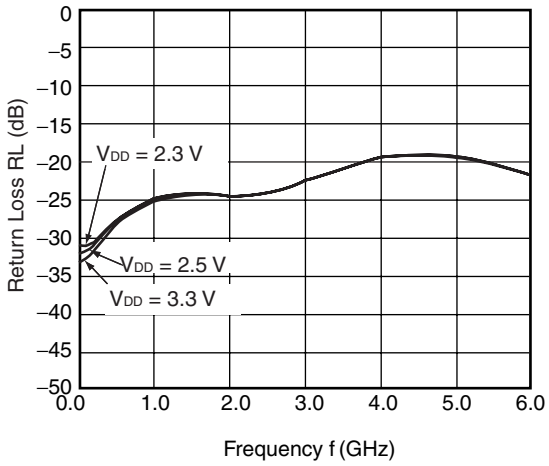
RFC-RF1/RF2
INSERTION LOSS vs. FREQUENCY



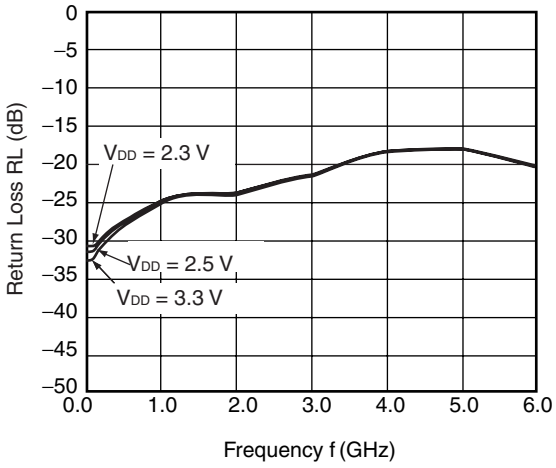
RFC-RF1/RF2
ISOLATION vs. FREQUENCY



RFC
RETURN LOSS vs. FREQUENCY

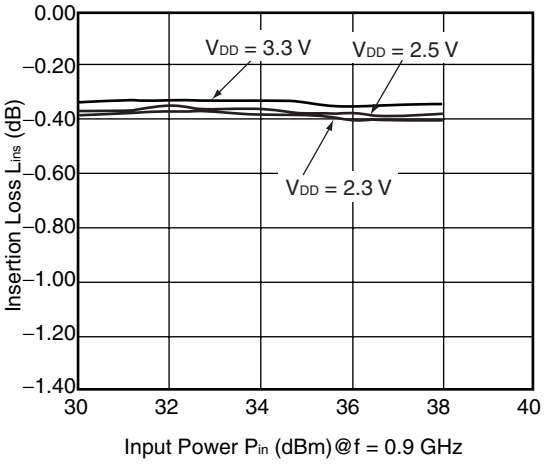


RF1/RF2
RETURN LOSS vs. FREQUENCY

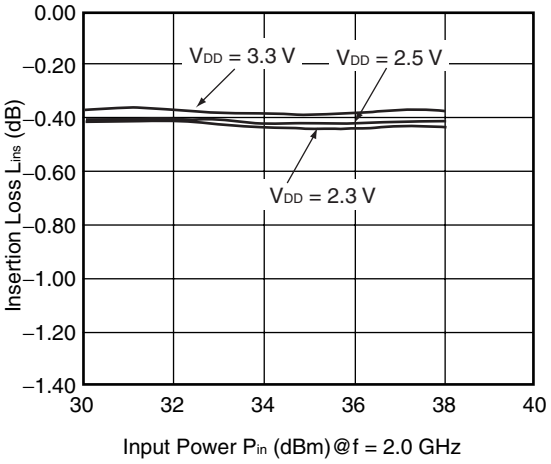


Remark The graphs indicate nominal characteristics.

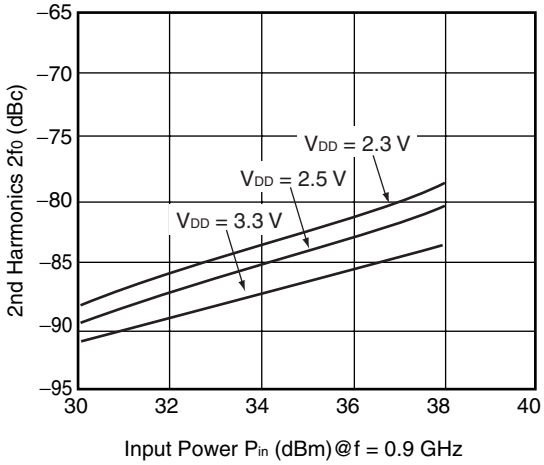
RFC-RF1/RF2
INSERTION LOSS vs. INPUT POWER



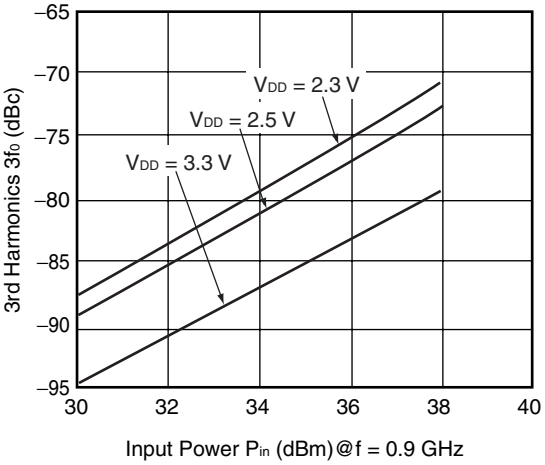
RFC-RF1/RF2
INSERTION LOSS vs. INPUT POWER



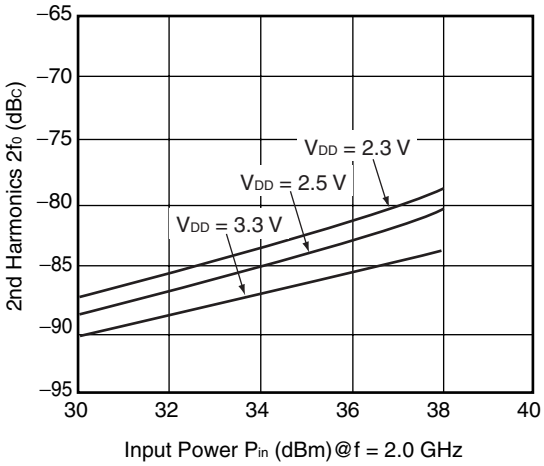
RFC-RF1/RF2
2nd HARMONICS vs. INPUT POWER



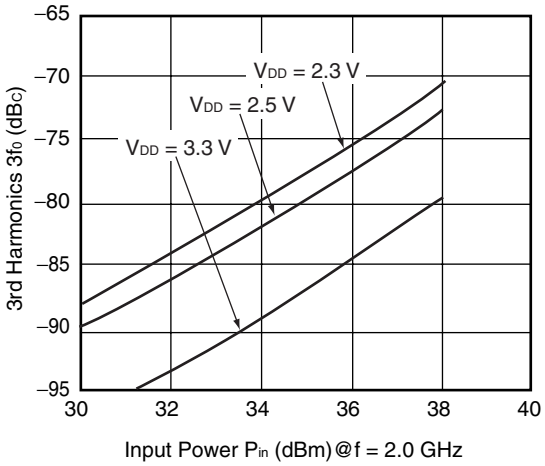
RFC-RF1/RF2
3rd HARMONICS vs. INPUT POWER



RFC-RF1/RF2
2nd HARMONICS vs. INPUT POWER

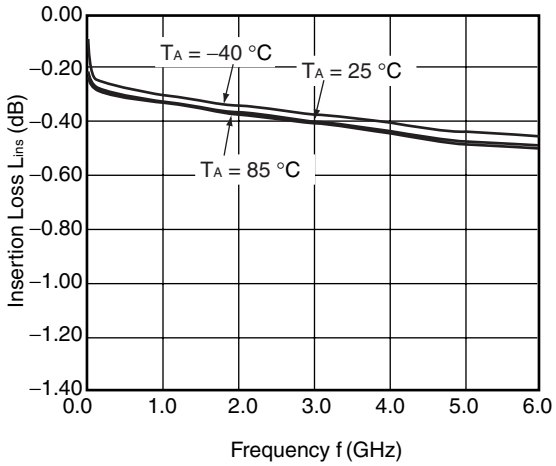


RFC-RF1/RF2
3rd HARMONICS vs. INPUT POWER

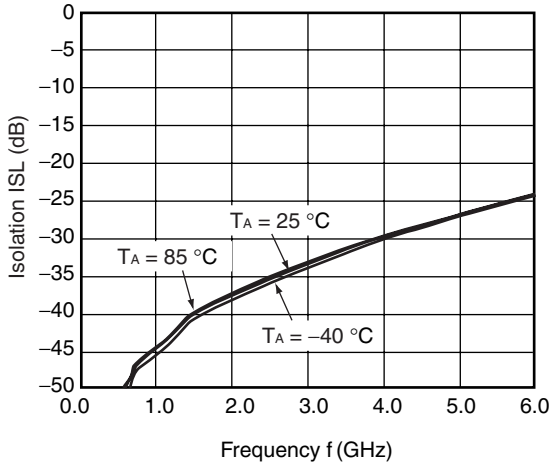


Remark The graphs indicate nominal characteristics.

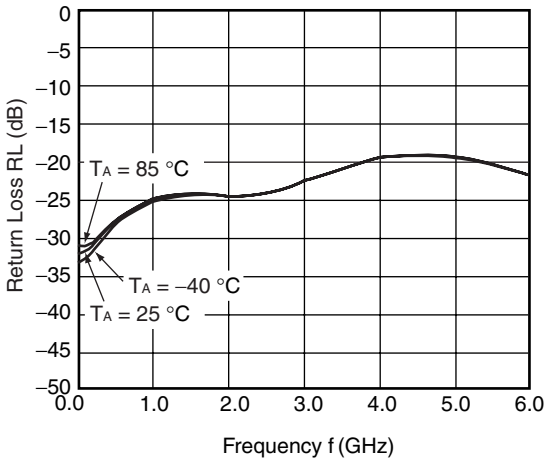
RFC-RF1/RF2
INSERTION LOSS vs. FREQUENCY



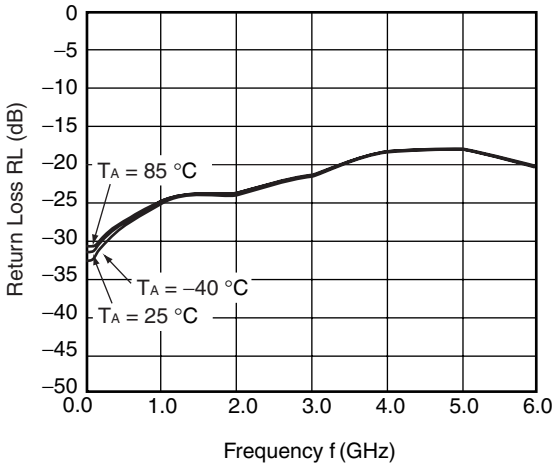
RFC-RF1/RF2
ISOLATION vs. FREQUENCY



RFC
RETURN LOSS vs. FREQUENCY



RF1/RF2
RETURN LOSS vs. FREQUENCY



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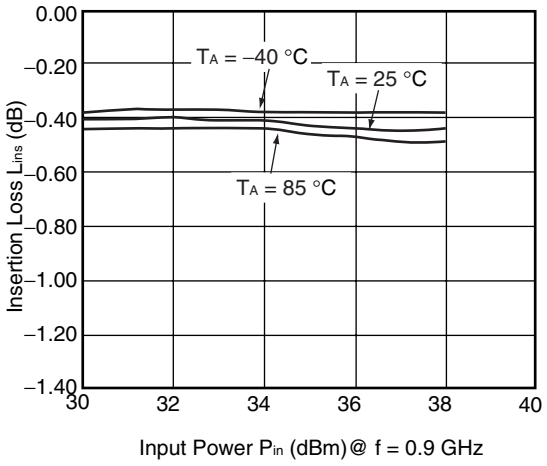
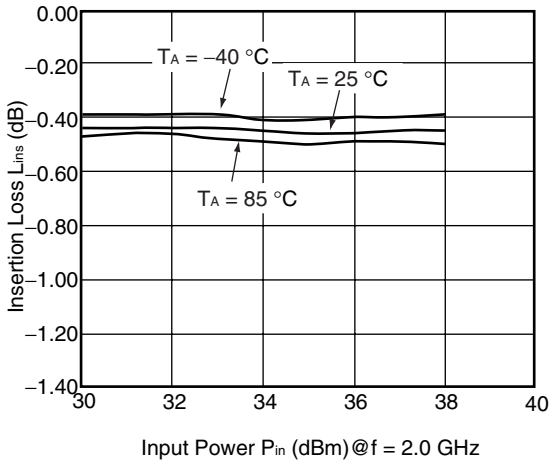
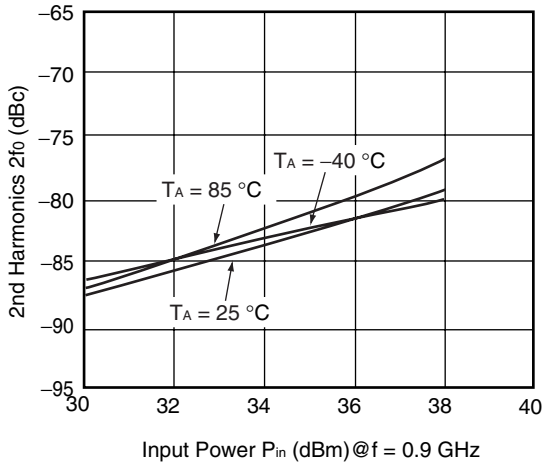
RFC-RF1/RF2
INSERTION LOSS vs. INPUT POWER



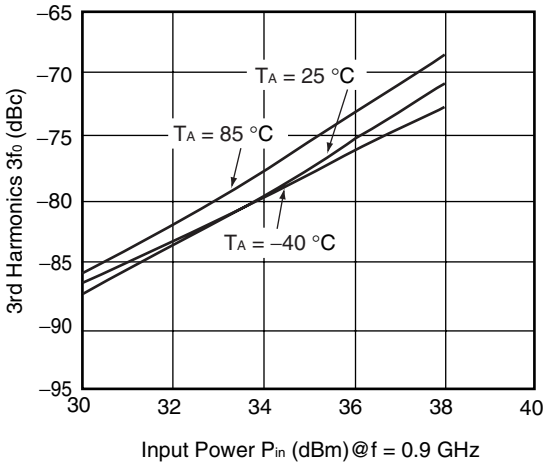
RFC-RF1/RF2
INSERTION LOSS vs. INPUT POWER



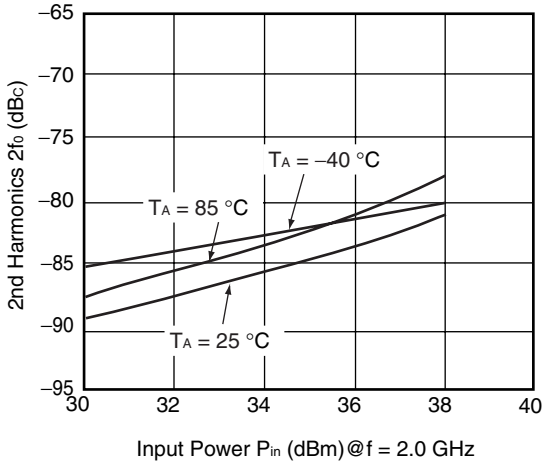
RFC-RF1/RF2
2nd HARMONICS vs. INPUT POWER



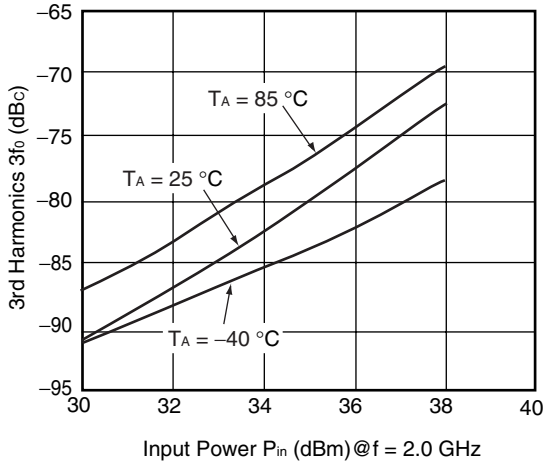
RFC-RF1/RF2
3rd HARMONICS vs. INPUT POWER



RFC-RF1/RF2
2nd HARMONICS vs. INPUT POWER



RFC-RF1/RF2 3rd HARMONICS vs.
INPUT POWER

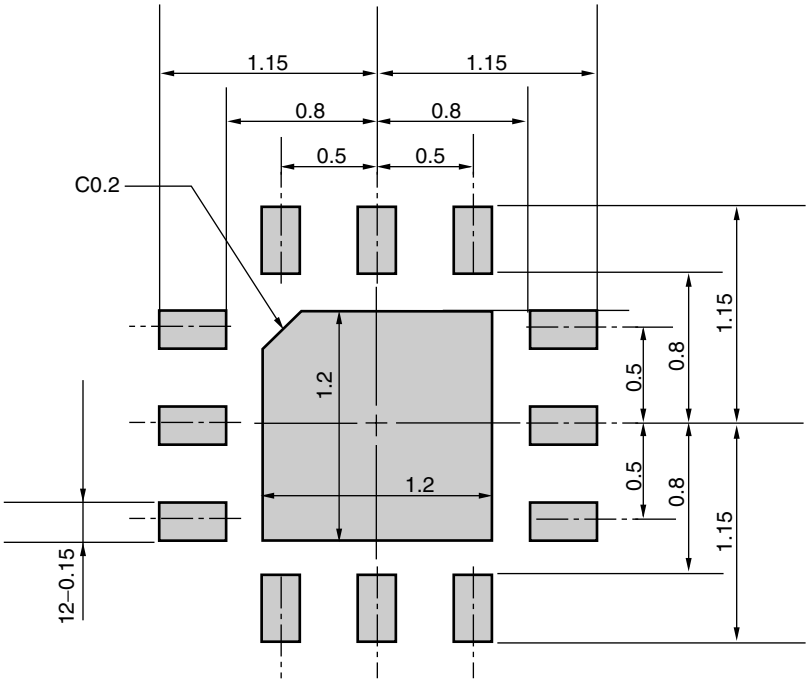


Remark The graphs indicate nominal characteristics.

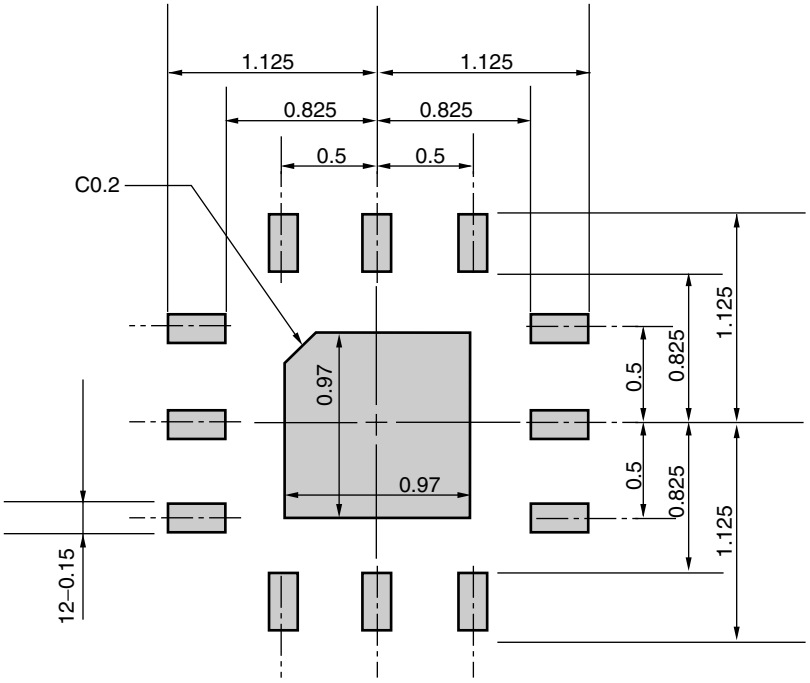
MOUNTING PAD LAYOUT DIMENSIONS

12-PIN PLASTIC QFN (T7K) (UNIT: mm)

MOUNTING PAD



SOLDER MASK

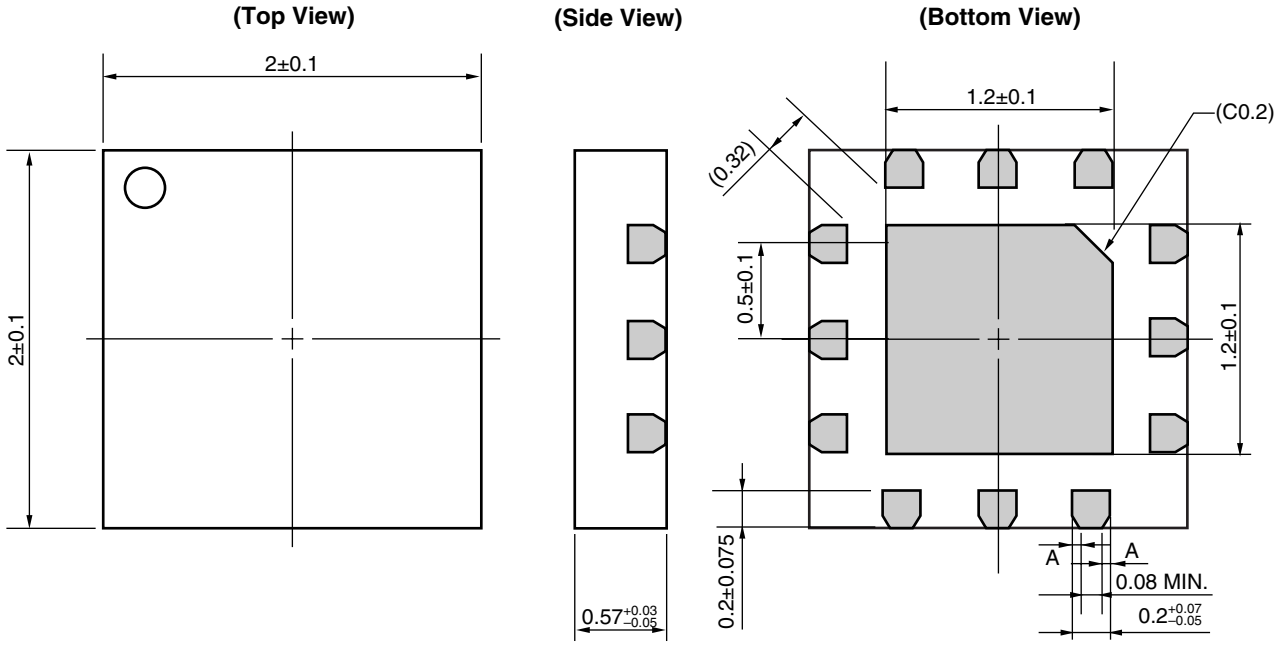


Solder thickness : 0.1 mm

Remark The mounting pad layout in this document is for reference only.
When designing PCB, please consider workability of mounting, solder joint reliability, prevention of solder bridge and so on, in order to optimize the design.

PACKAGE DIMENSIONS

12-PIN PLASTIC QFN (T7K) (UNIT: mm)



Remark A > 0

( ): Reference value

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2% (Wt.) or below	IR260
Partial Heating	Peak temperature (terminal temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2% (Wt.) or below	HS350

CAUTION

Do not use different soldering methods together (except for partial heating).

Revision History	μPD5902T7K Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 10, 2012	–	First edition issued
2.00	Nov 19, 2012	p.2	The block diagram is changed.
		p.3	The symbol indicating the range between terminals is changed from “to” to “–“.
		p.4	The evaluation circuit is changed.

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[Colophon 2.2]