NEC

MOS INTEGRATED CIRCUIT
μPD61171

SECOND GENERATION ENHANCED MULTIMEDIA ARCHITECTURE
PROCESSOR FOR DVD RECORDER/PERSONAL VIDEO RECORDERS

DESCRIPTION

The μPD61171 is a fully-integrated system processor for DVD recorders or personal video recorders (PVR). Based on NEC Electronics' second-generation Enhanced Multi Media Architecture (EMMArchitecture), the μPD61171 provides the functionality required to realize a high-performance and cost-effective DVD recorder or PVR.

FEATURES

- DVD-Video, DVD-Video Recording compliant
- DVB, MPEG2-TS/PS and MPEG1 compliant codec
- Dolby™ digital audio codec, DTS™ audio decoder
- High performance, dual MIPS32™ CPU core: 225 MIPS at 187 MHz
- High-bandwidth unified memory controller to support external DDR SDRAM
- Flexible multi-standard, multi-stream processor
- Integrated CSS and CPPM decryption
- Integrated CPRM and DES encryption/decryption
- Integrated Multi-2 and DVB descrambler
- Dual storage interfaces for ATA UDMA100-compliant HDD and ATAPI DVD drive
- Real time VBR/CBR encoding
- 3D noise reduction filter and motion-adaptive de-interlacer
- 7 graphics planes with dual video scalars
- Simultaneous progressive and interlace video outputs: 6 DACs for YPbPr (or YCbCr or RGB), S-Video (Y/C) and CVBS output with support for NTSC, PAL and SECAM
- Multi-channel audio outputs: IEC60958 and PCM with support for up to 8 channels
- Selectable host bus interface: Generic 16-bit host bus or PCI bus

APPLICATIONS

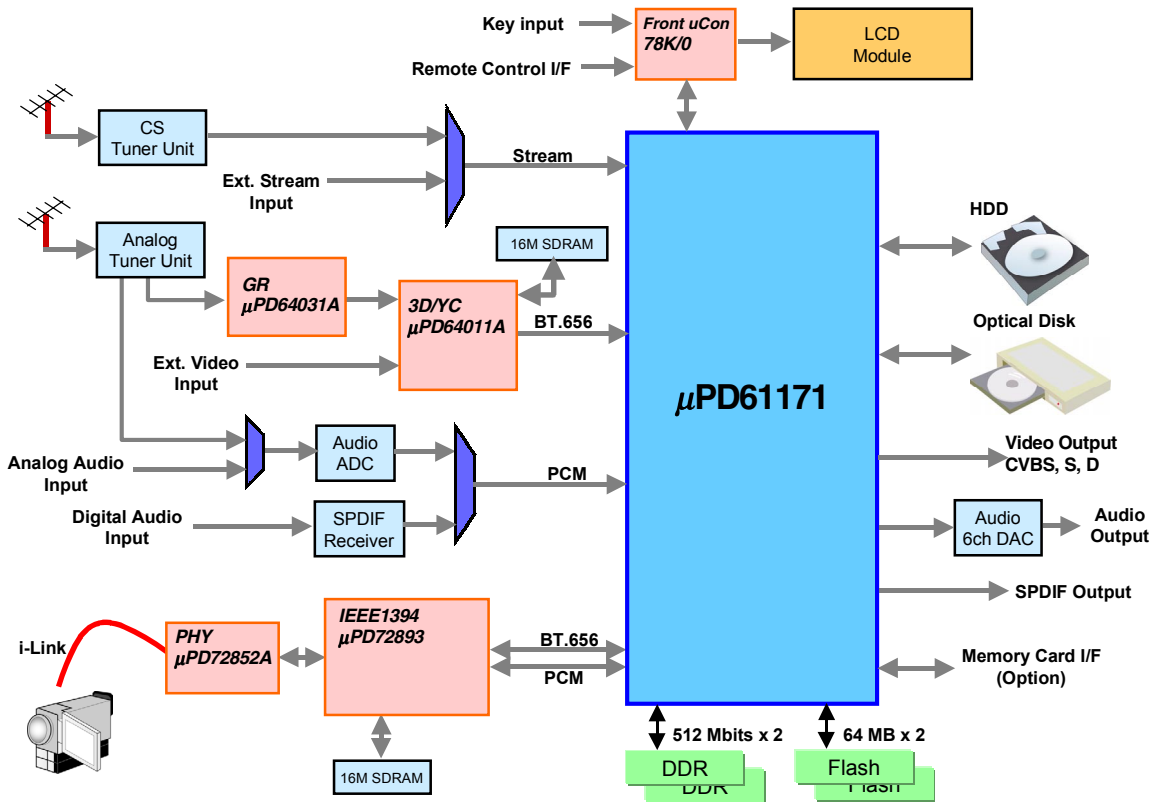DVD recorders, personal video recorders, home servers

ORDERING INFORMATION

Part number	Package	Remark
μPD61171F1-XYZ-MN2-A	449-pin plastic BGA (27 × 27)	XYZ: Audio option

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TYPICAL APPLICATION

FEATURE LIST

High-performance main processor:

    High-performance MIPS32 CPU core: 225 Dhrystone MIPS @187 MHz frequency

    32-bit RISC MIPS architecture

    Supports MIPS32 instruction set

    8 KB instruction cache, 8 KB data cache configuration

    EJTAG debugging interface

High-performance sub CPU:

    High-performance MIPS32 CPU core with DSP features for media processing

    8 KB instruction cache, 8 KB data cache configuration

    48 KB scratch-pad memory support

Unified memory controller:

    Supports 32-bit bus width DDR SDRAM

    Supports data rate up to PC266

    Unified CPU / MPEG Codec / Graphics memory

    Supports 128 M bits, 256 M bits, 512 M bits DDR SDRAM device

    Total memory size up to 1 G bits

External memory interface (EMI):

    ROM interface

        Total address area 64 MB/CS for ROM

        Supports normal, page and flash ROM

        Supports NOR, NAND and strata flash ROM

        2 chip select signals for ROM

    General input/output (GIO) interface

        Total address area 16 MB for GIO

        4 chip select signals for GIO

        Supports Intel, Motorola, and 16-bit PC card (PCMCIA) interfaces

MPEG video encode engine:

    MPEG2 video MP@ML, SP@ML standard and MPEG1 standard

    Single-pass VBR, CBR encode control

    Supports various picture sizes

        Horizontal: 720, 704, 640, 544, 480, 352, 320 pixels/line

        Vertical: 480, 240, 576, 288 lines/frame

        Pre-analysis: Film detection, scene change detection and motion estimation assist

    Supports video

        8-bit Y/Cb/Cr 4:2:2 (ITU-R BT.656)

    Time base corrector

    Embedded 32-bit RISC encode control processor

Audio encode engine:

    MPEG1 audio layer 2 standard

    LPCM for DVD/D-VHS

    Supports sample rate conversion

    Dolby Digital consumer encode (family option)

MPEG stream processor:

    MPEG2-PS, MPEG2-TS and MPEG1-System demultiplexing

    Supports DVD-Video, DVD-Video recording and VCD

    Integrated CSS and CPPM decryption

    Integrated CPRM and DES for encryption / decryption

    Integrated Multi-2 and DVB descrambler

    Multiplex support for format conversion

    Demultiplex support

    Partial TS generation

    Stream interfaces

        Two 8-bit parallel ports

        Two serial ports

MPEG video decode engine:

    MPEG2 video MP@ML, SP@ML standard and MPEG1 standard

    Supports double decode capability for trick play

    JPEG decode accelerator

Audio decode engine:

    MPEG1 audio layer 1/2 standard

    LPCM for DVD/D-VHS

    Dolby Digital 5.1 channel decode (family option)

    DTS (family option)

    MP3 (family option)

    WMA (family option)

    Supports virtual surround

    Supports mixing of test tone, attenuation

Display/graphics BitBlt engine:

    7 graphics planes

    256-level alpha blending between all planes

    Simultaneous interlace and progressive video output

    Motion adaptive 3D-NR and motion adaptive De-interlacer

    Clipping functions for OSD

    Color space and color depth conversion function

    Two independent real-time scalars plus offline scalers for both OSD planes

    Sub-picture decoding and scaling functions

Video encoder:

    Six 54 MHz 10-bit DACs for analog YPbPr (or YCbCr or RGB), S-Video (Y/C) and CVBS video output.

    NTSC, PAL and SECAM standards

    Support for L21 data, Teletext, WSS, VBID, and VPS

External audio/video port:

    1 video/stereo audio input port for MPEG2 audio/video encode engine

    1 video/stereo audio I/O port for external DV codec device

    1 video output port for external video encoder device

    Multi-channel output port for audio DAC device

    IEC60958 output port

    Supported video formats:

    ITU-R BT.656

    ITU-R BT.1358

PCI interface:

    3.3 V 33 MHz 32-bit PCI 2.2

    Initiator/Target

    2 target windows

    Boot across PCI

IDE interface:

    Supports two IDE interfaces for up to four IDE drives

    UATA100/66/33, bus master IDE and PIO modes

    2 IDE I/F Supports

Peripherals:

    Supports one MultiMediaCard™/Secure Digital Memory Card interface

    Supports one Memory Stick™ interface

    Two 16550 UARTs with 16-byte FIFOs

    Two asynchronous UARTs

    Supports one clocked serial interface (CSI)

    Two ISO-7816-compliant SmartCard interfaces

    Two I^2C-compatible multi-master interfaces

    General purpose I/O

    Four timers supporting input capture/output compare

    Two system timers, an elapse timer, a (volatile) real-time clock and a watch-dog timer

Physical:

    Power :   2.5 W (TYP)

    Power supply voltage : 3.3 V I/O

                           2.5 V I/O for DDR SDRAM interface

                           1.5 V for core logic

Package:

    449-pin Plastic BGA (27 $\times$ 27 mm)

1. FUNCTIONAL DESCRIPTION

1.1   Overview

The functionality of the device can be divided into the following areas:

CPU core
MPEG AV encoder
MPEG stream processor
MPEG video decoder
MPEG audio decoder/processor
External A/V input/output
Graphics processor
Video encoder
Miscellaneous interfaces

1.2   Block Diagram
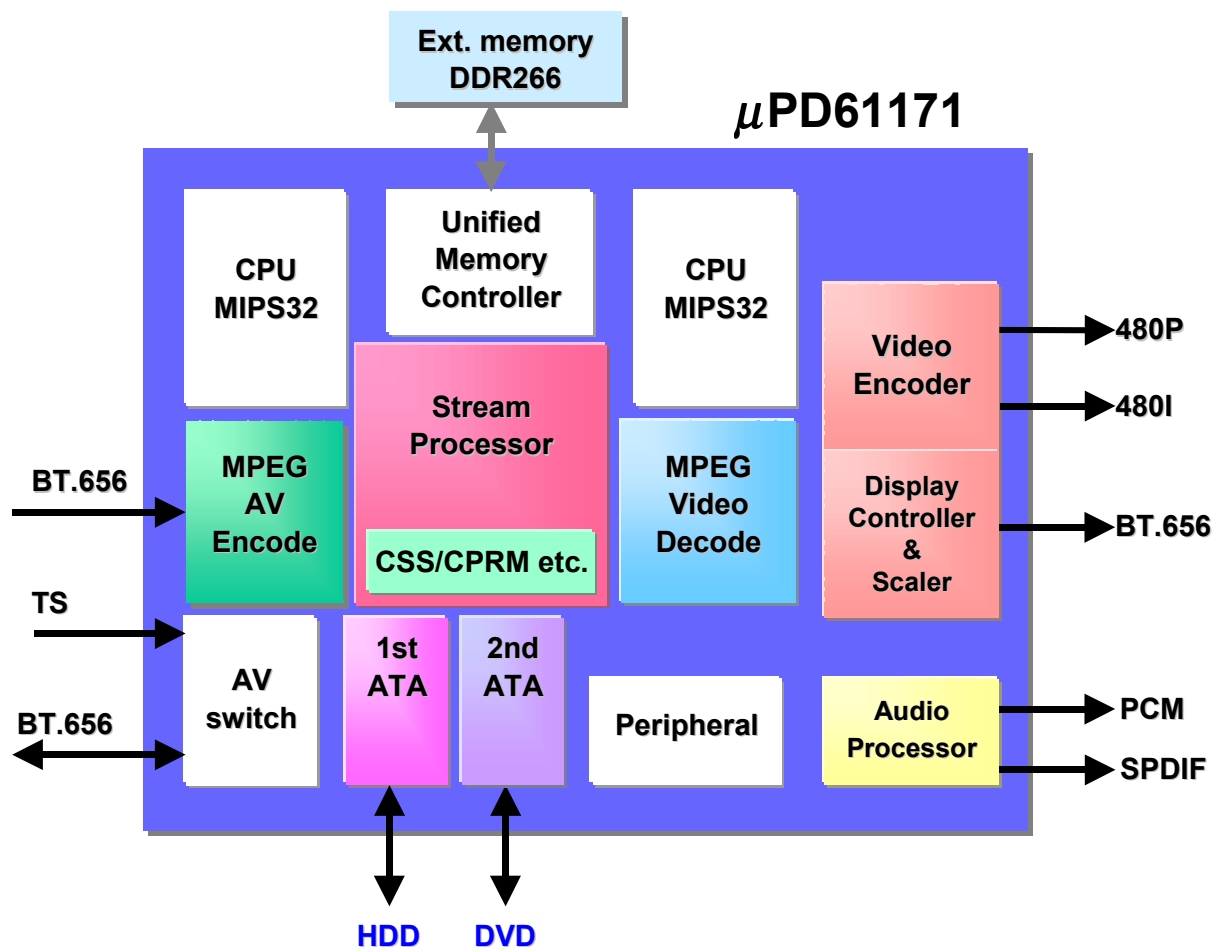
2. PACKAGE DRAWING

449-PIN PLASTIC BGA (27x27)

INDEX MARK
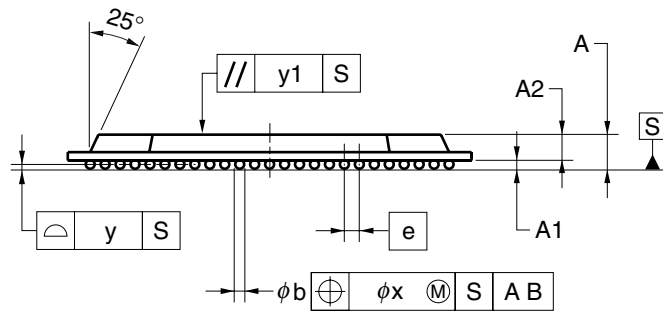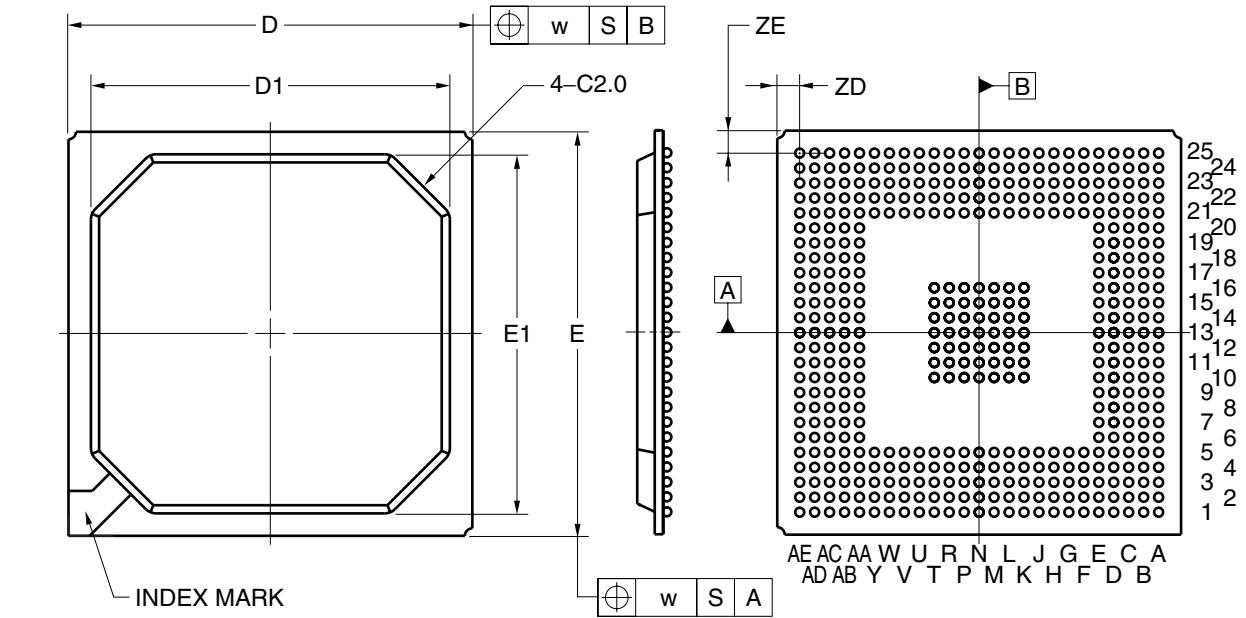
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E	27.00±0.20
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w	0.30
e	1.00
A	2.23±0.30
A1	0.50±0.10
A2	1.73
b	0.60±0.10
x	0.15
y	0.15
y1	0.35
ZD	1.50
ZE	1.50

P449F1-100-MN2-1

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