NEC

MOS INTEGRATED CIRCUIT

μPD63210,63210L

16-BIT D/A CONVERTER WITH BUILT-IN DIGITAL FILTER FOR AUDIO

DESCRIPTION

The μPD63210 is a 16-bit dual D/A converter IC for digital audio demodulation, which incorporates an 8-times oversampling digital filter and operational amplifiers for analog post filters. With few external parts and an easy substrate design (as to 1-bit D/A), it is suitable for multimedia terminals, MPEG audio equipment, video CDs, game machines, and electronic musical instruments, etc. To cope with sets for portable applications, a low-voltage operating version μPD63210L (lowest operating supply voltage = +3.0 V) is also available.

FEATURES

- 16-bit resistor string D/A converter (2-channel) adopted
  S/N = 104 dBTYP.; DR = 96 dBTYP. (when V_{DD} = 5.0 V)
- High-performance 8-times oversampling digital filter incorporated
  Pass band ripple : ±0.003 dB
  Stop band rejection : 90 dB
- System clock 384/512fs selectable
- Serial input data format selectable
  Format for 2'S compliment, MSB first, and backward justification data accommodated;
  Input can be selected between 16- and 18 bits
- Full line of low-voltage operating products (μPD63210L)
  μPD63210 : V_{DD} = 4.5 to 5.5 V
  μPD63210L : V_{DD} = 3.0 to 5.5 V
- Wide operating temperature range (T_A = –40 to +85 °C)
- Operational amplifier (2-channel) for D/A converter output incorporated
- Operational amplifier (2-channel) for post filter (LPF) configuration incorporated
- Digital de-emphasis function (fs = 32/44.1/48 kHz) incorporated
- Soft mute function incorporated
- CD double-speed playback function (when μPD63210: 384fs)
- 28-pin plastic SOP (375 mil) adopted

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD63210GT	28-pin plastic SOP (375 mil)	Standard
μPD63210LGT	28-pin plastic SOP (375 mil)	

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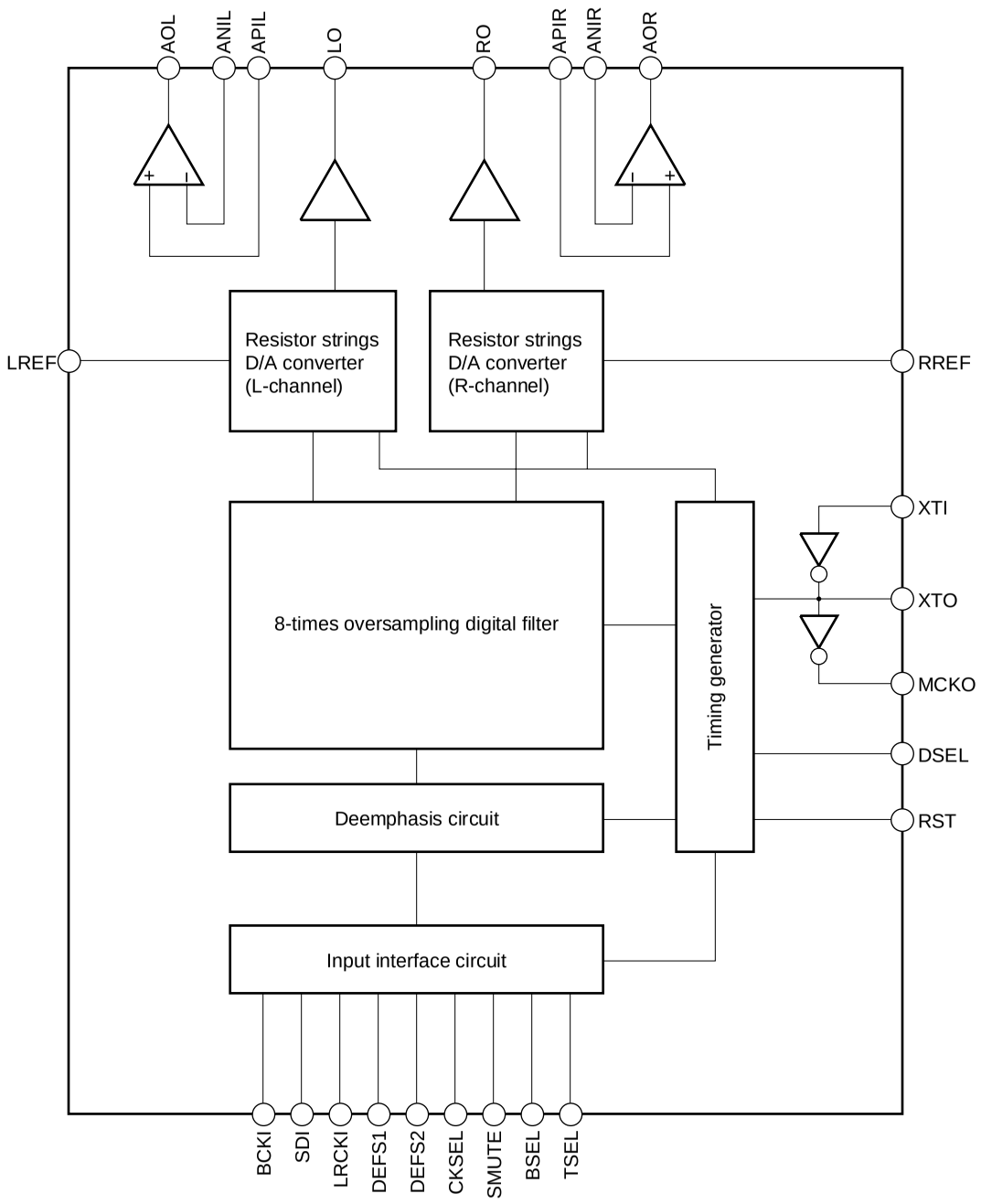
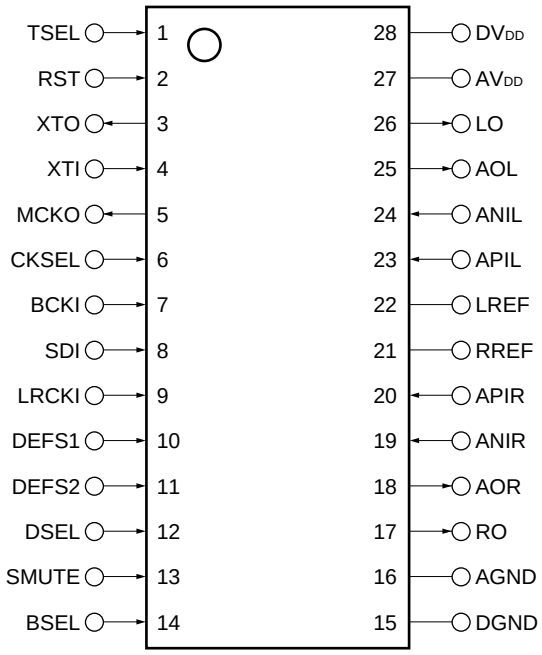
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



TSEL : Test selection input
RST : Reset input
XTO : Oscillation part output pin
XTI : Oscillation part input pin
MCKO : Master clock output
CKSEL : Clock selection input
BCKI : Bit clock input
SDI : Serial data input
LRCKI : LR clock input
DEFS1 : De-emphasis select input 1
DEFS2 : De-emphasis select input 2
DSEL : Double-speed playback select input
SMUTE : Soft mute control input
BSEL : Data bit count select input

DGND : Digital ground
AGND : Analog ground
RO : D/A converter output (R channel)
AOR : Filter amplifier output (R channel)
ANIR : Filter amplifier inverting input (R channel)
APIR : Filter amplifier non-inverting input (R channel)
RREF : Reference (R channel)
LREF : Reference (L channel)
APIL : Filter amplifier non-inverting input (L channel)
ANIL : Filter amplifier inverting input (L channel)
AOL : Filter amplifier output (L channel)
LO : D/A converter output (L channel)
AV_{DD} : Analog power supply
DV_{DD} : Digital power supply

1. PIN FUNCTIONS

Table 1-1. List of Pin Functions

Pin No.	Symbol	I/O	Function	Description
1	TSEL	I	Test selection	Normal operation: L
2	RST	I	Reset pin	H: System reset "H" period > 1/128fs **Example**: 0.18 μs or more when fs = 44.1 kHz
3	XTO	O	Oscillation part output pin	
4	XTI	I	Oscillation part input pin	
5	MCKO	O	Master clock output	
6	CKSEL	I	Clock selection	H: 512fs, L: 384fs
7	BCKI	I	Bit clock input	Refer to timing chart
8	SDI	I	Data input	
9	LRCKI	I	LR clock input	
10	DEFS1	I	De-emphasis switching 1	DEFS1 \ DEFS2: L / H L: OFF / 44.1 kHz H: 48.0 kHz / 32.0 kHz
11	DEFS2	I	De-emphasis switching 2	
12	DSEL	I	Double-speed playback switching	H: Double speed accommodated; L: Normal "H" can be selected only when using the μPD63210GT in 384fs mode (CKSEL = L) (double-speed operation assured).
13	SMUTE	I	Soft mute selection	Attenuated at the rising edge. Amplified at the trailing edge. MUTE OFF at "L".
14	BSEL	I	Bit selection	H: 18 bits; L: 16 bits
15	DGND	–	Digital GND	
16	AGND	–	Analog GND	
17	RO	O	DAC output Rch	
18	AOR	O	Filter amplifier output Rch	
19	ANIR	I	Filter amplifier inverting input Rch	
20	APIR	I	Filter amplifier non-inverting input Rch	
21	RREF	–	Rch reference pin	
22	LREF	–	Lch reference pin	
23	APIL	I	Filter amplifier non-inverting input Lch	
24	ANIL	I	Filter amplifier inverting input Lch	
25	AOL	O	Filter amplifier output Lch	
26	LO	O	DAC output Lch	
27	AV_{DD}	–	Analog V_{DD}	
28	DV_{DD}	–	Digital V_{DD}	

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, DGND = AGND = 0V unless otherwise specified)

Parameter	Symbol	Rating	Unit
Supply voltage	DV_{DD}, AV_{DD}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to DV_{DD} +0.3	V
Permissive dissipation	P_D	285 (T_a = 85 °C)	mW
Storage temperature	T_{stg}	–40 to +125	°C

Recommended Operating Range (DGND = AGND = 0V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	DV_{DD}, AV_{DD}	μPD63210	4.5	5.0	5.5	V
		μPD63210L	3.0	3.3	5.5	
Operating temperature	T_{opt}		–40	+25	+85	°C
Output load resistance	R_L	μPD63210; 17,18,25,26 pins	5			kΩ
		μPD63210L; 17,18,25,26 pins	10			

ELECTRICAL SPECIFICATIONS

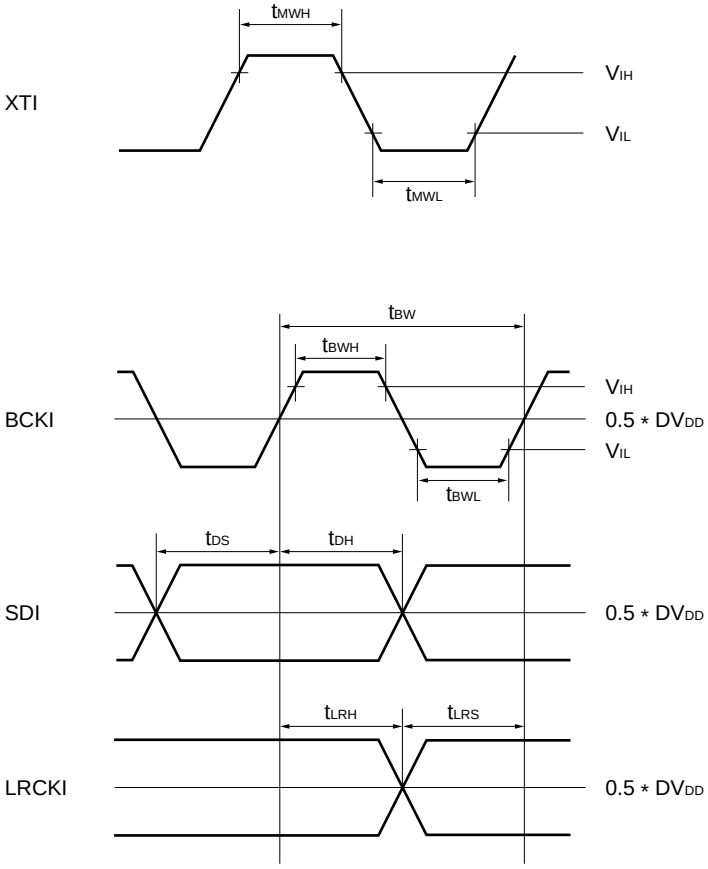
DC Characteristics (μPD63210: DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, T_a = –40 to +85 °C unless otherwise specified)

(μPD63210L: DV_{DD} = AV_{DD} = 3.0 to 5.5 V, DGND = AGND = 0 V, T_a = –40 to +85 °C unless otherwise specified)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	1, 2, 6, 7, 8, 9, 10, 11, 12, 13, and 14 pins	0.7DV_{DD}			V
Low-level input voltage	V_{IL}	1, 2, 6, 7, 8, 9, 10, 11, 12, 13, and 14 pins			0.3DV_{DD}	V
Input leakage current	I_L	1, 2, 6, 7, 8, 9, 10, 11, 12, 13, and 14 pins, T_a = 25 °C	–1.2	–	+1.2	μA
High-level output voltage	V_{OH}	5 pin, I_{OH} = –2.0 mA	DV_{DD}–0.4			V
Low-level output voltage	V_{OL}	5 pin, I_{OL} = 2.0 mA			+0.4	V
Current consumption (total)	I_{DD}	DV_{DD} = AV_{DD} = 5.0 V		24	50	mA
		DV_{DD} = AV_{DD} = 3.3 V (μPD63210L)		14	50	mA

AC Characteristics (μPD63210: DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, T_a = –40 to +85 °C unless otherwise specified)
(μPD63210L: DV_{DD} = AV_{DD} = 3.0 to 5.5 V, DGND = AGND = 0 V, T_a = –40 to +85 °C unless otherwise specified)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_X	Crystal oscillation: 384fs;	10	16.9344	19.2	MHz
		512fs	10	22.5792	25.6	MHz
Master clock frequency	f_{MCK}	External clock input: 384fs;	10	16.9344	19.2	MHz
		512fs	10	22.5792	25.6	MHz
Master clock pulse width ("H" section)	t_{MWH}	External clock input: 384fs;	25			ns
		512fs	19			ns
Master clock pulse width ("L" section)	t_{MWL}	External clock input: 384fs;	25			ns
		512fs	19			ns
BCK pulse width ("H" section)	t_{BWH}		150			ns
BCK pulse width ("L" section)	t_{BWL}		150			ns
BCK pulse cycle	t_{BW}		310			ns
Data setup time	t_{DS}		100			ns
Data hold time	t_{DH}		100			ns
LRCK setup time	t_{LRS}		100			ns
LRCK hold time	t_{LRH}		100			ns
SMUTE pulse width ("H" section)	t_{SMWH}		8/fs			



D/A Converter Characteristics

μPD63210 (T_A = 25 °C, DV_{DD} = AV_{DD} = 5.0 V, DGND = AGND =0 V, f_x = 16.933 MHz f_s = 44.1 kHz, 16 bits, DAC output)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RES			16		Bit
Noise distortion rate	THD	f_{IN} = 1 kHz, 0 dB		0.025	0.09	%
Full-scale output voltage	V_{FS}	17-/26-pins, f_{IN} = 1 KHz	1.7	2.0	2.3	V_{P-P}
S/N ratio	S/N	JIS-A filter	98	104		dB
Crosstalk	C.T	Single-channel 0dB, f_{IN} = 1 KHz	93	98		dB
Dynamic range	D.R	f_{IN} = 1 kHz, –60 dB	92	96		dB
LPF amplifier output voltage swing	V_{AOH}	$R_L \geq 5$ kΩ	4.75	4.92		V
LPF amplifier output voltage swing	V_{AOL}	$R_L \geq 5$ kΩ		0.02	0.25	V

μPD63210L (T_A = 25 °C, DV_{DD} = AV_{DD} = 3.3 V, DGND = AGND =0 V, f_x = 16.9344 MHz f_s = 44.1 kHz, 16 bits, DAC output)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RES			16		Bit
Noise distortion rate	THD	f_{IN} = 1 kHz, 0 dB		0.03	0.09	%
Full-scale output voltage	V_{FS}	17-/26-pins, f_{IN} = 1 KHz	1.12	1.32	1.52	V_{P-P}
S/N ratio	S/N	JIS-A filter	94	100		dB
Crosstalk	C.T	Single-channel 0dB, f_{IN} = 1 KHz	90	96		dB
Dynamic range	D.R	f_{IN} = 1 kHz, –60 dB	89	94		dB
LPF amplifier output voltage swing	V_{AOH}	$R_L \geq 10$ kΩ	3.05	3.22		V
LPF amplifier output voltage swing	V_{AOL}	$R_L \geq 10$ kΩ		0.02	0.25	V

3. OPERATION

3.1 Operation Clock

(1) Selection of system clocks

System clocks are selected by the CKSEL (No.6) pin.

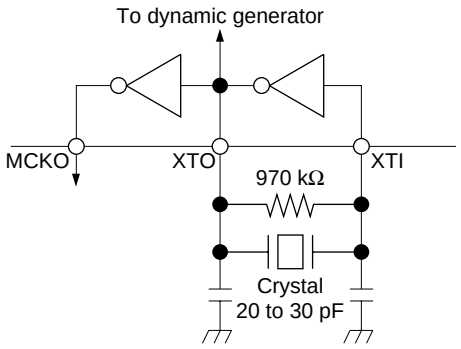
Table 3-1. Selection of System Clocks

System Clock	CKSEL
384fs	L
512fs	H

(2) Generation of operation clock

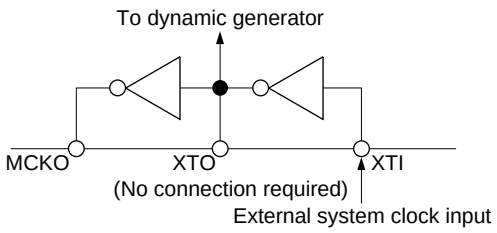
The clock required for internal operation can be generated by configuring a crystal oscillator circuit as shown in Figure 3-1.

Figure 3-1. Crystal Oscillator Circuit Configuration



As in Figure 3-2, the clock can also be generated by supplying a system clock from outside to the XTI (No.4) pin. The system clock waveform at this time must satisfy the conditions in the electrical specifications (such as V_{IH}, V_{IL} under DC characteristics; and t_{MCK}, t_{MWH}M, t_{MWL} under AC characteristics).

Figure 3-2. Configuration When Providing System Clock Externally



3.2 Data Input Circuit

(1) Input data format

Data on MSB first, 2's compliment, and backward justification is input.

(2) Selection of input data bit length

An input data bit length is selected by the BSEL (No.14) pin.

Table 3-2. Selection of Input Data Bit Length

Input Data Bit Length	BSEL
16 bits	L
18 bits	H

(3) Data input timing chart

SDI and LRCKI is incorporated in the internal shift register at the rising edge of BCKI. The SDI, LRCKI, and BCKI waveforms must satisfy the conditions in the electrical specifications (such as V_{IH}, V_{IL} under DC characteristics; and t_{BWH}, t_{BWL}, t_{BW}, t_{DS}, t_{DH}, t_{LRS}, and t_{LRH} under AC characteristics).
SDI considers the 16 bits (when BSEL = L; 18 bits when BSEL = H) preceding the change point of LRCKI to be valid data.

Regarding the combination of system clock selection and input data length selection, the conditions for inputtable BCKI are shown in Table 3-3.

Table 3-3. Limitations on BCKI

BCKI	384fs (CKSEL = L)		512fs (CKSEL = H)	
	16 bits (BSEL = L)	18 bits (BSEL = H)	16 bits (BSEL = L)	18 bits (BSEL = H)
32fs	○	–	○	–
48fs	○	○	–	–
64fs	○	○	○	○

The data input timing charts are shown in Figure 3-3 and Figure 3-4.

Figure 3-3. Data Input Timing Chart (when BSEL = L)

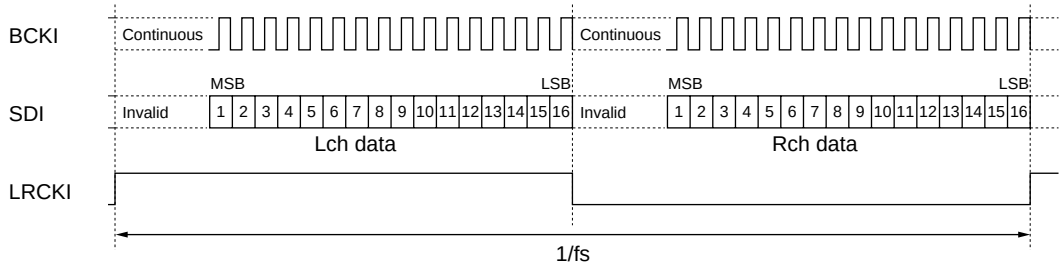
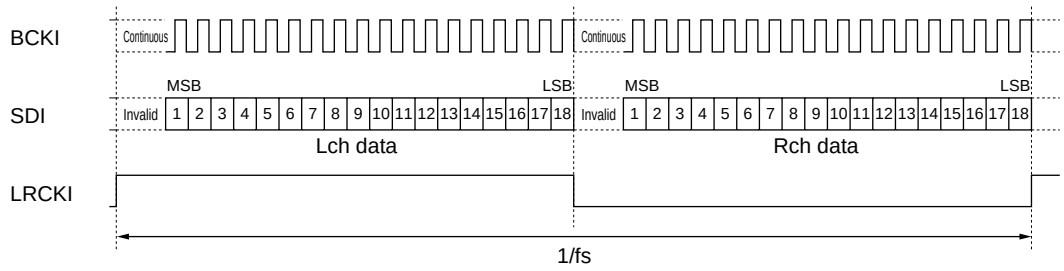


Figure 3-4. Data Input Timing Chart (when BSEL = H)



3.3 Digital Filter

The 8-times oversampling FIR digital filter is used to attenuate the image out of band noise component, thus facilitating the analog filter designing.

The configuration of the digital filter is shown in Figure 3-5. The characteristics of the digital filter are shown in Figures 3-6 and 3-7.

Figure 3-5. Configuration of Digital Filter

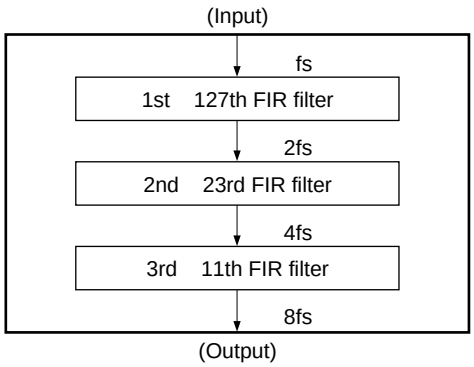


Figure 3-6. Frequency Characteristics of Digital Filter

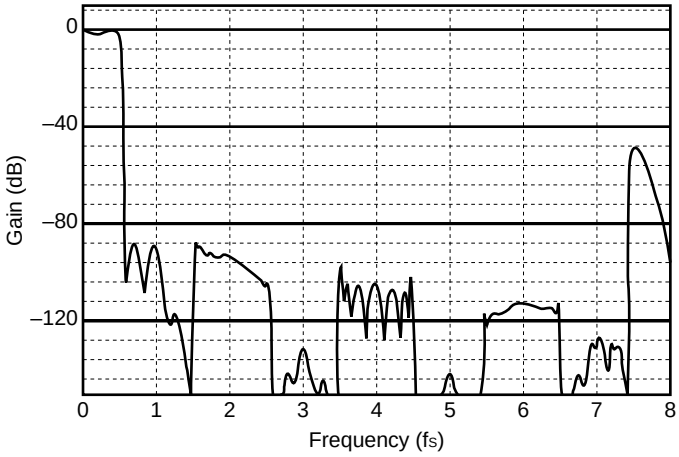
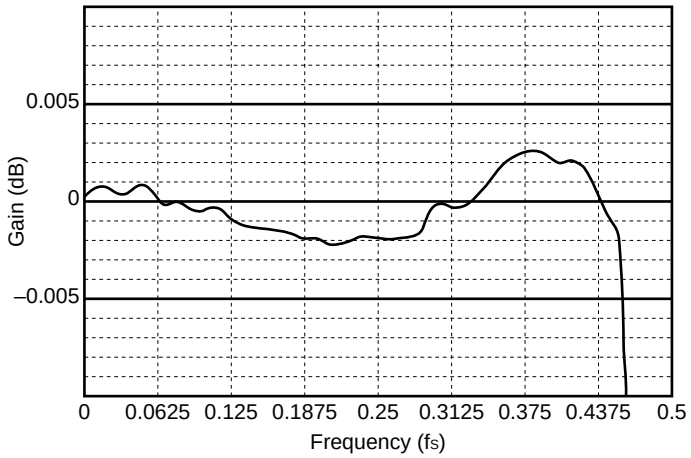


Figure 3-7. Intraband Ripple Characteristics of Digital Filter



3.4 Digital De-emphasis Function

The IIR digital filter performs de-emphasis operations. The filter can cope with three types of sampling frequencies (32/44.1/48 KHz) by using the DEFS1 (No.10) and DEFS2 (No.11) pins.

Table 3-4. Selection of De-emphasis Filter

De-emphasis	DEFS1	DEFS2
OFF	L	L
32 kHz	H	H
44.1 kHz	L	H
48 kHz	H	L

3.5 Soft Mute Function

The soft mute function can be realized by control of the SMUTE (No.13) pin.

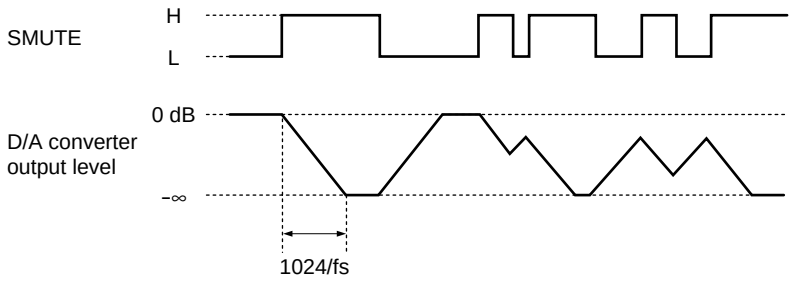
When applying the mute, set the value to SMUTE = H. By this, the output level of the D/A converter is attenuated from 0dB to negative infinity (-∞) in 128 steps. The time required for a complete mute is 1024/fs.

When cancelling the mute, set the value to SMUTE = L. By this, the output level of the D/A converter is increased from negative infinity (-∞) to 0dB in 128 steps. Figure 3-8 shows the relationship between the control of the SMUTE pin and the output level of the D/A converter.

When initializing by resetting the system, the mute is cancelled and the output level of the D/A converter reaches the maximum (0dB).

Don't input the narrower "H" pulse than 8/fs to pin 13, or analog output signal may become unstable. In this case, the unstable condition may be kept until system reset or power off.

Figure 3-8. Operation of Soft Mute Function



3.6 CD Double-Speed Playback Function (μPD63210 only)

The CD double-speed playback function can be selected by the DSEL (No.12) pin. For selection of the system clock, please set the value to 384 fs (CKSEL = L). The μPD63210L does not have this function.

Table 3-5. System Clock Selection in Normal/Double-Speed Playback

Parameter	DSEL	
	L (Normal)	H (Double-speed)
XTI input clock frequency	384fs	192fs
XTI frequency in CD playback	16.9344 MHz (fs = 44.1 kHz)	16.9344 MHz (fs = 88.2 kHz)
MCKO output clock frequency	384fs	192fs

3.7 System Reset

The system is reset by inputting the H pulse into the RST (No.2) pin. The high level width to be input should be at least 1/128 fs. For example, if fs = 44.1 KHz, the system reset can be executed by entering the H signal whose pulse is at least 0.18 μs wide.

3.8 Configuration of Analog LPF

Because the stop band rejection of the built-in 8-times oversampling digital filter is large (90 dB), the configuration of the analog LPF can be simple. Furthermore, by incorporating the output buffer (BUFF) of the D/A converter and the operational amplifier for LPF configuration, an analog LPF can be configured based on an extremely small number of external components. LPF's cutoff frequency can be set with an external constant in accordance with the sampling frequency.

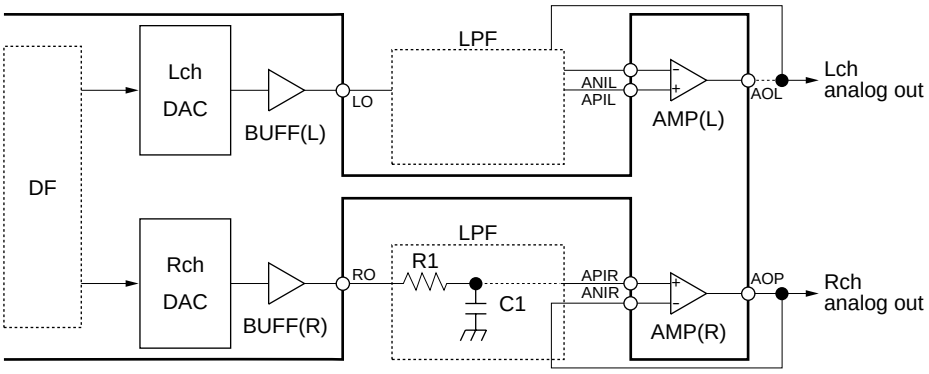
Figure 3-9 shows the configuration of the D/A converter output section. As such, an LPF is configured by inserting an RC circuit between the BUFF output and AMP input. This diagram shows an example of configuring a Butterworth filter whose gain is 0 dB.

In this case, R1 becomes the load of the BUFF output pin; therefore, ensure that the selection satisfies the electrical specifications (RL of the recommended operation range).

LPF Configuration Example

Conditions			Parts constants
Cutoff frequency	: fc = 30 kHz	→	R1 = 7.5 kΩ
Configuration	: Primary Butterworth		C1 = 680 pF
Gain	: 0 dB		
IC used	: μPD63210		

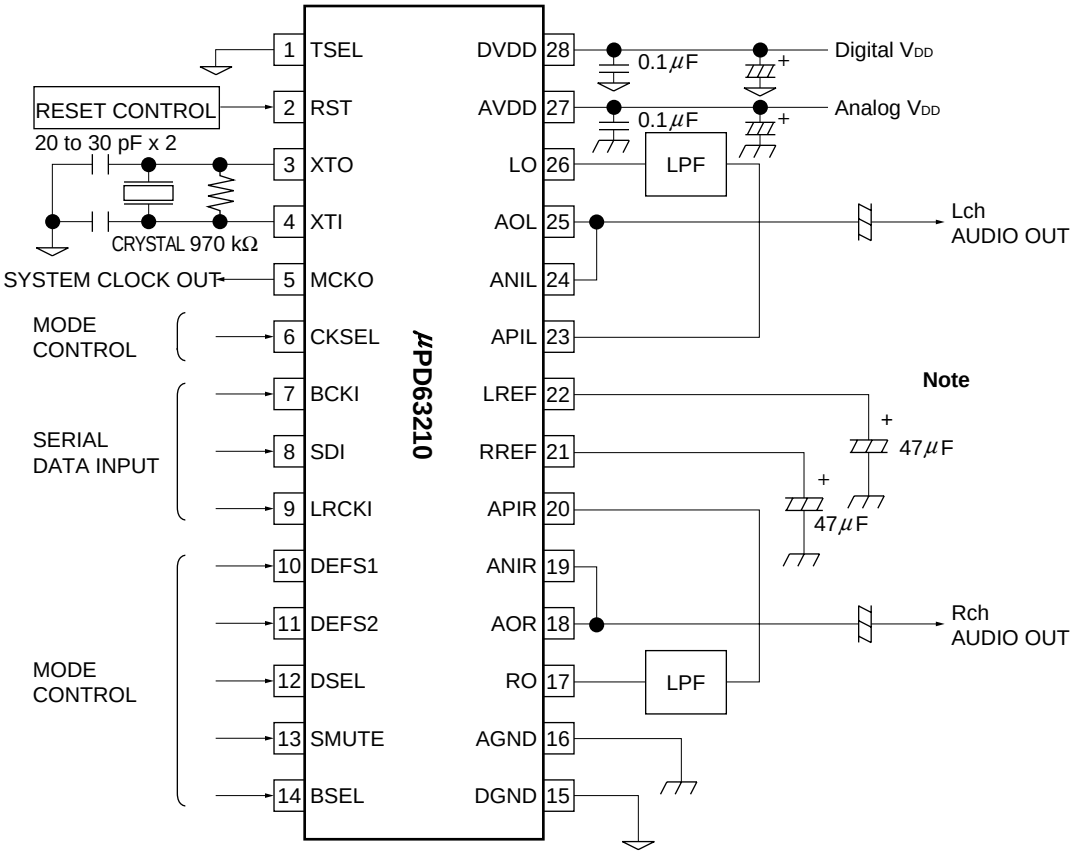
Figure 3-9. Configuration of D/A Converter Output Section (Configuration of Analog LPF)



4. APPLICATION CIRCUIT EXAMPLE

An application circuit example in using crystal oscillation circuits is shown in Figure 4-1.

Figure 4-1. Application Circuit Example in Using Crystal Oscillation Circuits



Note In this example, reference capacitors (21-/22-pin external capacitors) are installed independently. Even if these are realized in a common system (one 47μF), they will not cause any operational problems. However, the crosstalk may be deteriorated slightly (by several dB); therefore, please decide after evaluating the samples provided.

5. CAUTIONS

(1) Shock noise countermeasure

It is recommended that the analog mute circuit be connected to the next stage before using the converter. Without a mute circuit, shock noises may occur when the power is turned on.

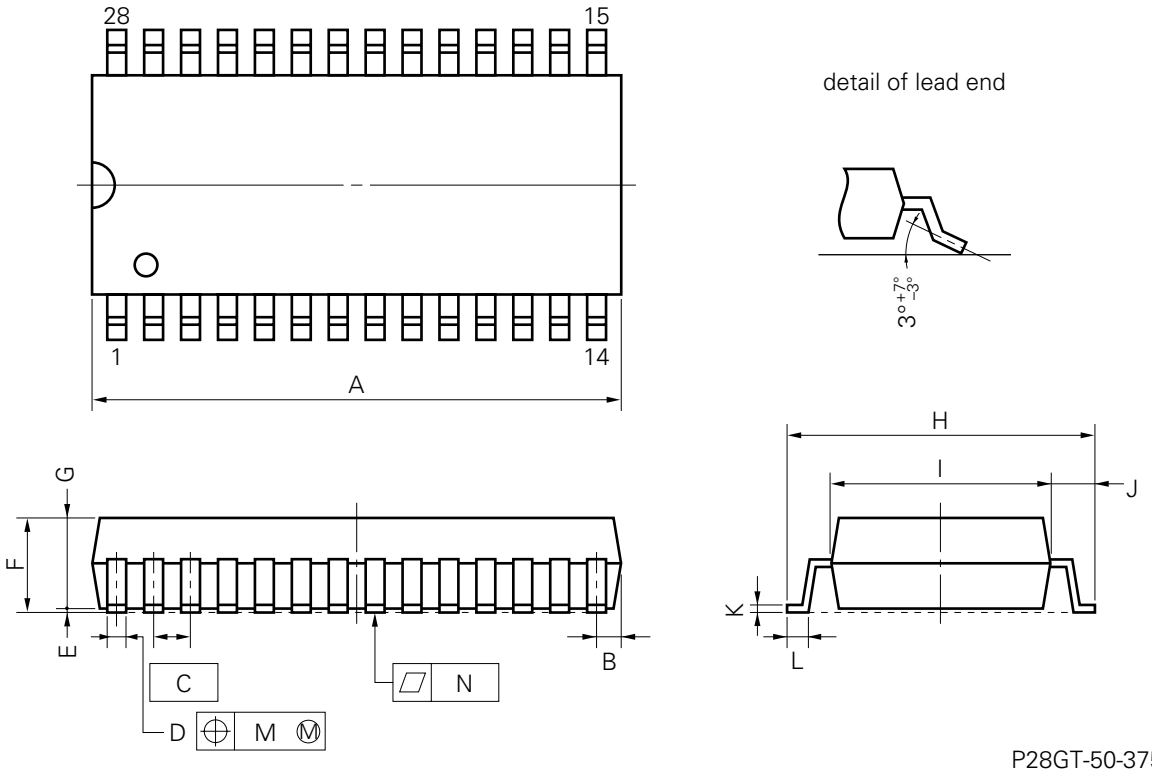
(2) Resetting

Reset the system when switching over the input data bit length, the system clock, the digital deemphasis, or the CD double-speed playback.

System reset must be executed after both master clock and LR clock become stable. If master clock or LR clock becomes unstable after system reset, the analog output signal may be unstable.

6. PACKAGE DRAWING

28 PIN PLASTIC SOP (375 mil)



P28GT-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.2 MAX.	0.717 MAX.
B	0.845 MAX.	0.034 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.50±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2±0.2	$0.283^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

7. RECOMMENDED SOLDERING CONDITIONS

The solder mounting of this product should be conducted under the following conditions. For details of the recommended soldering conditions, please refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended, please contact an NEC salesperson.

Table 7-1. Soldering Conditions

μPD63210GT : 28-pin plastic SOP (375 mil)
μPD63210LGT : 28-pin plastic SOP (375 mil)

Soldering Method	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C; time: within 30 secs (at no lower than 210 °C); count: twice <Precautions> (1) The second reflow should be started after the temperature of the device, which would have changed due to the first reflow, has returned to normal. (2) Please avoid flux water washing after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C; time: within 40 secs (at no lower than 200 °C); count: once <Precautions> (1) The second reflow should be started after the temperature of the device, which would have changed due to the first reflow, has returned to normal. (2) Please avoid flux water washing after the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature: no higher than 260 °C, time: within 10 secs; count: once Preheating temperature: up to 120 °C (package surface temperature)	WS60-00-1
Pin part heating	Pin part temperature: no higher than 300 °C; time: within 3 secs (per device side)	–

Caution Please avoid using two or more soldering methods at the same time (except for the pin part heating method).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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