LED DOT DISPLAY DRIVER

The μPD6322C is a dot display driver of CMOS structure, designed to drive 24 LEDs for dot matrix display.

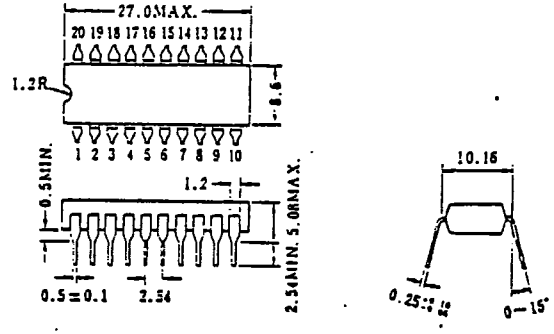
The driver is of a 20-pin DIP (Dual In-Line Package) construction and consists of a 5-bit parallel input circuit, a latch circuit, a 5 to 24 decoder and a LED driver.

The uPD6322C is best suited for analog display and preset station display in the digital tuning system to name a few of many other application.

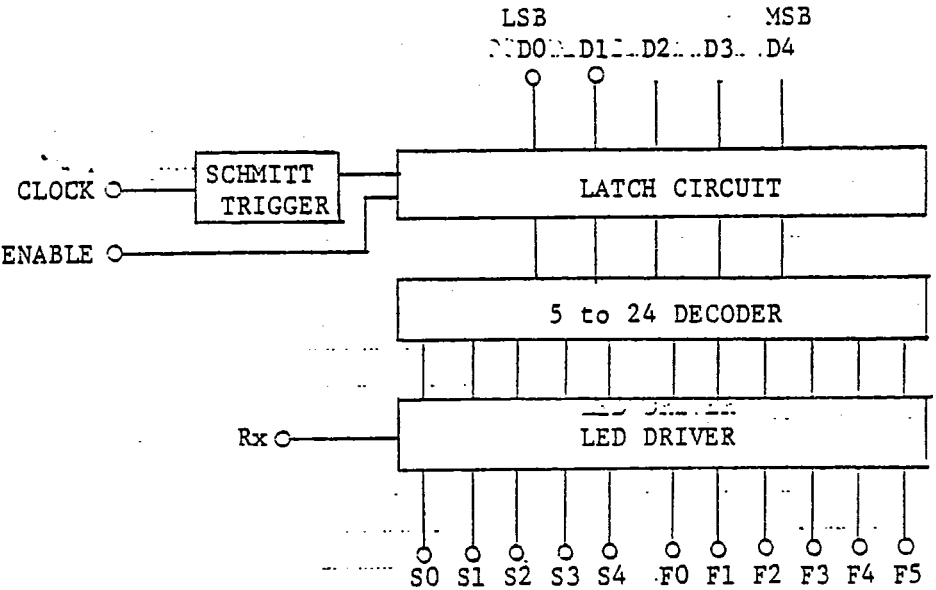
FEATURES

- o Single power supply : 5 V ± 10 %
- o Dot matrix display with 24 LEDs: 4 x 6 dot matrix
- o Green LED display is possible : 20 mA MAX.
- o Display current is adjustable with a single external resister.
- o Input latch is selectable (with ENABLE terminal).
- o Schmitt circuit is incorporated for clock input

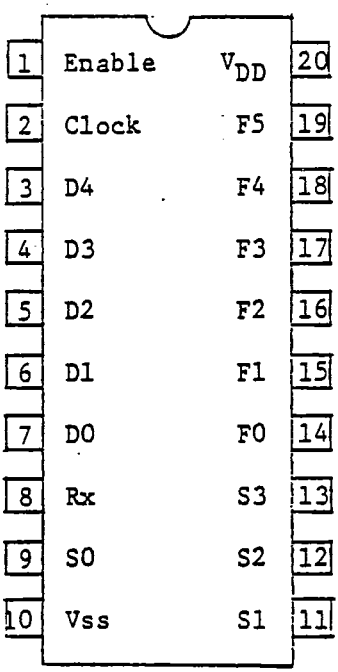
PACKAGE DIMENSIONS (Unit : mm)



BLOCK DIAGRAM



TERMINAL DIAGRAM



OPERATION

Truth Table

Input			Output
Enable	Clock	Data	Q_{n+1}
L	↑	H	H
L	↑	L	L
L	↓	X	Q_n
H	X	H	H
H	X	L	L

No Change

H: High level
L: Low level
X: H or L level

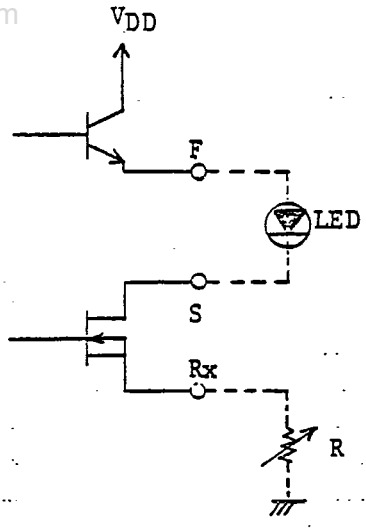
When the signal level at the ENABLE terminal (Pin No. 1) gose low, input data is latched at the leading edge of the CLOCK signal (at Pin No. 2). The data latched will remain unchanged at the High and Low levels of the CLOCK signal or at the traling edge of the same signal.

When the signal level at the ENABLE terminal goes high, the status of the CLOCK terminal is ignored and the output status varies with the status of input data. In this case, no input data is latched.

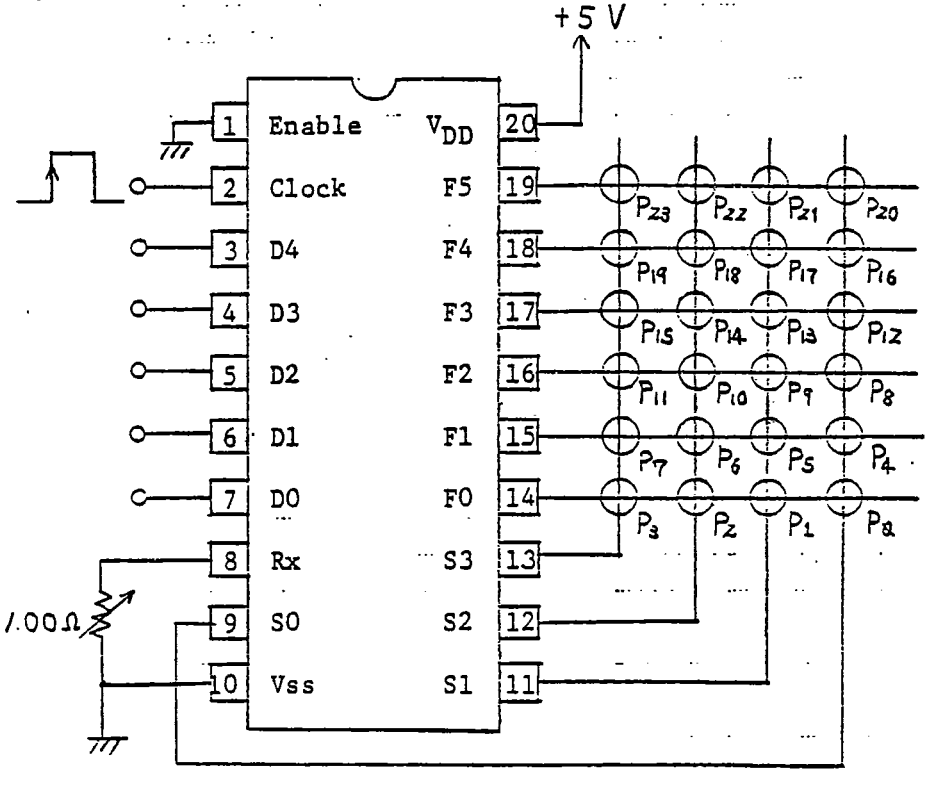
INPUT-OUTPUT TRUTH TABLE

	Input					Output										
	D4	D3	D2	D1	D0	F5	F4	F3	F2	F1	F0	S3	S2	S1	S0	Display
0	0	0	0	0	0	L	L	L	L	L	H				L	P0
1	0	0	0	0	1	L	L	L	L	L	H			L		P1
2	0	0	0	1	0	L	L	L	L	L	H		L			P2
3	0	0	0	1	1	L	L	L	L	L	H	L				P3
4	0	0	1	0	0	L	L	L	L	H	L				L	P4
5	0	0	1	0	1	L	L	L	L	H	L			L		P5
6	0	0	1	1	0	L	L	L	L	H	L		L			P6
7	0	0	1	1	1	L	L	L	L	H	L	L				P7
8	0	1	0	0	0	L	L	L	H	L	L				L	P8
9	0	1	0	0	1	L	L	L	H	L	L			L		P9
10	0	1	0	1	0	L	L	L	H	L	L		L			P10
11	0	1	0	1	1	L	L	L	H	L	L	L				P11
12	0	1	1	0	0	L	L	H	L	L	L				L	P12
13	0	1	1	0	1	L	L	H	L	L	L			L		P13
14	0	1	1	1	0	L	L	H	L	L	L		L			P14
15	0	1	1	1	1	L	L	H	L	L	L	L				P15
16	1	0	0	0	0	L	H	L	L	L	L				L	P16
17	1	0	0	0	1	L	H	L	L	L	L			L		P17
18	1	0	0	1	0	L	H	L	L	L	L		L			P18
19	1	0	0	1	1	L	H	L	L	L	L	L				P19
20	1	0	1	0	0	H	L	L	L	L	L				L	P20
21	1	0	1	0	1	H	L	L	L	L	L			L		P21
22	1	0	1	1	0	H	L	L	L	L	L		L			P22
23	1	0	1	1	1	H	L	L	L	L	L	L				P23
24	1	1	0	0	0	L	L	L	L	L	L					
25	1	1	0	0	1	L	L	L	L	L	L					
26	1	1	0	1	0	L	L	L	L	L	L					
27	1	1	0	1	1	L	L	L	L	L	L					
28	1	1	1	0	0	L	L	L	L	L	L					
29	1	1	1	0	1	L	L	L	L	L	L					
30	1	1	1	1	0	L	L	L	L	L	L					
31	1	1	1	1	1	L	L	L	L	L	L					

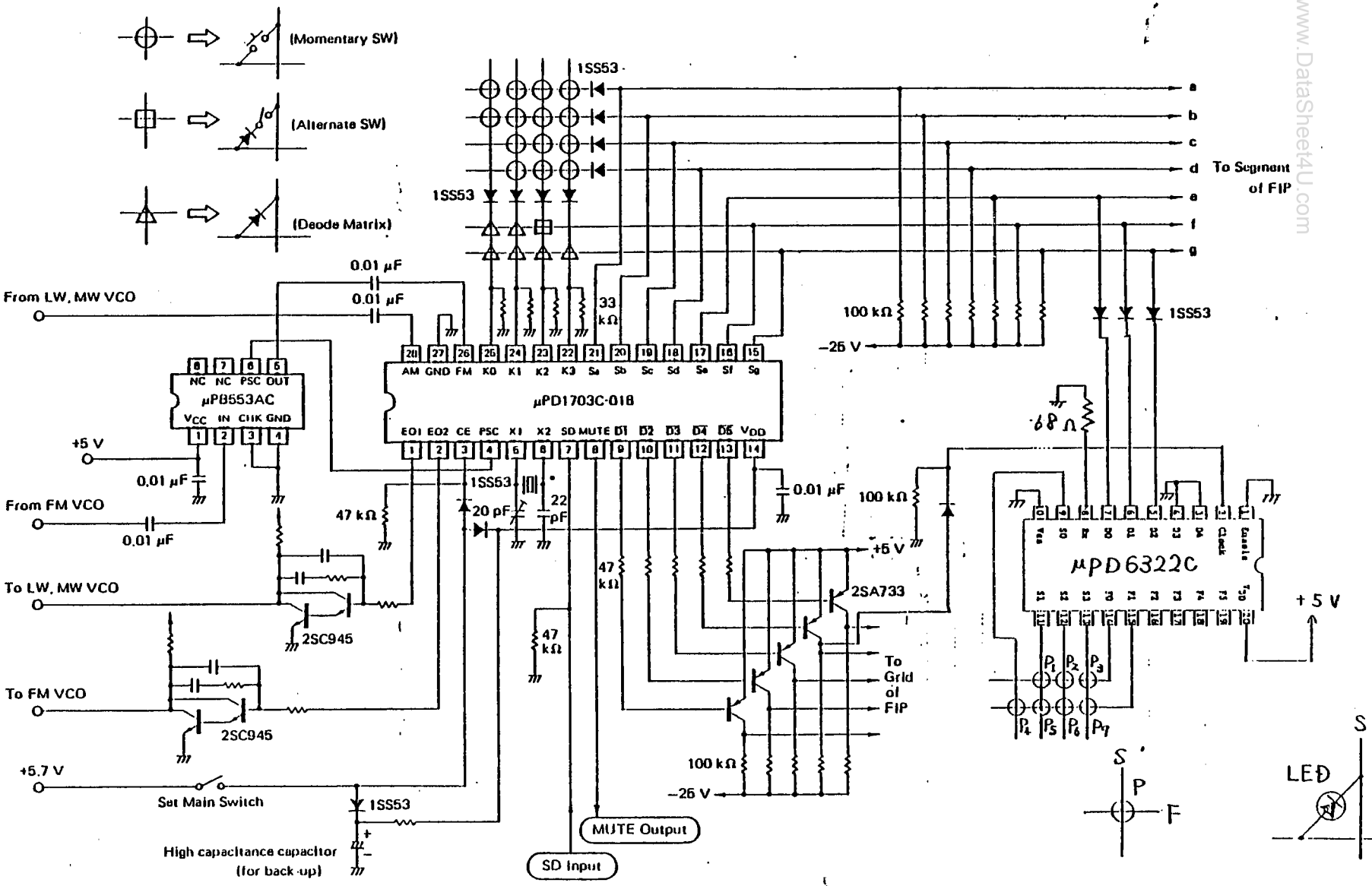
Output Circuit



Exampl of Connection



APPLICATION EXAMPLE OF CIRCUIT DIAGRAM



*4.5 MHz X'tal (Toyo Tsuhinki: TQC-231A-8C)

The applied circuits and circuit constants listed in this material are not intended for mass production design with deviations and temperature characteristics of component parts considered. Further, this company will not assume any responsibility as regards the patents on the circuits listed in this material.