NEC

MOS INTEGRATED CIRCUIT
μPD64082

THREE-DIMENSIONAL Y/C SEPARATION LSI

DESCRIPTION

The μPD64082 realizes a high precision Y/C separation and a noise reduction by the three-dimension signal processing for NTSC signal.

The three-dimension Y/C separation system can be easily realized with 4Mbit-EDO DRAM and A/D converter.

This product has a high precision 10-bit A/D converter internal, and 10-bit signal processing (only for luminance signal) for high picture quality.

This LSI includes the Wide Clear Vision ID signal decoder and Horizontal Helper signal decoder.

FEATURES

- Includes a high performance pipeline 10-bit A/D converter for composite and luminance signal, and 8-bit A/D converter for chroma signal processing.
- High resolution picture with 4 times of ratio in the previous system.
- Easy to make the three-dimension Y/C separation and YNR/CNR system with 4MBit-EDO DRAM.
- Includes system clock generator, 2-ch of A/D converter, and 2-ch of D/A converter.
- Includes HH decoder (Required the field memory).
- I^2C bus control.
- Single power supply of 3.3 V.

ORDERING INFORMATION

Part number	Package
μPD64082GF-3BA	100-pin plastic QFP (14 × 20)

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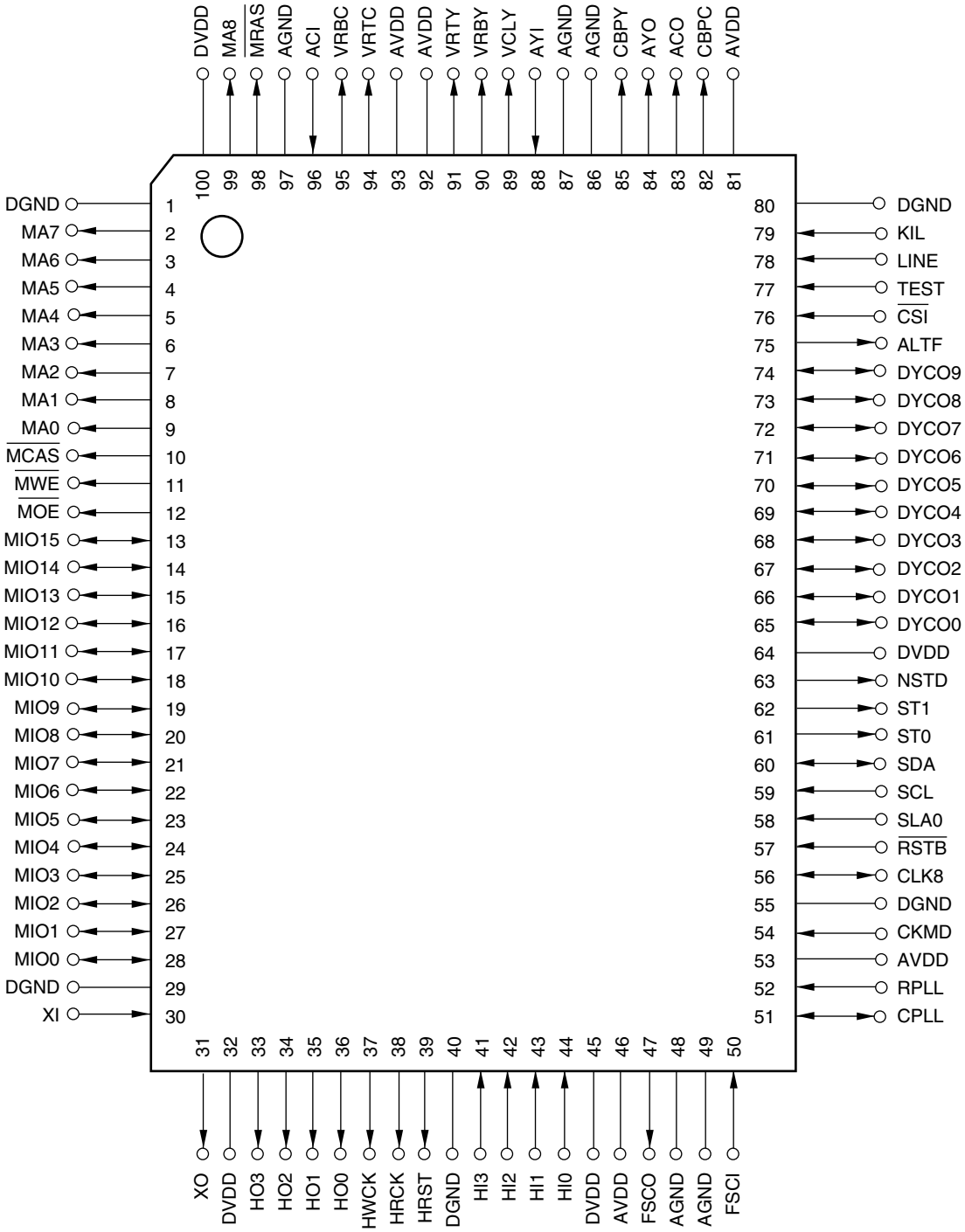
The mark ★ shows major revised points.

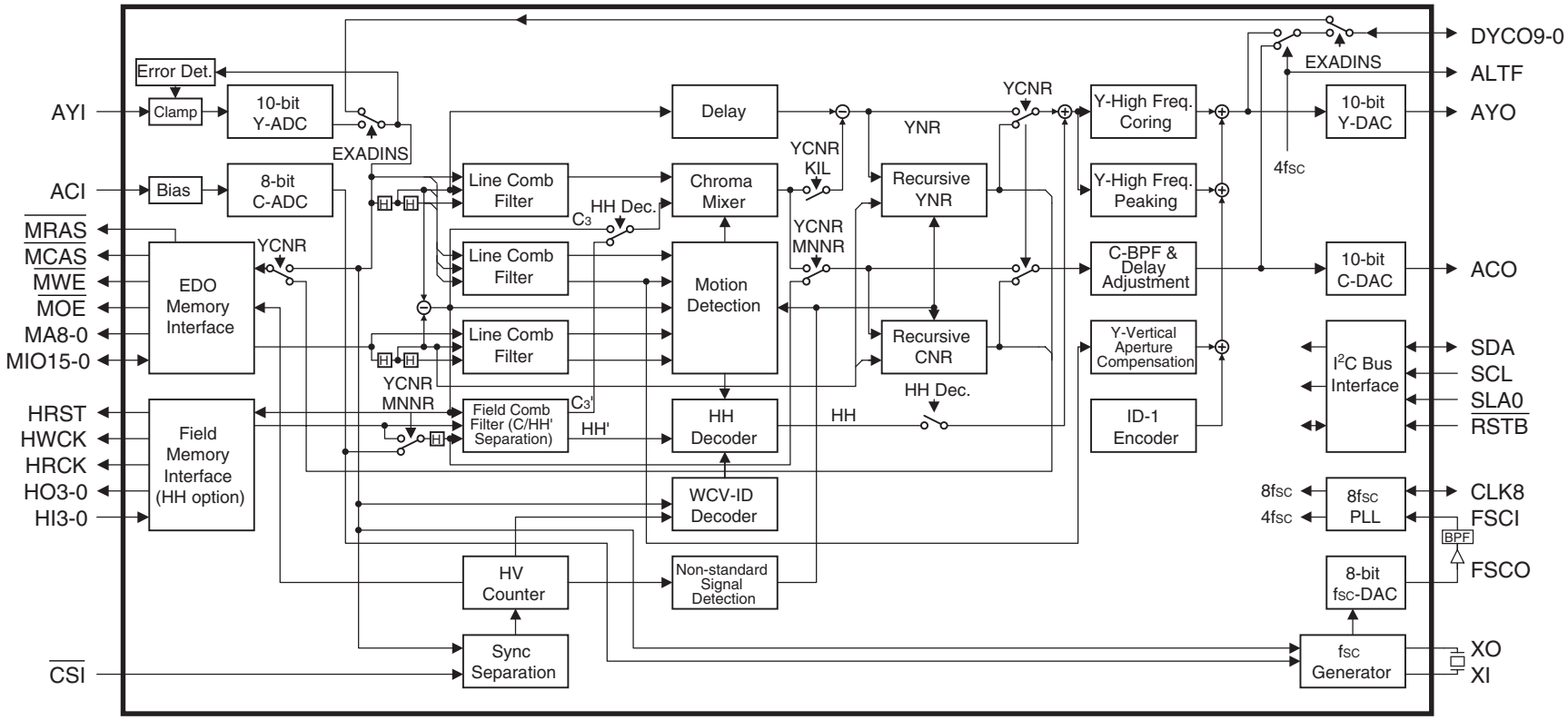
PIN CONFIGURATION (TOP VIEW)

- 100-pin plastic QFP (14 × 20)
  μPD64082GF-3BA



ACI	: Analog C (Chroma) Signal Input
ACO	: Analog C (Chroma) Signal Output
AGND	: Analog Section Ground
ALTF	: Alternate Flag for Digital Y/C Output
AVDD	: Analog Section Power Supply
AYI	: Analog Y (Luma) Signal Input
AYO	: Analog Y (Luma) Signal Output
CBPC	: C-DAC Phase Compensation Output
CBPY	: Y-DAC Phase Compensation Output
CKMD	: Clock Mode Selection
CLK8	: 8f_{SC} Clock Input / Output
CPLL	: Capacitor Connection for PLL
$\overline{\text{CSI}}$	: Composite Sync. Input (active-low)
DGND	: Digital Section Ground
DVDD	: Digital Section Power Supply
DYCO0 - DYCO9	: Digital Y/C Signal (Alternative) Outputs
FSCI	: f_{SC} (Subcarrier) Input
FSCO	: f_{SC} (Subcarrier) Output
HI3 - HI0	: Field Memory Inputs for HH Decoder
HO3 - HO0	: Field Memory Outputs for HH Decoder
HRCK	: Field Memory Read Clock for HH Decoder
HRST	: Field Memory Reset for HH Decoder
HWCK	: Field Memory Write Clock for HH Decoder
KIL	: Killer Selection
LINE	: Inter-Line Separate Selection
MA8 - MA0	: EDO Memory Address Outputs
$\overline{\text{MCAS}}$	: EDO Memory Column Address Strobe (active-low)
MIO15 - MIO0	: EDO Memory Data Inputs/Outputs
$\overline{\text{MOE}}$	: EDO Memory Output Enable (active-low)
$\overline{\text{MRAS}}$	: EDO Memory Row Address Strobe (active-low)
$\overline{\text{MWE}}$	: EDO Memory Write Enable (active-low)
NSTD	: Non Standard Detection Monitor
RPLL	: Testing Selection
$\overline{\text{RSTB}}$	: System Reset (active-low)
SCL	: Serial Clock Input
SDA	: Serial Data Input / Output
SLA0	: Slave Address Selection
ST1, ST0	: Inner States Monitor
TEST	: Testing Selection
VCLY	: Clamp Voltage Output for Y-ADC
VRTC	: Top Voltage Reference Output for C-ADC
VRTY	: Top Voltage Reference Output for Y-ADC
VRBC	: Bottom Voltage Reference Output for C-ADC
VRBY	: Bottom Voltage Reference Output for Y-ADC
XI	: X'TAL input
XO	: X'TAL output

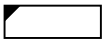
BLOCK DIAGRAM



TERMINOLOGY

This manual use the abbreviation listed below:

ADC	:	A/D (Analog to Digital) converter
DAC	:	D/A (Digital to Analog) converter
LPF	:	Low-pass filter
BPF	:	Band-pass filter
HPF	:	High-pass filter
Y signal, or Luma	:	Luminance, or luminance signal
C signal, or Chroma	:	Color signal, or chrominance signal
MN signal	:	MUSE-NTSC convert signal (Japan only)
f_{SC}	:	Color subcarrier frequency = 3.579545 MHz
$4f_{SC}$	:	4 times f_{SC}, burst locked clock = 14.318180 MHz
$8f_{SC}$	:	8 times f_{SC}, burst locked clock = 28.636360 MHz
f_H	:	Horizontal sync frequency = 15.734 kHz
$910f_H$	:	910 times f_H, line locked clock = 14.318180 MHz
$1820f_H$	:	1820 times f_H, line locked clock = 28.636360 MHz
f_V	:	Vertical sync frequency = 59.94 Hz
NR	:	Noise reduction
YNR	:	Luminance (Y) noise reduction
CNR	:	Chrominance (C) noise reduction
WCV-ID	:	Wide Clear Vision standard ID signal (Japan only)
HH	:	Horizontal Helper signal (Wide Clear Vision Standard category: Japan only)

In the following diagrams, a serial bus register is enclosed in a box: 

LIMITATION ITEMS

1. Clamp noise

Clamp noise (about 3 mV) appears in the sync-tip of luminance signal output.
Please make input signal (AYI: 88 pin) low impedance to decrease this noise.

2. $2f_{SC}$ noise

There is noise of the $2f_{SC}$ (7.2 MHz) component in the luminance signal output. This $2f_{SC}$ noise occurred by internal 10-bit A/D converter of the μPD64082.
Please consider to decrease this noise enough when you design output buffer and amplifier circuit.

[Other measures]

(a) Using coring (by serial bus register)
ex. SA10h, D7-D5 = 010 or 011
(b) Using trap filter for $2f_{SC}$.
(c) Using external ADC (refer to **3.5 External Y-ADC Connection Method**).

3. Trail noise

The trail noise like the afterimage sometimes occurs when the operation mode (NRMD = 00 to 01) and the sensitivity of horizontal sync nonstandard signal detection (VTRR register) are changed at the same time.
In this case set to forced horizontal sync nonstandard (SA01h, D5-D4: NSDS = 11) or forced inter-line processing (SA01h, D3-D2: MSS = 10) or NR off (SA06h = 00h) in the period in the 2 fields before to 8 fields behind in the moment to change.

★ **4. Memory power-down mode**

When using the memory power-down mode (SYSPDS = 1), the memory control lines ($\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WE}$) enter a floating state and must be pulled up to DVDD (3.3 V) to avoid unstable memory operation.

★ **5. Internal synchronous separator**

The internal synchronous separator performance may drop slightly if non-standard signals are input or at startup. If using only this function (EXCSS = 0), evaluate the performance carefully.

★ **6. Internal killer detector**

The internal killer detector performance may drop for weak signals. If using this function, evaluate the performance carefully.

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1. PIN FUNCTIONS

Table 1-1. Pin Functions (1/3)

	No.	Symbol	I/O	Level	Buffer type PU/PD [kΩ]	Description
	1	DGND	-	-		Digital section ground
★	2-9	MA7-MA0	O	TTL 3-state	1 mA	Address output for external EDO memory
★	10	$\overline{\text{MCAS}}$	O	TTL 3-state	1 mA	$\overline{\text{CAS}}$ output for external EDO memory (active-low)
★	11	$\overline{\text{MWE}}$	O	TTL 3-state	1 mA	$\overline{\text{WE}}$ output for external EDO memory (active-low)
★	12	$\overline{\text{MOE}}$	O	TTL 3-state	1 mA	$\overline{\text{OE}}$ output for external EDO memory (active-low)
	13-28	MIO15-MIO0	I/O	TTL 3-state	1 mA 5 V resistant	Data input/output for external EDO memory
	29	DGND	-	-		f_{SC} generator digital section ground
	30	XI	I	-		f_{SC} generator reference clock input (X'tal is connected.)
	31	XO	O	-		f_{SC} generator reference clock inverted output (X'tal is connected.)
	32	DVDD	-	-		f_{SC} generator digital section supply voltage
	33-36	HO3-HO0	O	TTL 3-state	1 mA	Data output for external field memory (Open when not used.) HO3 is the MSB, HO0 is the LSB.
	37	HWCK	O	TTL 3-state	3 mA	Write clock output for external field memory (Open when not used.)
	38	HRCK	O	TTL 3-state	3 mA	Read clock output for external field memory (Open when not used.)
	39	HRST	O	TTL 3-state	1 mA	Reset signal output for external field memory (Open when not used.)
	40	DGND	-	-		Digital section ground
	41-44	HI3-HI0	I	TTL	5 V resistant	Input for external field memory (Grounded when not used.) HI3 is the MSB, HI0 is the LSB.
	45	DVDD	-	-		Digital section supply voltage
	46	AVDD	-	-		f_{SC} generator DAC section supply voltage
	47	FSCO	-	Analog		f_{SC} generator f_{SC} output
	48	AGND	-	-		f_{SC} generator DAC section ground
	49	AGND	-	-		$8f_{SC}$-PLL ground
	50	FSCI	-	Analog		$8f_{SC}$-PLL f_{SC} input
	51	CPLL	-	-		$8f_{SC}$-PLL filter output (Grounded)
	52	RPLL	-	Schmitt	PU:50	Test pin (Grounded)
	53	AVDD	-	-		$8f_{SC}$-PLL section supply voltage

Table 1-1. Pin Functions (2/3)

No.	Symbol	I/O	Level	Buffer type PU/PD [kΩ]	Description
54	CKMD	I	TTL	5 V resistant PD:50	Clock mode test input ('L' : Normal mode, 'H' : Test mode) (Grounded)
55	DGND	-	-		Digital section ground
56	CLK8	O / I	TTL 3-state	3 mA 5 V resistant	8f_{SC} clock output (8f_{SC} clock input when CKMD pin = H)
57	$\overline{RSTB}$	I	Schmitt	5 V resistant PU:50	System reset input (active-low) (Active-low reset pulse is input from the outside.)
58	SLA0	I	TTL	5 V resistant PD:50	I^2C bus slave address selection input ('L' : B8 / B9h, 'H' : BA / BBh)
59	SCL	I	Schmitt	5 V resistant	I^2C bus clock input (Connected to system SCL line)
60	SDA	I / O	Schmitt N-ch open drain	5 mA 5 V resistant	I^2C bus data input/output (Connected to system SDA line)
61	ST0	O	TTL	1 mA	Internal signal monitor output 0
62	ST1	O	TTL	1 mA	Internal signal monitor output 1
63	NSTD	O	TTL	1 mA	Nonstandard signal detection monitor output ('L' : standard, 'H' : nonstandard)
64	DVDD	-	-		Digital section supply voltage
65-74	DYCO0-DYCO9 (LSB)-(MSB)	I/O	TTL	1 mA 5 V resistant	EXADINS=0: Digital YC signal alternate output EXADINS=1: Digital video data input for external Y-ADC (Pull down unuse lower bit pins via 100 Ω resistor) DYCO0 is the LSB, DYCO9 is the MSB.
75	ALTF	O	TTL	1 mA	EXADINS=0: Digital YC signal alternate flag output ('L' : C, 'H' : Y) EXADINS=1: 4f_{SC} clock output for external Y-ADC
76	$\overline{CSI}$	I	Schmitt	5 V resistant PD:50	Composite sync input (active-low)
77	TEST	I	TTL	5 V resistant PD:50	Test pin for IC selection ('L' : Normal mode, 'H' : Test mode) (Grounded)
78	LINE	I	TTL	5 V resistant PD:50	Forced inter-line processing selection input ('L' : ordinary processing, 'H' : forced inter-line processing)
79	KIL	I	TTL	5 V resistant PD:50	External killer input ('L' : ordinary processing, 'H' : forced YC separation stop)
80	DGND	-	-		Digital section ground
81	AVDD	-	-		Y-DAC and C-DAC supply voltage
82	CBPC	O	Analog		C-DAC phase compensation output
83	ACO	O	Analog		C-DAC analog C signal output
84	AYO	O	Analog		Y-DAC analog Y signal output
85	CBPY	O	Analog		Y-DAC phase compensation output
86	AGND	-	-		Y-DAC and C-DAC ground
87	AGND	-	-		Y-ADC ground

Table 1-1. Pin Functions (3/3)

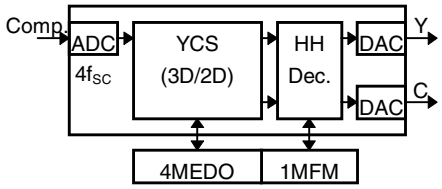
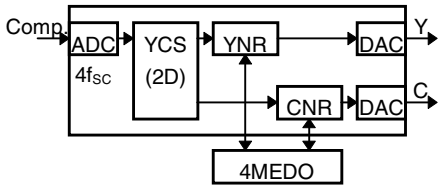
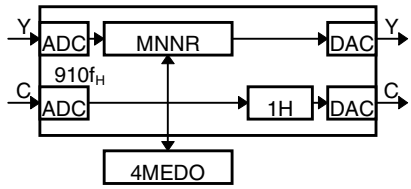
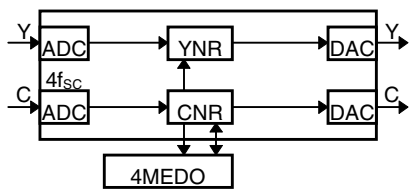
	No.	Symbol	I/O	Level	Buffer type PU/PD [kΩ]	Description
	88	AYI	I	Analog		Y-ADC analog composite signal or Y signal input
	89	VCLY	O	Analog		Y-ADC clamp potential output
	90	VRBY	O	Analog		Y-ADC bottom reference voltage output
	91	VRTY	O	Analog		Y-ADC top reference voltage output
	92	AVDD	-	-		Y-ADC supply voltage
	93	AVDD	-	-		C-ADC supply voltage
	94	VRTC	O	Analog		C-ADC top reference voltage output
	95	VRBC	O	Analog		C-ADC bottom reference voltage output
	96	ACI	I	Analog		C-ADC analog C signal input
	97	AGND	-	-		C-ADC ground
★	98	$\overline{\text{MRAS}}$	O	TTL 3-state	1 mA	$\overline{\text{RAS}}$ output for external EDO memory (active-low)
★	99	MA8	O	TTL 3-state	1 mA	Address output for external EDO memory
	100	DVDD	-	-		Digital section supply voltage

2. SYSTEM OVERVIEW

2.1 Operation Modes

The μPD64082 can operate in the following major three signal processing modes. Mode selection is performed according to NRMD on the serial bus.

Table 2-1. Operation Modes

Serial bus setting Mode name	Function [Note 1]	Pin input	System clock [Note 2]	Feature Model diagram
NRMD = 00 YCS mode	Y/C separation and HH decoding (Japan only)	AYI : Composite signal ACI : None (invalid)	Burst locked clock ($4f_{SC}$, $8f_{SC}$)	• For standard signals, motion-adaptive three-dimensional Y/C separation is performed. • For nonstandard signals, inter-line Y/C separation is performed. • Adding field memory enables supporting HH decoding stipulated in the wide clear vision specification. [Note 3] 
NRMD = 01 YCS+ mode	2D Y/C separation and YCNR	AYI : Composite signal ACI : None (invalid)	Burst locked clock ($4f_{SC}$, $8f_{SC}$)	• Inter-line Y/C separation and Frame recursive YNR and CNR is performed. 
NRMD = 10 MNNR mode	Frame comb type YNR 1H-delayed C signal	AYI : Y signal ACI : C signal	Line locked clock ($910f_H$, $1820f_H$)	• Motion-adaptive frame-average type YNR is performed. It can reduce inter-frame noise from the MN signal. • In addition to a Y signal delay, the C signal is delayed by 1H. [Note 4] 
NRMD = 11 YCNR mode	Frame recursive type YNR Frame recursive type CNR	AYI : Y signal ACI: C signal	Burst locked clock ($4f_{SC}$, $8f_{SC}$)	• Frame recursive YNR and CNR are performed. They can reduce random noise from VCR playback signals. [Note 5] 

Notes 1. 3D Y/C separation, Frame-recursive YNR/CNR, Frame-comb YNR, each function is independence. So these don't operate at the same time.

2. $4f_{SC}$ ($910f_H$) is used for signal processing, and $8f_{SC}$ ($1820f_H$) is used for the memory interface and digital YC output sections.

3. HH decoding is impossible for Y/C separate inputs. It is impossible also for VCR playback signals and nonstandard signals.

4. C signal delay processing cannot be performed for horizontal sync signals with jitter, such as VCR playback signals. In some MN signals, the horizontal sync signal phase may fluctuate during the vertical sync period. In these signals, the phase of an internally delayed C signal may be disturbed because the line locked clock fluctuates immediately after the end of the vertical sync period.

5. With the precision of the VCR playback signal, the vertical nonstandard detection circuit sometimes malfunctions, and the NR operation stops.

In this case, when using FORCED STANDARD SETTING (NSDS = 01), the NR operation becomes possible.

2.2 Filter Processing

Table 2-2 lists filters used in each mode.

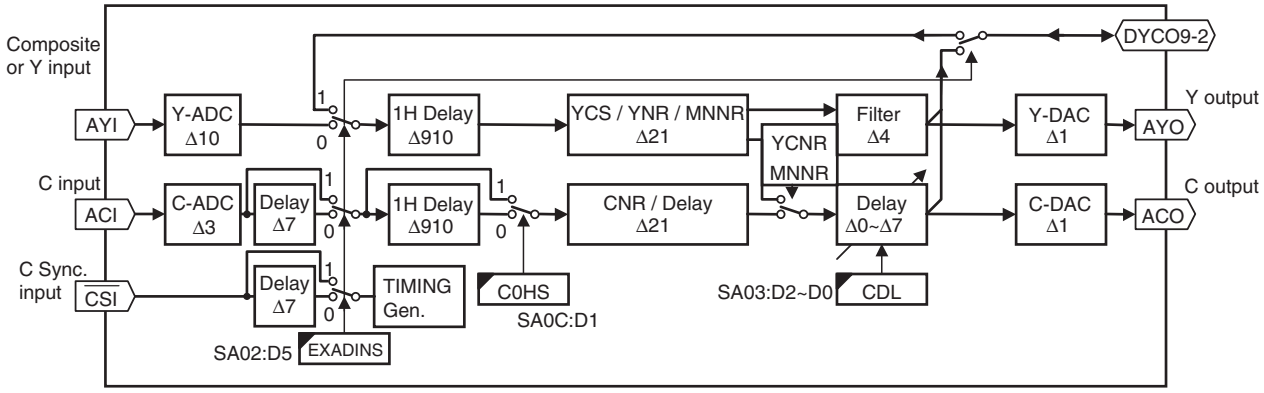
Table 2-2. Filter Matrix

Mode	Standard / nonstandard / killer signal detection	Filter selected			
		Effective-picture period		Blanking period	
		Still picture portion	Moving picture portion	Horizontal (11 μs)	Vertical (1H to 22H)
YCS mode (NRMD = 00)	Standard signal detected	Frame comb	Line comb		Band-pass
	Nonstandard signal detected	Line comb			Band-pass
	Killer signal detected	Through (Y/C separation stop)			
YCS+ mode (NRMD = 01)	Standard or horizontal nonstandard signal detected	Line comb + Frame recursive	Line comb		Band-pass
	Vertical nonstandard signal detected	Line comb			Band-pass
	Killer signal detected	Through			
MNNR mode (NRMD = 10)	Standard signal detected	Frame comb	Through		
	Nonstandard signal detected	Through			
YCNR mode (NRMD = 11)	Standard or horizontal nonstandard signal detected	Frame recursive	Through		
	Vertical nonstandard signal detected	Through			
	Killer signal detected	Through			
Vertical contour compensation / Y peaking		Active			Through

2.3 System Delay

The following diagram shows a model of system delays (video signal delays).

Figure 2-1. System Delay Model

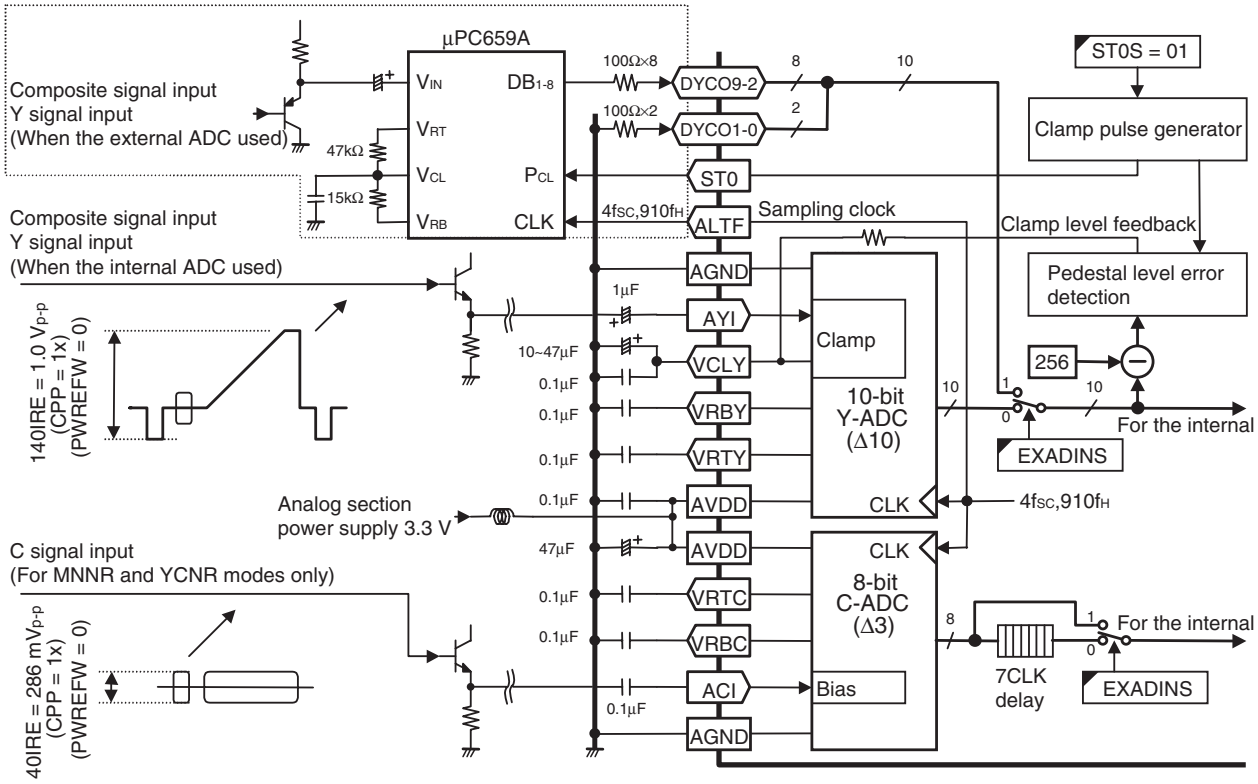


Remark Δ1 corresponds to a one-clock pulse delay ($4f_{SC}$ or $910\ f_H$ = about 69.8 ns)

3. VIDEO SIGNAL INPUT BLOCK

This block converts analog video signals to digital form.

★ **Figure 3-1. Video Signal Input Block Diagram**



3.1 Video Signal Inputs

Video signals are input to the AYI, ACI and DYCO9 to DYCO2 pins according to the operation mode selected from the serial bus.

- YCS mode : The composite signal is input to the AYI pin. (EXADINS = 0)
  8-bit composite signals in digital form are input to the DYCO9 to DYCO2 pins.
  (EXADINS = 1)
  An input to the ACI pin is disabled.
- MNNR/YCNR mode : The Y signal is input to the AYI pin. (EXADINS = 0)
  8-bit Y signals in digital form are input to the DYCO9 to DYCO2 pins. (EXADINS = 1)
  The C signal is input to the ACI pin.

3.2 Pedestal Level Reproduction

This circuit reproduces the pedestal level of a video signal. The pedestal level error detection circuit detects the difference between that level and the internal fixed value of 256 LSB levels, and outputs the feedback level.

This output signal is connected to VCLY pin via internal resistor to feed back to video signal for fixing pedestal level to 256 LSB.

Note Do not use this circuit when the external ADC is used.

3.3 Video Signal Input Level

It is necessary to limit the level of video signal inputs to within a certain range to cope with the maximum amplitude of the video signal and variations in it. Figure 3-2 shows the waveform of the video signal input whose amplitude is 140 IRE_{p-p} = 840 LSB_{p-p} (0.8 times a maximum input range of 1024 LSB). In this case, it is possible to input a white level of up to 131 IRE for the Y signal and up to 175 IRE_{p-p} for the C signal.

★ **Figure 3-2. Video Signal Input Waveform Example (for 75% Color Bar Input)**

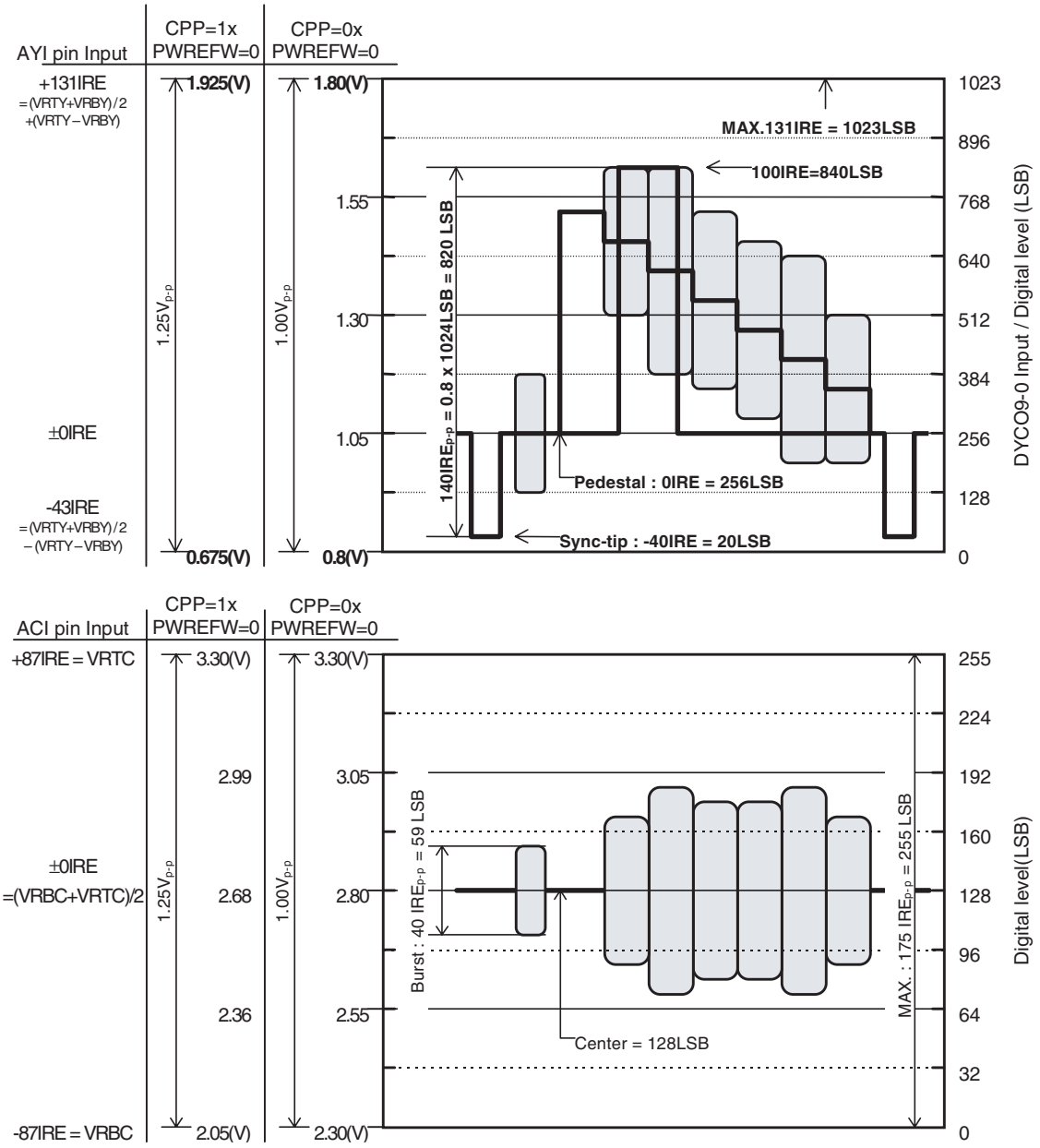


Table 3-1 shows the recommended input level of video signals.

★ **Table 3-1. Recommended Input Level of Video Signals**

Mode Name	Serial bus setting	The maximum input range of ACI pin	Recommended input level of video signals for ACI pin.
1 V_{p-p} Mode	CPP = 0x, PWREFW = 0	1.00 V_{p-p} (Typ.)	140 IRE $_{p-p}$ = 0.8 V_{p-p} (1.00 V × 0.8)
1.25 V_{p-p} Mode	CPP = 1x, PWREFW = 0	1.25 V_{p-p} (Typ.)	140 IRE_{p-p} = 1.0 V_{p-p} (1.25 V × 0.8)

3.4 Pin Treatment

- Supply 3.3 V to the AVDD pins. Isolate them sufficiently from the digital section power supply.
- Use as wide wiring patterns as possible for the ground lines of each bypass capacitor and the AGND pins so as to minimize their impedance.
- Connect a video signal to the AYI and ACI pins by capacitive coupling. Maintain a low input impedance for video signals. Be sure to keep the wiring between the capacitor and the AYC and ACI pins as short as possible.
- Pull down the VRTY, VRBY, VRTC and VRBC reference voltage pins via a 0.1 μF bypass capacitor.
- Pull down the VCLY pin via a 0.1 μF bypass capacitor and a 10 to 47 μF electrolysis capacitor.
- Do not bring the digital system wiring (especially the memory system) close to this block and the straight downward of the IC.
- Keep the ACI pin open if no chroma input is used.

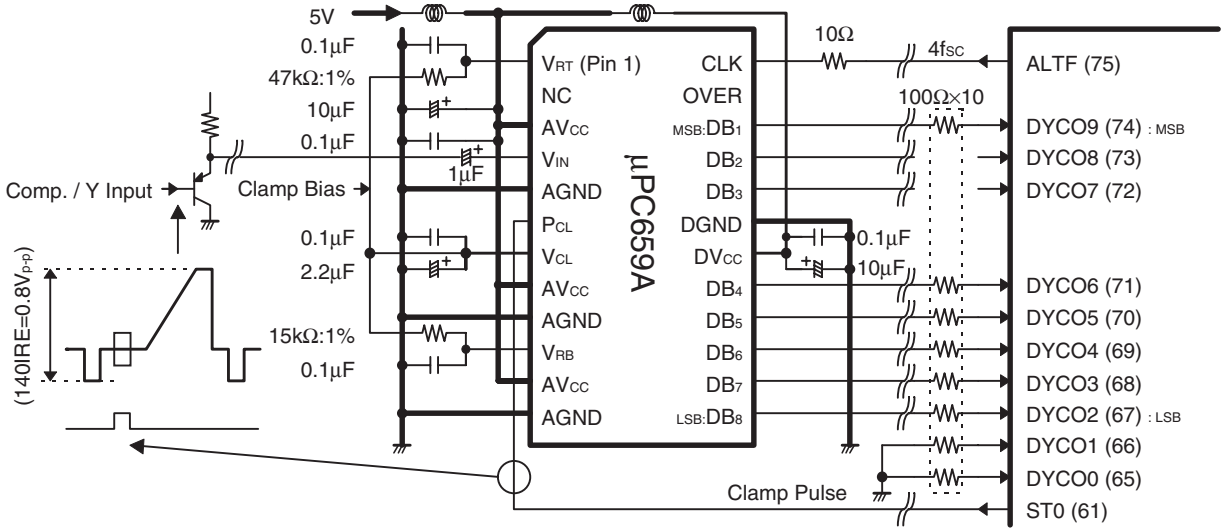
3.5 External Y-ADC Connection Method

Setting up EXADINS = 1 on the serial bus puts the IC in the external Y-ADC mode. In this mode, the ALTF pin is used to output 4f_{SC} sampling clock pulses, and the DYCO9 to DYCO0 pins are used to receive digital data inputs. Setting up ST0S = 01 on the serial bus causes a clamp pulse to be output from the ST0 pin. It is used as a pedestal clamp pulse for external ADC. The clamp potential for the pedestal level of external Y-ADC must be determined so that the sampled value becomes about 256 ±8LSB. Supply converted 10-bit data to the DYCO9 to DYCO0 pins via a 100 Ω resistor. For using 8-bit ADC (exp. μPC659A), Pull down the DYCO1 and DYCO0 pins via 100 Ω resistor.

In this mode, for Y-ADC in the μPD64082, keep the VRTY and VRBY pins open, and pull down the VCLY and AYI pins via a 0.1 μF capacitor.

★ When using the S input via the external Y-ADC and internal C-ADC, if the Y and C delays differ, adjust the delay using the serial bus CDL.

Figure 3-3. Example of Application Circuit Set Up for External ADC

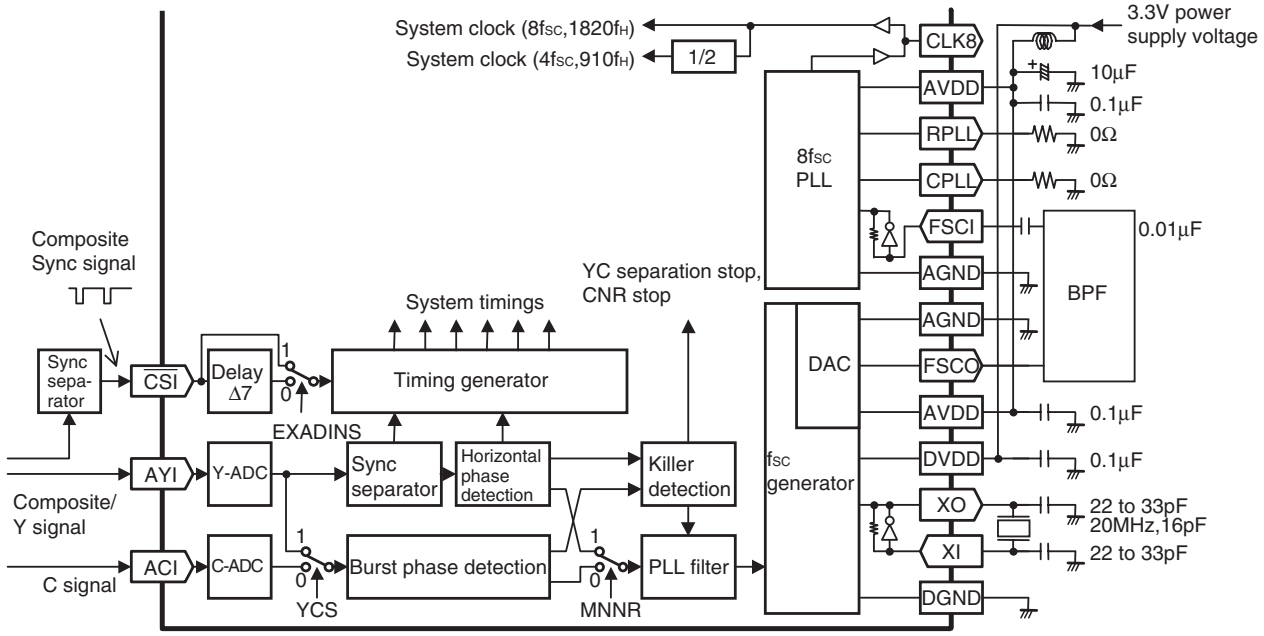


Serial bus setting: EXADINS = 1, ST0S = 01

4. CLOCK/TIMING GENERATION BLOCK

This block generates system clock pulses and timing signals from video signals.

★ **Figure 4-1. Clock/Timing Generation Block Diagram**



4.1 Sync Separator and Timing Generator

These sections separate horizontal and vertical sync signals from the composite or Y signal sampled at 4fSC or 910fH, and generate system timing signals by using them as references.

4.2 Composite Sync Signal Input

An active-low composite sync signal separated from the video signal is input at the $\overline{\text{CSI}}$ pin. This input is used as a reference signal to lock onto sync at the timing generator.

4.3 Horizontal/Burst Phase Detection Circuit

The horizontal phase detection circuit extracts the horizontal sync signal from the Y signal sampled at 4fSC or 910fH to detect a horizontal phase error. This phase error is used for generation of 227.5fH and timing generator. The burst phase detection circuit extracts the burst signal from the composite signal or C signal sampled at 4fSC to detect a burst phase error. This phase error is used for fSC generation.

4.4 PLL Filter Circuit

The PLL filter circuit integrates a burst or horizontal phase error to determine the oscillation frequency of the fSC generator ahead.

4.5 Killer Detection Circuit

The killer detection circuit compares the amplitude of the burst signal with the KILR value set on the serial bus to judge on a color killer. If the burst amplitude becomes smaller than or equal to the set KILR value when the burst locked clock is operating, the fSC generator is allowed to free-run.

4.6 fsc Generator

The fsc generator generates fsc (or 227.5fH when the line locked clock is running) from an oscillation frequency determined in the PLL filter. fsc is converted by internal DAC to an analog sine waveform before it is output from the FSCO pin. Because this output contains harmonic components, they must be removed using an external band-pass filter (BPF) connected via a buffer, before the analog sine waveform is input to the FSCI pin via a capacitor. The fsc generator uses a 20 MHz free-run clock pulse as a reference.

4.7 8fsc-PLL Circuit

The 8fsc-PLL circuit generates 8fsc (or 1820fH) from fsc (or 227.5fH) input at the FSCI pin. The 8fsc signal is output from the CLK8 pin. It is also used as the internal system clock.

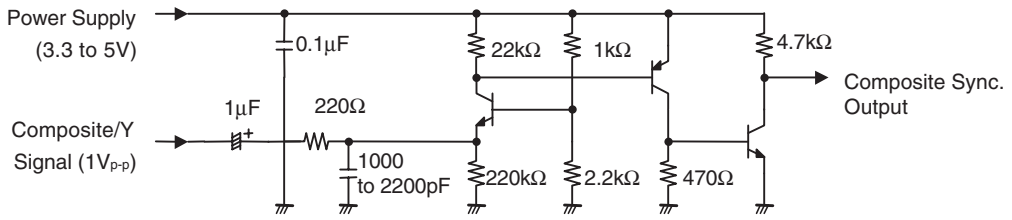
4.8 Pin Treatment

- Supply 3.3 V to the AVDD pins. Isolate them sufficiently from the digital section power supply.
- Use as wide wiring patterns as possible for the ground lines of each bypass capacitor and the DGND and AGND pins so as to minimize their impedance.
- Connect a 20-MHz Crystal resonator across the XI and XO pins. Provide guard areas using ground patterns to keep these pins from interfering with other blocks. Table 4-1 shows the crystal resonator specification example.
- Connect a BPF to the FSCO pin via an emitter follower. Supply the fsc signal to the FSCI pin via a capacitor.
- Pull down the RPLL and CPLL pins via a 0 Ω resistor.
- Input an active-low composite sync signal to the $\overline{\text{CSI}}$ pin. Figure 4-2 shows the external composite sync separator application circuit example.

Table 4-1. Crystal Resonator Specification Example

Parameter	Specification
Frequency	20.000000 MHz
Load Capacitance	16 pF
Equivalent Serial Resistance	40 Ω or less
Frequency Permitted Tolerance	50 ppm or less
Frequency Temperature Tolerance	50 ppm or less

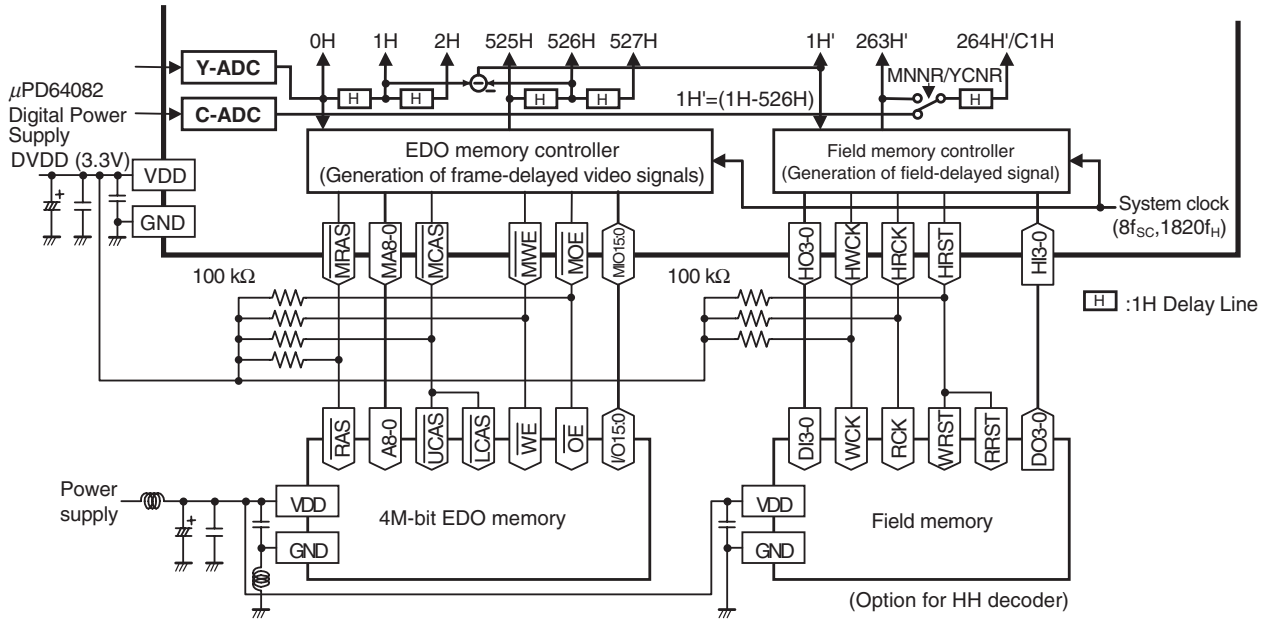
Figure 4-2. External Composite Sync Separator Application Circuit Example



5. MEMORY INTERFACE BLOCK

This block controls external memory to generate frame-/field-delayed video signals. Because the memory interface input pins are designed to 5 V resistant, they can be connected directly to 5-V type memory.

★ **Figure 5-1. Memory Interface Block Diagram**



5.1 EDO Memory Controller

The EDO memory controller accesses external 4-Mbit EDO memory at high speed to generate frame-delayed (525H) signals. It also refreshes memory. See **16. ELECTRICAL CHARACTERISTICS 4-Mbit EDO Memory Requirements** for the requirements of the EDO memory.

5.2 Field Memory Controller

The field memory controller accesses external field memory at high speed to generate field-delayed (262H') signals. See **16. ELECTRICAL CHARACTERISTICS Field Memory Requirements** for the requirements of the field memory. No field memory is required when the HH decoder is not used.

5.3 Pin Treatment

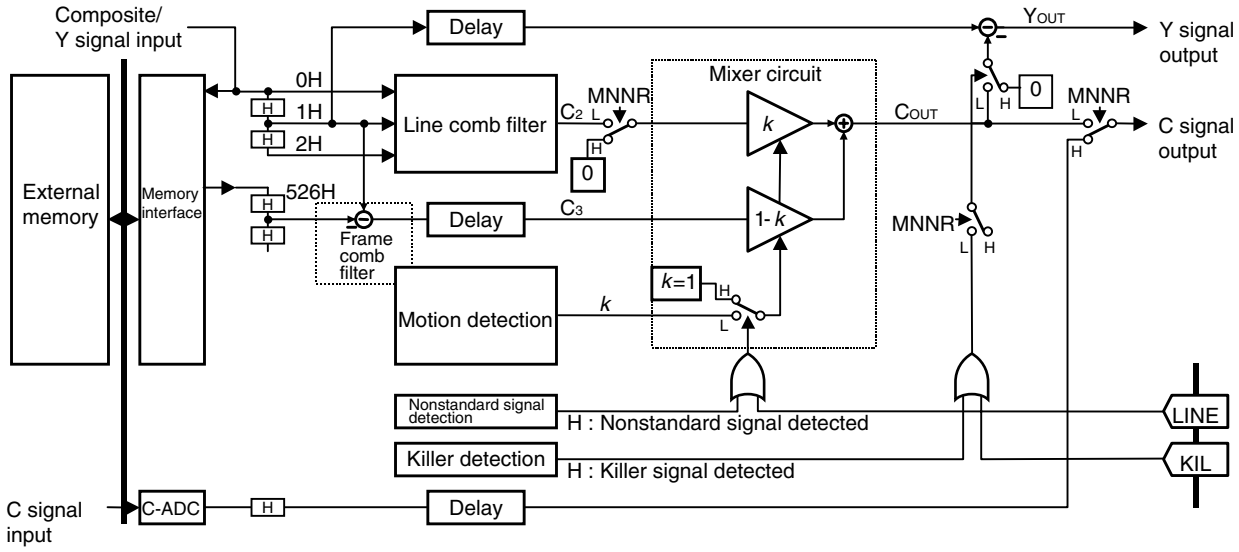
The memory block is likely to be a source of noise. It is necessary to pay due attention when designing a circuit and circuit pattern to contain the memory block. If noise from the memory block or a power supply enters the video signal circuit, some noises for example vertical stripe may appear on the video picture.

- Isolate the power supply for the memory block sufficiently from power supplies for other blocks, and keep the impedance of connections between the memory block and its power supply as low as possible.
- Keep the memory and interface lines, especially $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, HWCK, and HRCK lines, away sufficiently from analog blocks, and protect them using partitions consisting of ground patterns. Do not lay these interface lines directly under the μPD64081B. Also keep the wiring length as short as possible.
- Do not put the memory at the reverse side of the μPD64082.
- Pull down the HI3 to HI0 pins to the ground level if the field memory is not used.
- ★ When using the memory power-down mode (SA16h, D7: SYSPDS = 1), pull-up the memory control pins ($\overline{MRAS}$, $\overline{MCAS}$, $\overline{MOE}$, $\overline{MWE}$, HWCK, HRCK, and HRST) to DVDD of the μPD64082 (3.3 V).

6. COMB FILTER BLOCK

This block performs Y/C separation or frame comb type YNR according to the result of checks in various detection circuits. This block is used in the YCS or MNNR mode.

Figure 6-1. Comb Filter Block Diagram



6.1 Line Comb Filter

The C signal is separated from video signals that have been delayed by 0H, 1H, and 2H. This filter serves as a logical comb filter based on inter-line correlation to reduce dot and cross-color interference. The filter output (C_2) is used in the moving picture portion of standard signals, nonstandard signals, and blanking periods. In the MNNR mode, this filter output is not used. It is always kept at a "0" level.

6.2 Frame Comb Filter

The C signal (or, in the MNNR mode, a noise component) is separated from video signals that have been delayed by 1H and 526H. The filter output (C_3) is used in still picture portions by the motion detection circuit.

6.3 Mixer Circuit

The mixer circuit mixes C signals to adapt to the motion according to the motion factor from the motion detection circuit. In other words, C_{OUT} is generated by mixing the line comb filter output (C_2) and the frame comb filter output (C_3) by a mixture ratio according to the motion factor k (0 to 1). If the input signal is a nonstandard signal, or if the LINE pin is at a high level, C_2 is output without performing motion-adaptive mixture.

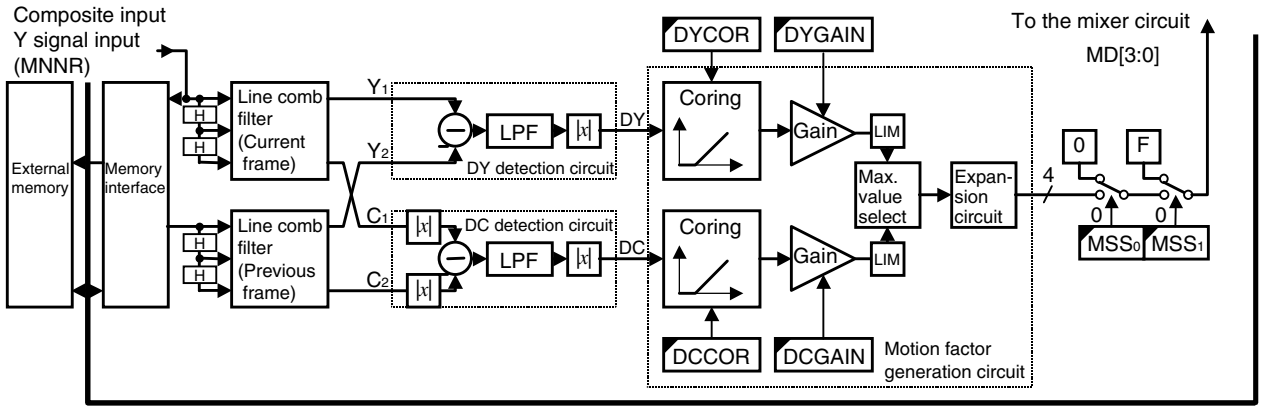
6.4 C Signal Subtraction

The Y_{OUT} signal is separated by subtracting the C_{OUT} signal (or, in the MNNR mode, a noise component) from a composite video signal that has been delayed by 1H. Subtraction is quitted when the killer detection circuit detects that the input signal is a color killer signal (monochrome signal or non-burst signal) or that the KIL pin is at an H' level.

7. MOTION DETECTION BLOCK

This block generates a 4-bit motion factor indicating an inter-frame motion level from the video signal inter-frame difference. This motion factor is used as a mixture ratio to indicate how the frame and line comb filter outputs are mixed. This block is used in the YCS or MNNR mode.

Figure 7-1. Motion Detection Block Diagram



7.1 Line Comb Filter

Before obtaining an inter-frame difference, the line comb filter performs YC separation for the composite signals of both frames.

7.2 DY Detection Circuit

The DY detection circuit detects a Y signal inter-frame difference. After a Y signal difference between the current and previous frames is obtained, its absolute value, obtained by limiting the frequency band for the Y signal difference using an LPF, is output as a Y frame difference signal, or a DY signal.

7.3 DC Detection Circuit

The DC detection circuit detects a C signal inter-frame difference. After a C signal difference between the current and previous frames is obtained, its absolute value, obtained by limiting the frequency band for the C signal difference using an LPF, is output as a C frame difference signal, or a DC signal. Because the phase of the C signal is inverted between frames, the absolute values of the C signals of both frames have been obtained before the difference is obtained.

7.4 Motion Factor Generation Circuit

The motion factor generation circuit generates a 4-bit motion factor from the DY and DC signals. The first coring circuit performs coring according to the DYCOR and DCCOR settings on the serial bus to block weak signals like noise. The gain adjustment circuits ahead perform gain adjustment according to the DYGAIN and DCGAIN settings on the serial bus to specify the sensitivity of the motion factor. These outputs are limited to a 4-bit width, and one having a higher level is selected for output by the maximum value selection circuit. The selected signal is expanded horizontally, then output as a final motion factor.

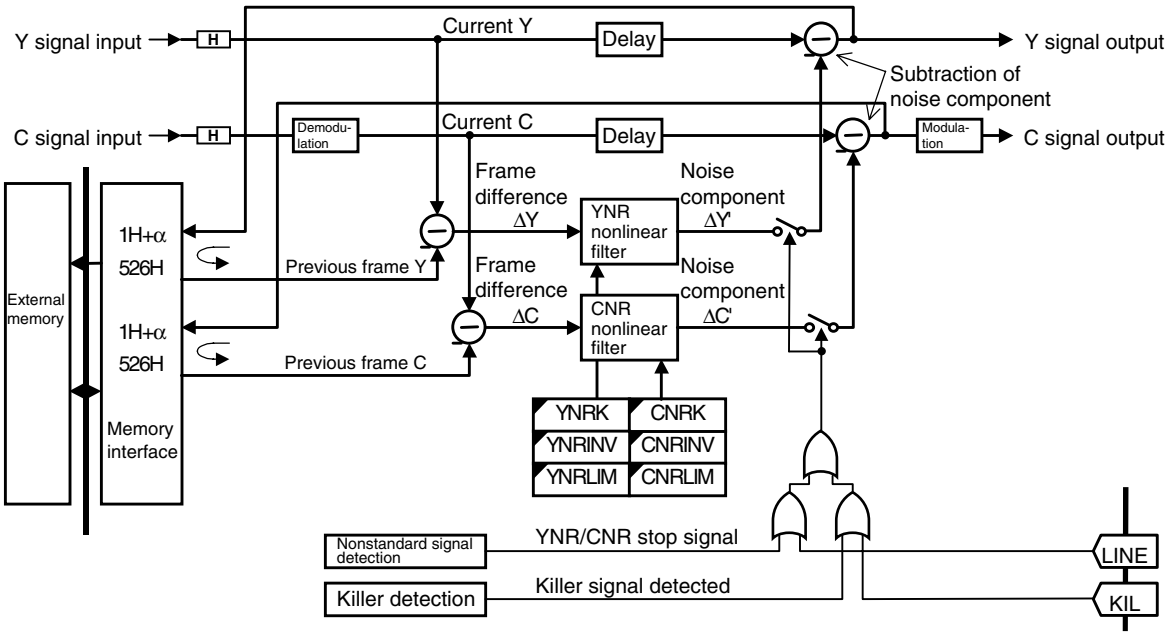
7.5 Forcible Control for The Motion Factor

The motion factor can be set to 0 (forced stop) or a maximum value (forced motion) using the MSS signal on the serial bus.

8. YNR/CNR BLOCK

This block performs frame recursive YNR and CNR. It is used in the YCNR mode. It cannot be used in the YCS or MNNR mode.

Figure 8-1. YNR/CNR Block Diagram



8.1 YNR/CNR Processing

The frame difference (ΔY) signal is generated by subtracting the previous frame Y signal from the current frame Y signal. The noise component ΔY' signal is extracted by eliminating the motion component of the ΔY signal at the nonlinear filter. Noise components are reduced by subtracting the noise component ΔY' signal from the current frame Y signal. At the same time, the Y signal submitted to noise reduction is delayed by a frame to be used to generate ΔY for the next frame. This way the frame recursive YNR is configured. Much the same processing is performed for the C signal to reduce noise components.

8.2 Nonlinear Filter

The ΔY' and ΔC' noise components are extracted from ΔY and ΔC. ΔY and ΔC contain inter-frame motion components and noise components. Subtracting ΔY and ΔC from the current frame Y and C signals causes inter-frame motion components to remain in the output picture. To solve this problem, a nonlinear filter that passes only low-amplitude signals is used; generally, motion components have a large amplitude, while noise components have a small amplitude. How nonlinear the filter is to be is specified using YNRK, YNRLIM, YNRINV, CNRK, CNRLIM, and CNRINV on the serial bus.

8.3 YNR/CNR Operation Stop

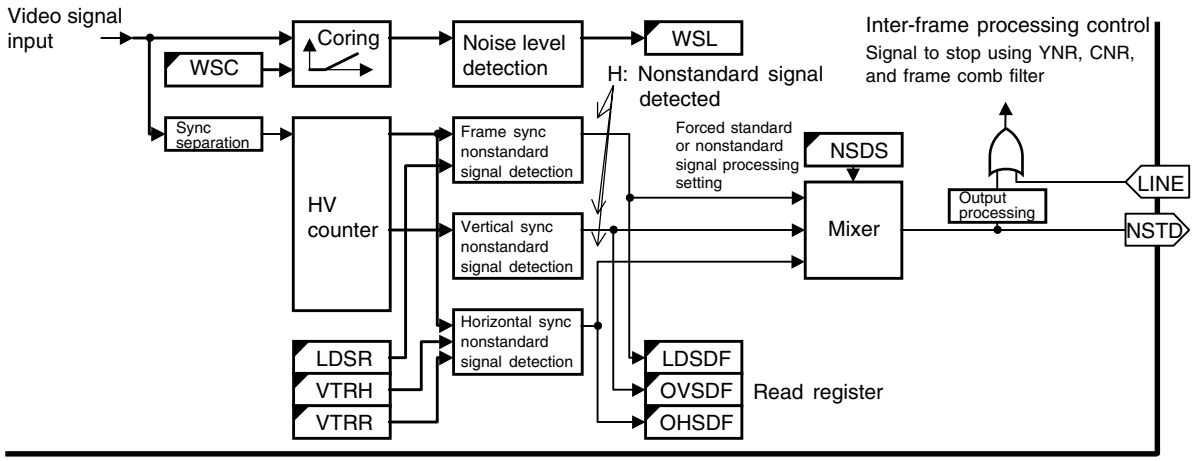
If the nonstandard signal detection circuit detects a vertical nonstandard signal or frame sync nonstandard signal, or the LINE pin is at a high level, the killer detection circuit detects a color killer signal, or the KIL pin is at a high level, YNR and CNR operations are stopped.

9. NONSTANDARD SIGNAL DETECTION BLOCK

This block detects nonstandard signals not conforming to the NTSC standard, such as VCR playback signals, home TV game signals, and Laser-Disc special playback signals. The detection result is used to stop inter-frame video processing.

(and selects intra-field video processing forcibly.)

Figure 9-1. Nonstandard Signal Detection Block Diagram



9.1 Horizontal Sync Nonstandard Signal Detection

The horizontal sync nonstandard signal detection circuit detects signals not having a standard relationship between f_{SC} and f_H ($f_{SC} = 227.5f_H$) like a VCR playback signal. The sensitivity of detection is set using VTRR and VTRH on the serial bus. If the circuit detects a nonstandard signal, it stops using the frame comb filter. The detection result can be read using OHSDF on the serial bus.

9.2 Vertical Sync Nonstandard Signal Detection

The vertical sync nonstandard signal detection circuit detects signals not having a standard relationship between f_H and f_V ($f_H = 262.5f_V$) like a VCR special playback signal and home TV game signal. The sensitivity of detection cannot be set. If the circuit detects a nonstandard signal, it stops using the frame comb filter, YNR, and CNR. The detection result can be read using OVSDF on the serial bus.

9.3 Frame Sync Nonstandard Signal Detection

The frame sync nonstandard signal detection circuit detects signals out of horizontal sync phase between frames, such as a laser-disc special playback signal. The sensitivity of detection is set using LDSR on the serial bus. If the circuit detects a nonstandard signal, it stops using the frame comb filter, YNR, and CNR. The detection result can be read using LDSDF on the serial bus.

9.4 Forced Standard or Nonstandard Signal Control

It is possible to specify either forced standard or nonstandard signal control using NSDS on the serial bus.

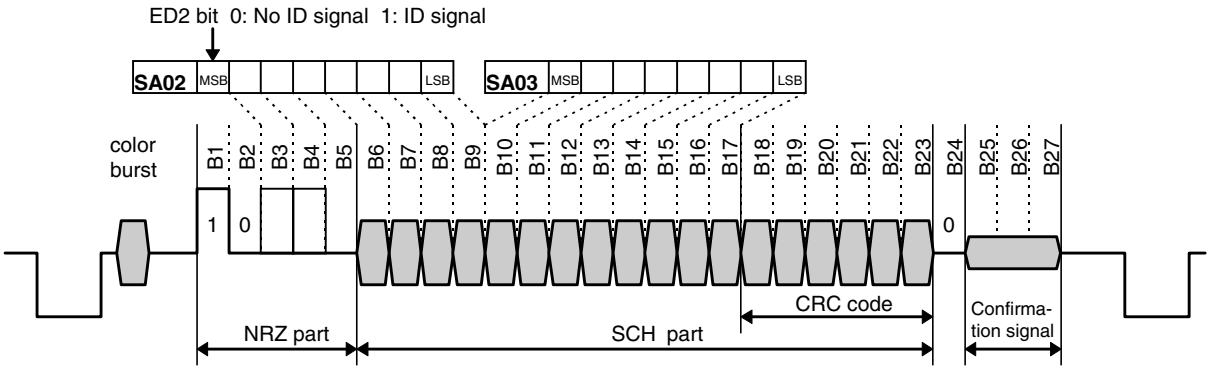
9.5 Noise Level Detection

The noise level detection circuit detects a noise level in the flat portion of a video signal. The sensitivity of detection is set using WSCOR on the serial bus. The detection result can be read using WSL on the serial bus; it is not used in the IC. The detection result can be processed in a microprocessor to find a weak electric field.

10. WCV-ID DECODER BLOCK

This block decodes an identification control signal superimposed on a wide clear vision signal of 22H and 285H.
(Remark: The wide clear vision standard applies only in Japan.)

Figure 10-1. Wide Clear Vision ID Signal Configuration



10.1 WCV-ID Decoder

The WCV-ID decoder checks whether the video signal contains an ID signal by examining mainly the following seven items. If all these items turn out to be normal, an ID signal is detected. The check and decode results are output to the ED2 bit and bits B3 to B17 on the serial bus, respectively. In addition, the phase of the confirmation signal is detected.

<1> A difference in DC level between B1 and B2 is not smaller than a certain value.
<2> The DC level of the SCH part is not higher than a certain value.
<3> The f_{SC} amplitude of the NRZ part is not larger than a certain value.
<4> The f_{SC} amplitude of the SCH part is not smaller than a certain value (if FSCOFF = 0),
<5> Items <1> to <4> continue for at least 12 fields.
<6> The parity of the NRZ part (B3 to B5) is normal [Note].
<7> The CRC of the NRZ part and SCH part (B3 to B23) is normal [Note].

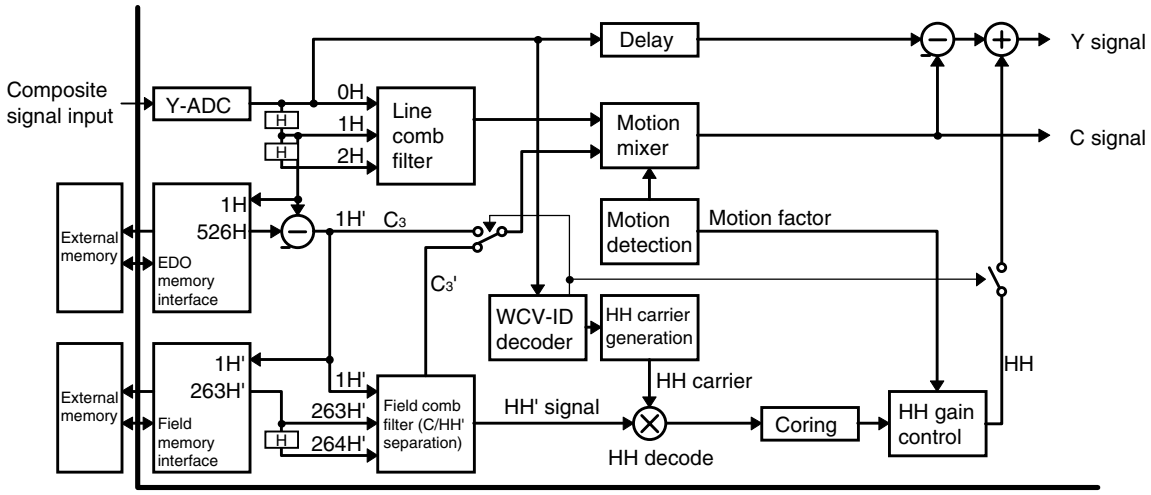
Note If an error is detected in item <6> or <7>, bits B3 to B17 on the serial bus hold the decoded value for the previous field.

11. HH DECODER BLOCK

This block decodes the HH signal superimposed on the wide clear vision signal main picture part. This block is used in the YCS mode. In the MNNR or YCNR mode, this block can not be used.

(Remark: The wide clear vision standard applies only in Japan.)

Figure 11-1. HH Decoder Block Diagram



11.1 C/HH' Separation

The field comb filter is configured using three-line (1H', 263H', and 264H') data, such as the frame comb filter output, its field-delayed output, and 1H-delayed data. It is used to separate the C and HH' signals. The C_3' signal separated this way is used as a C signal motion mixture during HH decoding operation. The line memory for field comb filter configuration is used to delay the C signal by 1H during the MNNR/YCNR mode.

11.2 HH Decoding

The HH carrier signal is generated in reference to the 4/7f_{SC} phase (B25 to B27) detected in the WCV-ID decoder. The HH signal is decoded by demodulating the carrier signal with the HH' signal. The coring circuit performs ±2LSB (in 8-bit terms) coring for the decoded HH component to prevent S/N deterioration.

11.3 HH Gain Control

In the motion signal part of a picture, cross-talk may occur between the C and HH' signals, resulting in interference components getting in the decoded HH signal. To solve this problem, A motion factor is used to limit the HH signal for the motion part. The motion factor-based limitation characteristic is set up using HHMG and HHTG on the serial bus. After being submitted to gain control, the HH signal is added to the Y signal main line.

11.4 Transition to HH Decoding

When the YCS Mode (NRMD = 00) is used, if all the following conditions are satisfied, transition occurs to HH decoding.

<1> The nonstandard signal detection circuit has not detected a nonstandard signal.

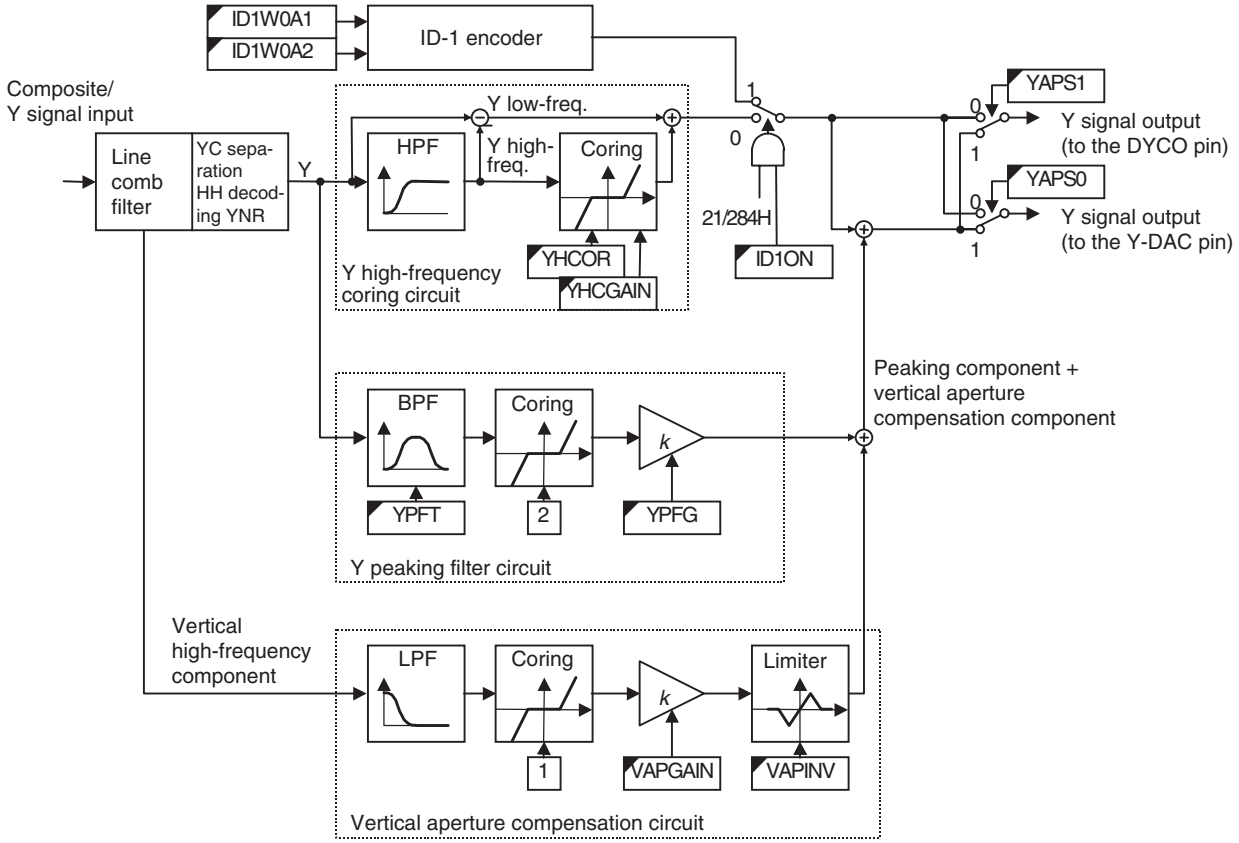
<2> The WCV-ID detection circuit has detected an ID signal, or forced decoding has been specified using HHDS on the serial bus.

<3> The HH' multiplex bit (B10) is 1 continuously for at least four fields.

12. Y SIGNAL OUTPUT PROCESSING BLOCK

After Y/C separation or Y Noise reduction, this block performs high-frequency coring, peaking, and vertical aperture compensation for the Y signal submitted to YNR processing.

Figure 12-1. Y Signal Output Processing Block Diagram



12.1 Y High-Frequency Coring Circuit

The Y high-frequency coring circuit performs coring for the high-frequency component of the Y main line signal. It works as a simplified noise reducer, because it can eliminate high-frequency components at 1 LSB to 3 LSB levels. The coring level is set using YHCOR on the serial bus.

<1> HPF circuit : Separates the input Y signal into the low- and high-frequency components.

<2> Coring circuit : Performs coring for Y high-frequency components according to the YHCOR setting, and outputs a Y signal by adding the Y high- and low-frequency components after they are submitted to coring. The coring effect can set 1/2 times by the YHCGAIN setting.

12.2 Y Peaking Filter Circuit

The Y peaking filter circuit performs peaking processing for the Y signal to correct the frequency response of the Y signal.

<1> BPF circuit : Extracts high-frequency components from the original Y signal according to the YPFT setting on the serial bus. The center frequency of the BPF can be selected from 3.58, 3.86, 4.08, and 4.22 MHz.

<2> Coring circuit : Performs ±2LSB (in 8-bit terms) coring for Y high-frequency components to prevent S/N deterioration during peaking processing.

<3> Gain adjustment circuit : Performs gain adjustment for peaking components according to the YPFG setting on the serial bus. The gain to be added can be changed in 16 steps over a range between −1.000 times and +0.875 times.

<4> Addition to the main line : Y peaking components, together with vertical aperture compensation components, are added to the Y signal.

12.3 Vertical Aperture Compensation Circuit

The vertical aperture compensation circuit extracts vertical contour components from a Y signal and adds them to the Y signal to emphasize contours.

<1> Line comb filter : Extracts vertical high-frequency components from the video signal.

<2> LPF circuit : Eliminates C signal components and Y signal slant components to extract vertical contour components.

<3> Coring circuit : Performs ±1LSB (in 8-bit terms) coring for vertical high-frequency components to prevent S/N deterioration during aperture compensation.

<4> Gain adjustment circuit : Performs gain adjustment for aperture compensation components according to the VAPGAIN setting on the serial bus.

<5> Limiter circuit (nonlinear processing) : Performs limit processing for aperture compensation components according to the VAPINV setting on the serial bus. Signals for which contours are to be emphasized are rather weak ones. Uniform emphasis would result in initially large signals becoming too large. To solve this problem, the limiter circuit blocks signals larger than the VAPINV setting, thereby disabling contour emphasis for large signals.

<6> Addition to the main line : Vertical aperture compensation components, together with Y peaking components, are added to the Y signal.

12.4 Turning On/Off Y Peaking and Vertical Aperture Compensation

The YAPS setting on the serial bus can be used to turn Y peaking and vertical aperture compensation on and off.

12.5 ID-1 Encoder

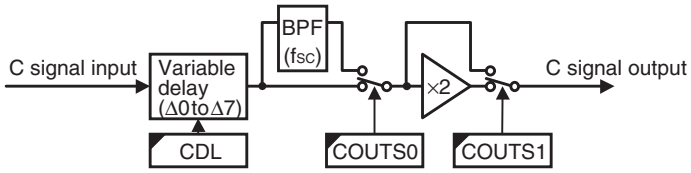
★ Bit information conforming to the ID-1 standard (CPX-1204) can be superimposed on the Y signal output at 20H/283H. ID1ON on the serial bus specifies whether to turn on or off superimposition. ID1W0A1 and ID1W0A2 specify the bit information to be superimposed.

If ID-1 information has already be superimposed on the original signal, it will be replaced with the newly specified ID-1 information.

13. C SIGNAL OUTPUT PROCESSING BLOCK

After Y/C separation, the C signal output processing block performs delay adjustment, BPF processing, and gain adjustment for the C signal submitted to CNR processing.

Figure 13-1. C Signal Output Processing Block Diagram



13.1 C Signal Delay Adjustment

The delay time of the C signal can be varied in a range between 0 and 7 clock pulses (4fSC) according to CDL on the serial bus. This way, the delay of the C signal relative to the Y signal can be set to anywhere between –4 clock pulses (–280 ns) and +3 clock pulses (+210 ns).

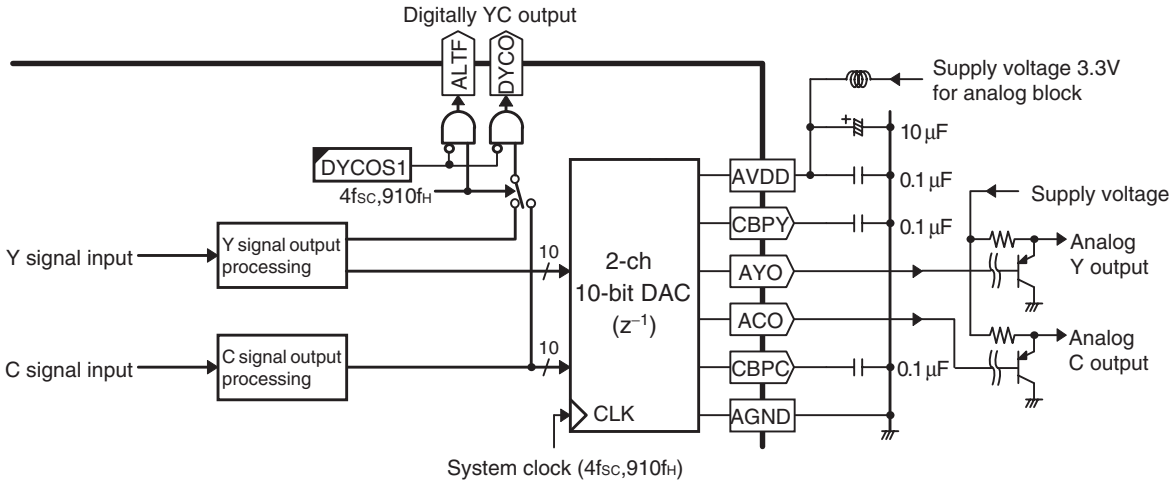
13.2 BPF and Gain Processing

COUTS on the serial bus can be used to specify whether to insert a BPF. It can also be used to specify the gain (×2 or ×1).

14. VIDEO SIGNAL OUTPUT BLOCK

The video signal output block can convert digital video signals to analog form. It can also output digital video signals without performing D/A conversion.

★ **Figure 14-1. Video Signal Output Block Diagram**



14.1 Digital YC Output Processing

When setting up DYCOS = 00 on the serial bus, DYCO9 (MSB) to DYCO0 (LSB) pins alternately output 10 bits of Y signals in straight binary and 10 bits of C signals in offset binary. And ALTF pin outputs alternative flag of Y or C signals. When ALTF = 'L' means "C Signal Outputs", when ALTF = 'H' means "Y Signal Outputs".

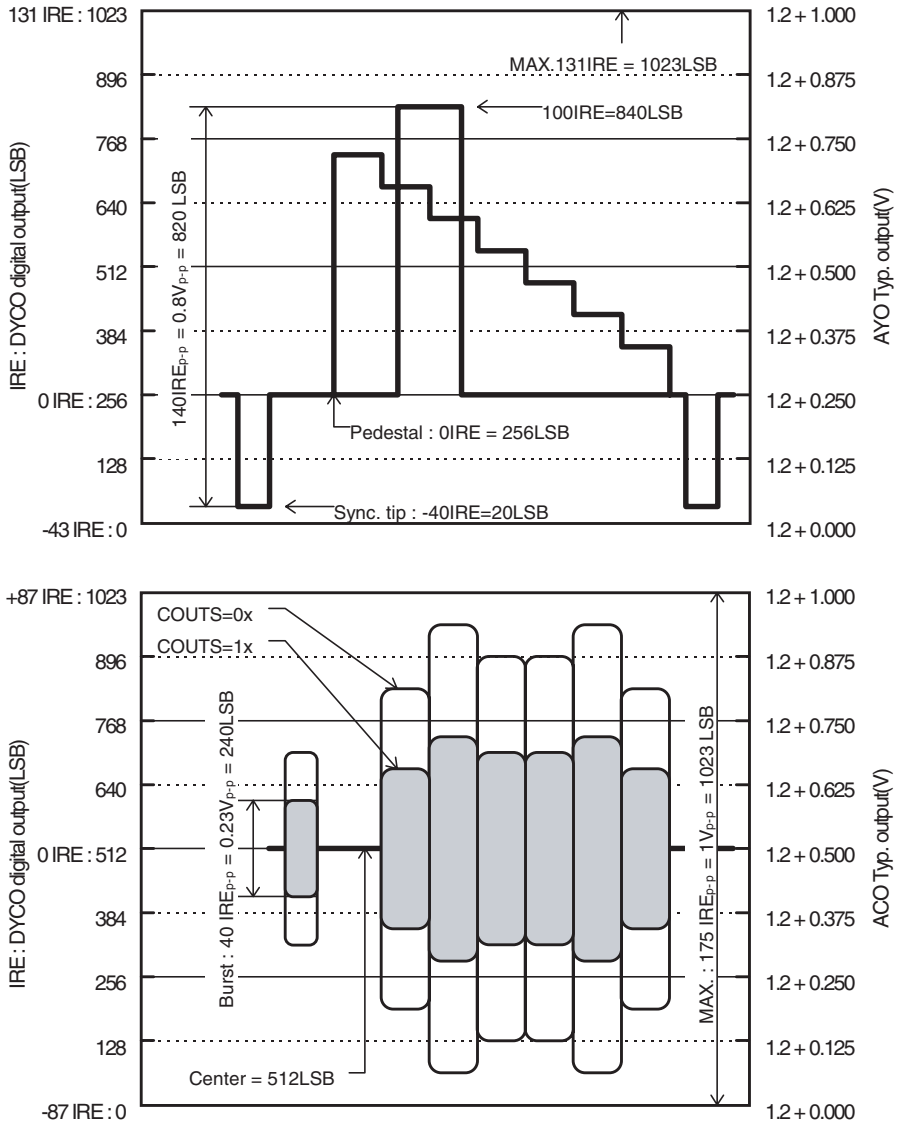
When setting up DYCOS = 1x on the serial bus, DYCO9 (MSB) to DYCO0 (LSB) and ALTF pins are high - impedance. When the DYCO pins are not used, setting DYCOS = 1x on the serial bus reduces radiation noise of these pins.

When the external Y-ADC is used, DYCO9 to DYCO0 pins are used as the digital input terminal of video signal. So the digital YC output is not available.

14.2 Video Signal Output Level

Figure 14-2 shows sample waveforms that would be observed at the AYO and ACO pins after a typical video signal is input (see **3. VIDEO SIGNAL INPUT BLOCK**).

Figure 14-2. Video Signal Output Waveform Example (for 75 % Color Bar Input)



14.3 Pin Treatment

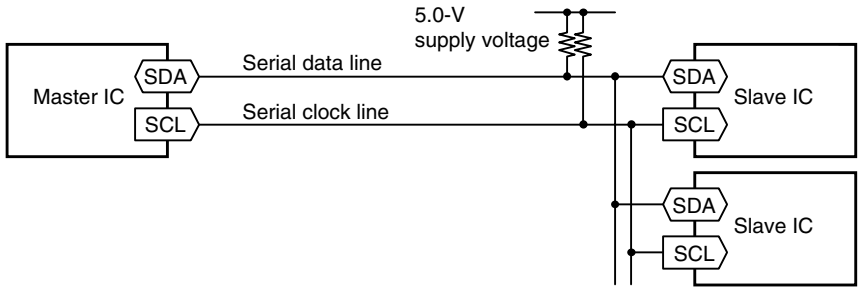
- Supply 3.3 V to the AVDD pins. Isolate them sufficiently from the digital section power supply.
- Use as wide wiring patterns as possible as the ground lines of each bypass capacitor and the AGND pins so as to minimize their impedance.
- Pull down the CBPY and CBPC pins via a 0.1 μF bypass capacitor.
- When DAC aren't used, connect AGND pin to digital ground, AVDD pin to digital power supply, and AYO, ACO, CBPY and CBPC pins set open.

15. I²C BUS INTERFACE

15.1 Basic Specification

The I²C bus is a two-wire bidirectional serial bus developed by Philips. It consists of a serial data line (SDA) for communication between ICs and a serial clock line (SCL) for establishing sync in communication.

Figure 15-1. I²C Bus Interface



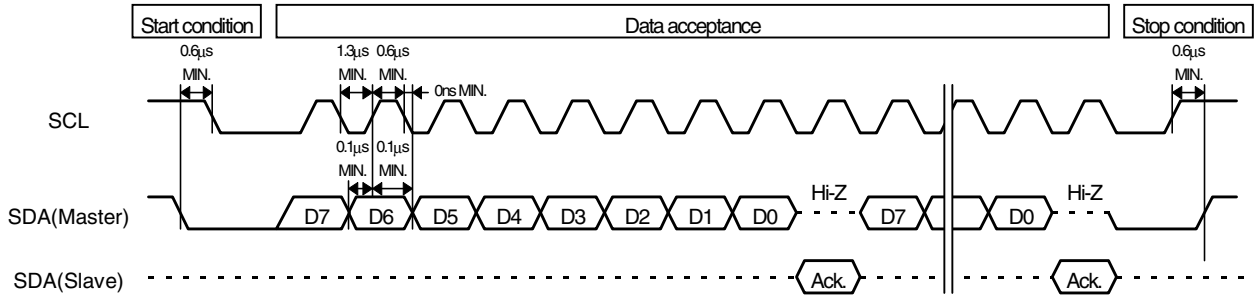
The following procedure is used to transfer data from the master IC to a slave IC.

<1> Start condition : To start communication, hold the SCL at a high level, then pull down the SDA from a high to a low level.

<2> Data transfer : To transfer data, pull up the SCL from a low to a high, while holding the current state of the SDA. Data transfer is carried out in units of 9 bits, that is, 8 data bits (D7 to D0, MSB first) plus an acknowledgment bit (ACK). A selected slave IC sets the SDA to a low when it receives bit 9 to send acknowledgment.

<3> Stop condition : To terminate communication, pull up the SDA from a low to a high upon acknowledgment, while keeping the SCL at a high.

Figure 15-2. Start Condition, Data Transfer, and Stop Condition Formats



15.2 Data Transfer Formats

Immediately when the master IC satisfies the start condition, each slave receives a slave address. If the received slave address matches that of a slave IC, communication begins between the slave IC and the master IC. If not, the SDA line is released. Two sets of slave addresses can be specified according to the SLA pin.

Table 15-1. Slave Address

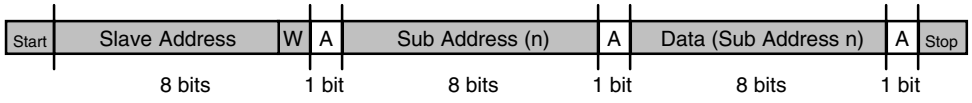
SLA pin setting (Unchangeable when power is on)	Slave address	
	Write mode	Read mode
L or open	B8h (1011100 0b)	B9h (1011100 1b)
H	BAh (1011101 0b)	BBh (1011101 1b)

(1) Write mode formats (reception mode for slaves)

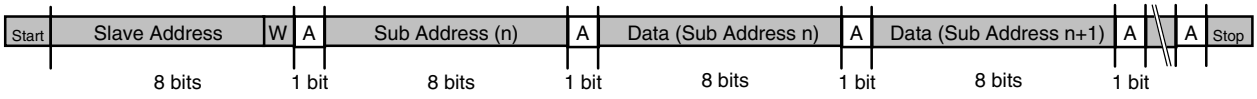
If a slave IC receives its write-mode slave address in byte 1, it continues to receive a subaddress in byte 2 and data in the subsequent bytes. The subaddress auto-increment function enables continuous data reception.

Figure 15-3. Write Mode Formats

(a) One-byte write format



(b) Multiple-byte write format



(2) Read mode format (transmission mode for slaves)

If a slave IC receives its read-mode slave address in byte 1, it sends data in byte 2 and the subsequent bytes. No subaddress is specified in this mode. Transmission begins always at address 0. Before establishing a stop condition, the master IC must send no-acknowledgment and release the SDA line.

Figure 15-4. Read Mode Format

Remark Start : Start condition
W : Write mode specification (= 0)
A : Acknowledgment
Stop : Stop condition
R : Read mode specification (= 1)
N : No-acknowledgment

XXX : Issued by the master device XXX : Issued by a slave device (μPD64082)

15.3 Resetting The I²C Bus Interface (Initialization)

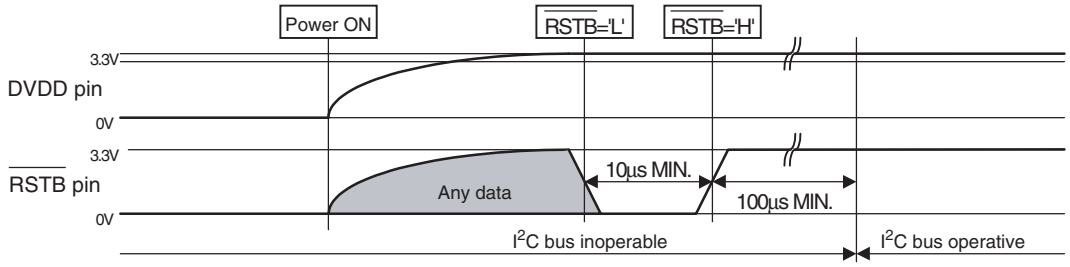
It is necessary to reset the I²C bus interface immediately when it is supplied with power. When reset, the I²C bus interface releases its SDA line and becomes operative. In addition, its write register is previously loaded with an initial value.

<1> When the power is switched on, wait until the power supply line reaches and settles on a 3.3-V level before starting initialization.

<2> Initialize the I²C bus interface circuit by keeping the $\overline{\text{RSTB}}$ pin at a low level for at least 0.5 μs.

<3> Pull up the $\overline{\text{RSTB}}$ pin to a high before starting communication on the I²C bus interface.

Figure 15-5. I²C Bus Interface Reset Timing



15.4 Serial Bus Registers

This IC incorporates twenty-four 8-bit write registers and seven 8-bit read registers. Writing to the write registers is possible in the write mode (with a slave in reception mode), while reading from the read registers is possible in the read mode (with a slave in transmission mode). The following table lists how each serial bus register is mapped.

(1) Write register mapping

Slave address: 10111000b = B8h (SLA0 = L), 10111010b = BAh (SLA0 = H)

	Data Map (SA00-SA17)							
SA	D7	D6	D5	D4	D3	D2	D1	D0
00	NRMD		HHDS		COUTS		YAPS	
01	CLKS		NSDS		MSS		KILS	
02	DYCOS		EXADINS	MFREEZE	PECS		EXCSS	
03	CPP		HDP			CDL		
04	DYCOR				DYGAIN			
05	DCCOR				DCGAIN			
06	YNRK	YNRINV	YNRLIM		CNRK	CNRINV	CNRLIM	
07	ID1ON	ID1W0A1	ID1W0A2	CLK8OFF	ST1S		ST0S	
08	WSC		VTRH		VTRR		LDSR	
09	PWREFW	PDREF			PBREF			
0A	VAPGAIN		VAPINV					
0B	0	0	YPFT		YPFG			
0C	V1PS		VEGS		CC3N	C0HS	CLPH	SELD2FH
0D	0	0	SELD1FL	0	0	1	0	1
0E	0	0	0	0	1	0	0	0
0F	0	1	0	0	0	1	0	0
10	YHCOR		YHCGAIN	ED2OFF	OVST	CSHDT	KCTT	
11	SHT		VCT	OTT	CLKG2D	CLKGGT	CLKGEB	CLKGT
12	HPLLFS	BPLLFS	FSCFG	PLLFG	KILR			
13	HSSL				VSSL			
14	BGPS				BGPW			
15	ADCLKS		ADPDS	NSDSW	NRZOFF	FSCOFF	VTVH	
16	SYSPDS	HMEMOFF	HRSTINV	HRSTTMG	HCP			
17	CNROFS	HHMG	HHFG		HHTG			

Caution It may be necessary to change set values on the serial bus depending on the results of performance evaluation conducted by NEC.

(2) Read register mapping

Slave address: 10111001b = B9h (SLA0 = L), 10111011b = BBh (SLA0 = H)

	Data Map (SA00 - SA06)							
SA	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	HHDF	KILF	NSF	LDSDF	OVSDF	OHSDF
01	WSL							
02	ED2	B3	B4	B5	B6	B7	B8	B9
03	B10	B11	B12	B13	B14	B15	B16	B17
04	VSN							
05	SVEN							
06	MVEN							

Table 15-2 lists the function of each write register. The initial and typical values for each register were determined for evaluation purposes by NEC. They are not necessarily optimum values.

Table 15-2. Write Register Functions (1/14)

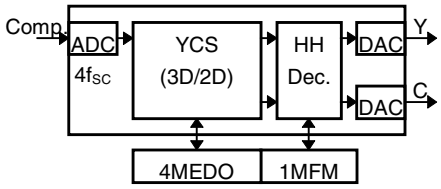
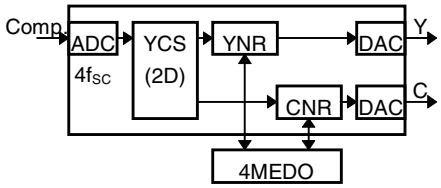
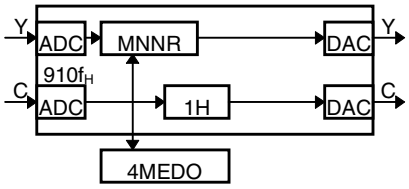
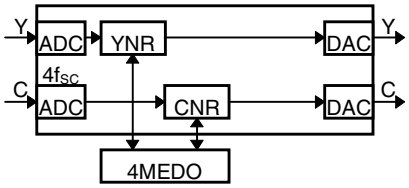
SA	Bit	Name and function	Description	Typical value	Initial value
00	D7-D6	**NRMD** Specifies an operation mode.	00 : YCS mode : YC separation (burst locked clocking)  01 : YCS+ mode : 2DYC separation and YCNR  10 : MNNR mode : frame comb type YNR+C delay (line locked clocking)  11 : YCNR mode : frame recursive YCNR(burst locked clocking) 	-	00
	D5-D4	**HHDS** Specifies whether to force HH decoding.	00: Automatic setting (according to results of WCV-ID decoding) 01: Forced HH decoding off 1x: Forced HH decoding on **Caution HH decoding is valid only in the YCS mode (NRMD = 00). Other mode need HHDS = 01 setting.**	01	01
	D3-D2	**COUTS** Specifies the way the C signal is output. (Common to digital and analog outputs)	00: Input-to-output gain of 2, without BPF processing 01: Input-to-output gain of 2, with BPF processing 10: Input-to-output gain of 1, without BPF processing 11: Input-to-output gain of 1, with BPF processing	11	11
	D1-D0	**YAPS** Specifies Y signal output correction. (Vertical aperture compensation and Y peaking filtering)	00: Correction is disabled for both analog and digital outputs. 01: Correction is enabled for only analog outputs. 10: Correction is enabled for only digital outputs. 11: Correction is enabled for both analog and digital outputs.	11	11

Table 15-2. Write Register Functions (2/14)

SA	Bit	Name and function	Description	Typical value	Initial value
01	D7-D6	**CLKS** Specifies whether to force use of the system clock.	00: Automatic setting (in an operation mode specified by NRMD) 01: Forced burst locked clocking 1x: Forced line (horizontal) locked clocking **Caution If the specified setting does not match the input signal, a malfunction may occur.**	00	00
	D5-D4	**NSDS** Specifies whether to force standard/nonstandard signal processing.	00: Adaptive processing (performed according to whether a nonstandard signal is detected) 01: Forced standard signal processing (performed regardless of whether a nonstandard signal is detected) 10: Forced horizontal sync nonstandard signal processing 11: Forced vertical sync nonstandard signal processing (forced inter-line processing) **Caution If the specified setting does not match the input signal, a malfunction may occur.**	00	00
	D3-D2	**MSS** Specifies whether to force inter-frame or inter-line processing.	00: Adaptive processing (performed according to the LINE pin input and motion detection signal) 01: Forced inter-frame processing (performed according to the LINE pin input) 1x: Forced inter-line processing	00	00
	D1-D0	**KILS** Specifies whether to force killer processing	00: Adaptive processing (performed according to the KIL pin input and internal killer detection results) 01: Internal killer detection is not used (processing is performed according to the KIL pin input only). 1x: Forced killer processing In killer processing, subtraction of the C signal from Comp. Signal is disabled.	01	00

Table 15-2. Write Register Functions (3/14)

SA	Bit	Name and function	Description	Typical value	Initial value
02	D7-D6	**DYCOS** Specifies DYCO pin input/output.	00: Y/C separation signal alternate output 01: Test mode (forbidden setting) 1x: High impedance	10	10
★	D5	**EXADINS** Specifies whether to select external Y-ADC.	0: Internal Y-ADC 1: External Y-ADC (digital video signal, converted from analog form, is input to the DYCO9 to DYCO2 pins) Refer to **3.4 Pin Treatment**	0	0
	D4	**MFREEZE** External memory test bit	0: Normal mode 1: Test mode (forbidden setting)	0	0
	D3-D2	**PECS** Specifies a pedestal error correction test bit.	00: Normal setting 01: Test setting (forbidden setting) 10: Test setting (forbidden setting) 11: Test setting (forbidden setting)	00	00
	D1-D0	**EXCSS** Specifies whether to use external C sync input.	00: Internally separated sync signal is always used ($\overline{CSI}$ input is not used). 01: Sync signal input at the $\overline{CSI}$ pin is used during out-of-sync state. 1x: Sync signal input at the $\overline{CSI}$ pin is always used.	01	01
03	D7-D6	**CPP** Specifies the amplitude of the internal Y-ADC input and a clamp method.	PWREFW (SA09h:D7) = 0 CPP: ADC input amplitude Clamp pulse width 00 : Y-ADC & C-ADC V_{TB} = 1.00 V_{p-p}, 2.2 μs 01 : Y-ADC & C-ADC V_{TB} = 1.00 V_{p-p}, 1.1 μs 10 : Y-ADC & C-ADC V_{TB} = 1.25 V_{p-p}, 2.2 μs 11 : Y-ADC & C-ADC V_{TB} = 1.25 V_{p-p}, 1.1 μs PWREFW (SA09h:D7) = 1 CPP: ADC input amplitude Clamp pulse width 00 : Y-ADC:V_{TB}=1.25 V_{p-p}, C-ADC:V_{TB}=1.00 V_{p-p} 2.2 μs 01 : Y-ADC:V_{TB}=1.25 V_{p-p}, C-ADC:V_{TB}=1.00 V_{p-p} 1.1 μs 10 : Y-ADC:V_{TB}=1.00 V_{p-p}, C-ADC:V_{TB}=1.25 V_{p-p} 2.2 μs 11 : Y-ADC:V_{TB}=1.00 V_{p-p}, C-ADC:V_{TB}=1.25 V_{p-p} 1.1 μs	10	00
	D5-D3	**HDP** Fine adjustment of system horizontal phase	000: −1.12 μs to 100: ±0.00 μs (Typ.) to 111: +0.84 μs Fine-adjusts the horizontal-processing phase with respect to the horizontal sync signal. (0.28 μs/step)	100	100
	D2-D0	**CDL** Fine adjustment of C signal output delay	000: −280 ns to 100: ±0 ns (Typ.) to 111: +210 ns Fine-adjusts the C signal phase with respect to the Y signal. (70 ns/step)	100	100

Table 15-2. Write Register Functions (4/14)

SA	Bit	Name and function	Description	Typical value	Initial value
04	D7-D4	**DYCOR** DY detection coring level (Y motion detection coring)	0000: Coring 0 (Closer to motion pictures) to 1111: Large amount of coring (Closer to still pictures) The coring level for inter-frame Y difference detection is specified. A signal smaller than specified is assumed to be noise, resulting in '0' being output.	0010	0011
	D3-D0	**DYGAIN** DY detection gain (Y motion detection gain)	0000: Gain of 0 (Closer to still pictures) to 1111: Maximum gain (Closer to motion pictures) Inter-frame Y difference detection gain is specified.	1001	0110
05	D7-D4	**DCCOR** DC detection coring level (C motion detection coring)	0000: Coring 0 (Closer to motion pictures) to 1111: Large amount of coring (Closer to still pictures) The coring level for inter-frame C difference detection is specified. A signal smaller than specified is assumed to be noise, resulting in 0 being output.	0011	0011
	D3-D0	**DCGAIN** DC detection gain (C motion detection gain)	0000: Gain of 0 (Closer to still pictures) to 1111: Maximum gain (Closer to motion pictures) Inter-frame C difference detection gain is specified.	0110	0110

Table 15-2. Write Register Functions (5/14)

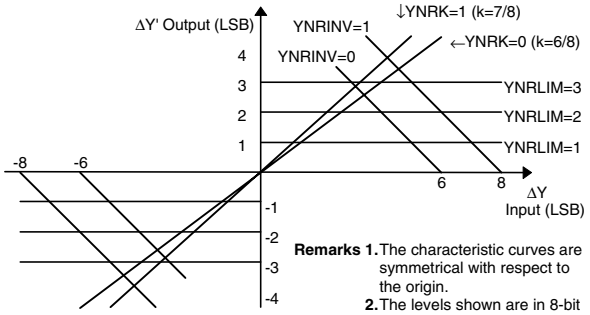
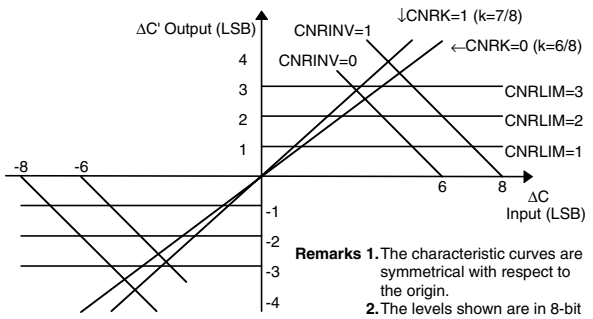
SA	Bit	Name and function	Description	Typical value	Initial value
06	D7	**YNRK** Specifies the frame recursive YNR nonlinear filter gain.	0: x 6/8 (small noise reduction effect and small after-image) 1: x 7/8 (large noise reduction effect and large after-image) The magnitude of the NR effect is specified.	0	0
	D6	**YNRINV** Specifies the frame recursive YNR nonlinear filter convergence level.	0: 6 LSB (small noise reduction effect and small after-image) 1: 8 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in 0 being output.	0	0
	D5-D4	**YNRLIM** Specifies the frame recursive YNR nonlinear filter limit level.	00: 0 LSB (YNR off) to 11: 3 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in a limit value being output. Nonlinear characteristic curve based on YNRK, YNRINV, and YNRLIM  **Remarks 1.** The characteristic curves are symmetrical with respect to the origin. **2.** The levels shown are in 8-bit terms.	01	00
	D3	**CNRK** Specifies the frame recursive CNR nonlinear filter gain.	0: x 6/8 (small noise reduction effect and small after-image) 1: x 7/8 (large noise reduction effect and large after-image) The magnitude of the NR effect is specified.	0	0
	D2	**CNRINV** Specifies the frame recursive CNR nonlinear filter convergence level.	0: 6 LSB (small noise reduction effect and small after-image) 1: 8 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in 0 being output.	0	0
	D1-D0	**CNRLIM** Specifies the frame recursive CNR nonlinear filter limit level.	00: 0 LSB (CNR off) to 11: 3 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in a limit value being output. Nonlinear characteristic curve based on CNRK, CNRINV, and CNRLIM  **Remarks 1.** The characteristic curves are symmetrical with respect to the origin. **2.** The levels shown are in 8-bit terms.	01	00

Table 15-2. Write Register Functions (6/14)

SA	Bit	Name and function	Description	Typical value	Initial value
07	D7	**ID1ON** Specifies whether to superimpose ID-1 specification ID signal.	0: Through (no superimposition) 1: Forced superimposition **Caution Do not set this bit to 1 during no-signal state.**	-	0
	D6	**ID1W0A1** Specifies whether to set bit A1 of ID-1 word 0.	0: 0 (transmission aspect of 4:3) 1: 1 (transmission aspect of 16:9)	-	0
	D5	**ID1W0A2** Specifies whether to set bit A2 of ID-1 word 0.	0: 0 (image display format = normal) 1: 1 (image display format = letter box)	-	0
	D4	**CLK8OFF** Specifies the state of the CLK8 pin output.	0: Active-low (to output $8f_{SC}$ clock pulse) 1: Fixed to low level (to reduce radiation noise)	1	0
	D3-D2	**ST1S** Specifies internal signal monitor output for the ST1 pin.	00: Mode flag (L = YCS, H = MNNR or YCNR) 01: Internal Y-ADC clamp pulse (active-high) 10: Composite sync (active-low) 11: H sync (active-high)	-	00
	D1-D0	**ST0S** Specifies internal signal monitor output for the ST0 pin.	00: HH decode flag (L = non-decoding, H = decoding) 01: External Y-ADC clamp pulse (active-high) 10: HV blanking (active-high) 11: V sync (active-low)	-	00

Table 15-2. Write Register Functions (7/14)

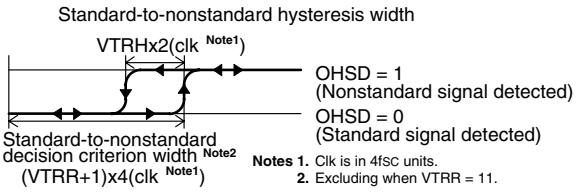
SA	Bit	Name and function	Description	Typical value	Initial value
08	D7-D6	**WSC** Specifies the amount of noise detection coring.	00: 0LSB (high detection sensitivity) 01: 1LSB 10: 2LSB 11: 3LSB (low detection sensitivity) Specifies an input coring value for the noise detection circuit. Detection results are not used within the device.	01	01
	D5-D4	**VTRH** Specifies hysteresis for horizontal sync nonstandard signal detection (out-of-horizontal sync intra-field)	00: Hysteresis off (width of 0 clock pulses) 01: Low hysteresis (width of 2 clock pulses) 10: Medium hysteresis (width of 4 clock pulses) 11: High hysteresis (width of 6 clock pulses) For horizontal sync nonstandard signal detection, a criterion value to detect an out-of-horizontal sync state intra-field is decreased by a value indicated above.	01	01
	D3-D2	**VTRR** Specifies sensitivity for horizontal sync nonstandard signal detection (out-of-horizontal sync intra-field)	00: High detection sensitivity (width of ±4 clock pulses) 01: Medium detection sensitivity (width of ±8 clock pulses) 10: Low detection sensitivity (width of ±12 clock pulses) 11: Detection off If the degree of out-of-horizontal sync state intra-field becomes larger than specified, a horizontal sync nonstandard signal is assumed to have been detected. Horizontal sync nonstandard signal detection characteristic curve  **Notes 1.** Clk is in 4fSC units. **2.** Excluding when VTRR = 11.	01	01
	D1-D0	**LDSR** Specifies sensitivity for frame sync nonstandard signal detection (out-of-horizontal sync inter-frame)	00: High detection sensitivity (width of 0.5 clock pulses) 01: Medium detection sensitivity (width of 1 clock pulse) 10: Low detection sensitivity (width of 1.5 clock pulses) 11: Detection off If the degree of out-of-horizontal sync state inter-frame becomes larger than specified, a frame sync nonstandard signal is assumed to have been detected.	10	01

Table 15-2. Write Register Functions (8/14)

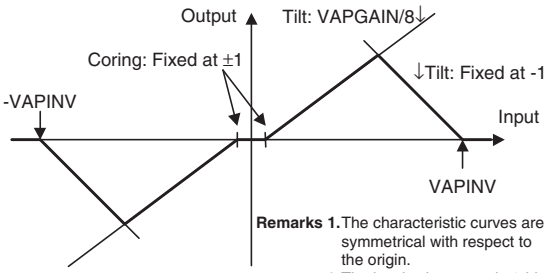
SA	Bit	Name and function	Description	Typical value	Initial value
09	D7	**PWREFW** Internal ADC input range	0 : Same input range on Y-ADC and C-ADC 1 : Different input range on Y-ADC and C-ADC Refer to **CPP (SA03, D7 - D6)**	0	0
	D6-D4	**PDREF** Test bit	Setting of this bit is invalid in this IC.	100	100
	D3-D0	**PBREF** Test bit	Setting of this bit is invalid in this IC.	1000	1000
0A	D7-D5	**VAPGAIN** Specifies a vertical aperture compensation gain.	000: Correction off to 111: Maximum correction (0.875 times)	-	000
	D4-D0	**VAPINV** Specifies a vertical aperture compensation convergence point.	00000: Correction off to 11111: Maximum correction Vertical aperture compensation characteristic curve based on VAPGAIN and VAPINV  **Remarks 1.** The characteristic curves are symmetrical with respect to the origin. **2.** The levels shown are in 8-bit terms.	-	00000

Table 15-2. Write Register Functions (9/14)

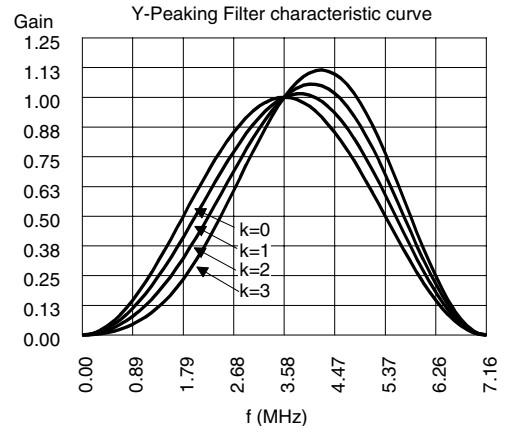
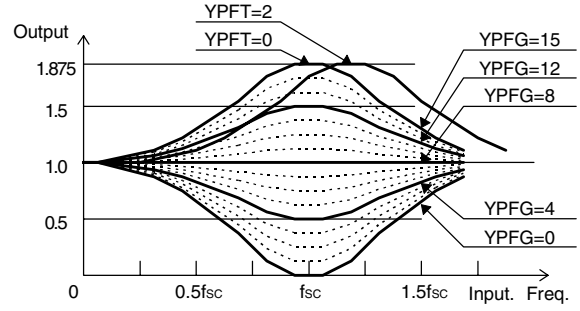
SA	Bit	Name and function	Description	Typical value	Initial value
0B	D7	**TEST** Test bit	0: Normal mode 1: Test mode (forbidden setting)	0	0
	D6	**TEST** Test bit	0: Normal mode 1: Test mode (forbidden setting)	0	0
	D5-D4	**YPFT** Specifies the Y peaking filter (BPF) center frequency.	00: 3.58 MHz 01: 3.86 MHz 10: 4.08 MHz 11: 4.22 MHz 	11	11
	D3-D0	**YPFG** Specifies a Y peaking filter gain.	0000: −1.0 times to 1000: ±0.0 times to 1111: +0.875 times Y signal output frequency characteristic curve based on YPFT and YPFG 	1000	1000

Table 15-2. Write Register Functions (10/14)

SA	Bit	Name and function	Description	Typical value	Initial value
0C	D7-D6	**V1PSEL** Line comb filter horizontal dot interference suppression level	00: Suppression off 01: Low suppression level 10: Medium suppression level 11: High suppression level Horizontal dot interference is reduced at inter-line Y/C separation.	10	10
	D5-D4	**VEGSEL** Line comb filter vertical dot interference suppression level	00: Suppression off 01: Low suppression level 10: Medium suppression level 11: High suppression level Vertical dot interference is reduced at inter-line Y/C separation.	10	10
	D3	**CC3N** Selects a line comb filter C separation filter characteristic.	0: Narrow bandwidth 1: Wide bandwidth	0	0
	D2	**C0HS** Specifies C signal delay time extension at NR	0: 1H delay 1: No 1H delay	0	0
	D1	**CLPH** Y-ADC clamp test bit	0: Normal mode 1: Test mode (forbidden setting)	0	0
	D0	**SELD2FH** Specifies DC detection High-frequency sensitivity.	0: Low sensitivity, Closer to still pictures 1: High sensitivity, Closer to motion pictures	0	0
0D	D7	-	0	0	0
	D6	-	0	0	0
	D5	**SELD1FL** Specifies DY detection low-frequency sensitivity.	0: Low sensitivity, Closer to still pictures 1: High sensitivity, Closer to motion pictures	0	0
	D4	-	0	0	0
	D3	-	0	0	0
	D2-D0	-	101	101	101
0E	D7-D4	-	0000	0000	0000
	D3-D0	-	1000	1000	1000
0F	D7-D4	-	0100	0100	0100
	D3-D0	-	0100	0100	0100

Table 15-2. Write Register Functions (11/14)

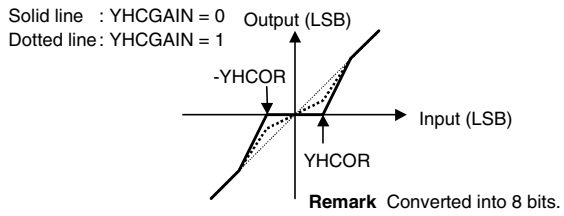
SA	Bit	Name and function	Description	Typical value	Initial value
10	D7-D6	**YHCOR** Specifies Y output high frequency component coring.	00: Coring off 01: Small amount of coring (±1 LSB: 8-bit terms) 10: Medium amount of coring (±2 LSB: 8-bit terms) 11: Large amount of coring (±3 LSB: 8-bit terms) Coring characteristic curve (for high-frequency component only)  **Remark** Converted into 8 bits.	00	00
	D5	**YHCGAIN** Specifies Y output high-frequency component coring gain.	0: Normal (×1) 1 :1/2 gain Refer to **YHCOR (SA10h, D7-D6)**	0	0
	D4	**ED2OFF** Specifies WCV-ID detection circuit.	0: Normal mode 1: Forced WCV-ID detection circuit turned off	0	0
	D3	**OVST** Nonstandard signal detection test bit	0: Normal mode 1: Test mode	0	0
	D2	**CSHDT** H / V counter test bit	0: Normal mode 1: Test mode	0	0
	D1-D0	**KCTT** H / V counter test bit	0x: Normal mode 1x: Test mode	00	00

Table 15-2. Write Register Functions (12/14)

SA	Bit	Name and function	Description	Typical value	Initial value
11	D7	**SHT1** Nonstandard signal detection test bit	0: Normal mode 1: Test mode	0	0
	D6	**SHT0** Nonstandard signal detection test bit	0: Normal mode 1: Test mode	0	0
	D5	**VCT** H / V counter test bit	0: Normal mode 1: Test mode	0	0
	D4	**CLKGAT** H / V counter test bit	0: Normal mode 1: Test mode	0	0
	D3	**CLKG2D** Clock generator section test bit	0: Test mode 1: Normal mode	1	0
	D2	**CLKGGT** Clock generator section test bit	0: Normal mode 1: Test mode	0	0
	D1	**CLKGEB** Clock generator section test bit	0: Normal mode 1: Test mode	0	0
	D0	**CLKGT** Clock generator section test bit	0: Normal mode 1: Test mode	0	0
12	D7	**HPLLFS** Specifies the horizontal PLL filter.	0: Slow convergence 1: Quick convergence (must be set to 1 when MN signal is input)	-	1
	D6	**BPLLFS** Specifies the burst PLL filter.	0: Quick convergence 1: Slow convergence	1	0
	D5	**FSCFG** Specifies the burst extraction gain.	0: High gain 1: Low gain	0	1
	D4	**PLLFG** Specifies the PLL loop gain.	0: Low gain (slow convergence) 1: High gain (quick convergence)	1	1
	D3-D0	**KILR** Killer detection reference	0000: Detection off 0001: Low detection sensitivity to 1111: High detection sensitivity	0010	1011
13	D7-D4	**HSSL** Horizontal sync slice level	0000: 4LSB to 1111: 19LSB (in 8-bit input terms, 1LSB/step)	1111	1100
	D3-D0	**VSSL** Vertical sync slice level	0000: HSSL setting + 0LSB to 1111: HSSL setting + 15LSB (in 8-bit input terms, 1LSB/step)	1000	1000

Table 15-2. Write Register Functions (13/14)

SA	Bit	Name and function	Description	Typical value	Initial value
14	D7-D4	**BGPS** Specifies the internal burst gate start position.	0000: H sync center + 2 μs to 1111: H sync center + 5.75 μs Calculation of gate start position from the H sync center : 0.25 × BGPS + 2.5 (μs)	0101	0100
	D3-D0	**BGPW** Specifies the internal burst gate width.	0000: 0.5 μs to 1111: 4.25 μs Calculation of gate width : 0.25 × BGPW + 0.5 (μs)	0011	1010
15	D7-D6	**ADCLKS** Specifies the ADC clock delay.	00: 0 ns typically (forbidden setting) 01: 3 ns typically 10: 17.5 ns typically 11: 20.5 ns typically **Remark** These delay times are relative to the "00" setting.	11	10
★	D5	**ADPDS** Specifies whether to use ADC power-down.	0: Do not stop operation of ADC not in use.(High current drain) 1: Stop operation of ADC not in use. (Low current drain)	1	1
	D4	**NRDSW** Non-standard detection section test bit	0: Normal mode 1: Test mode	0	0
	D3	**NRZOFF** WCV-ID detection NRZ section check	0: NRZ section amplitude check on 1: NRZ section amplitude check off	0	0
	D2	**FSCOFF** WCV-ID detection FSC section check	0: FSC amplitude check on 1: FSC amplitude check off	0	0
	D1-D0	**VTVH** Specifies WCV signal no-image section processing (only letter box signal is valid).	00: Ordinary processing 10: Forced inter-frame Y/C separation 10: Forced inter-line Y/C separation 11: Forced through (composite signal is output.)	00	00
16	D7	**SYSPDS** Memory power down	0: Normal operation 1: Power down When this bit is set to "1", EDO memory and field memory control pins ($\overline{MRAS}$, $\overline{MCAS}$, $\overline{MWE}$, $\overline{MOE}$, MA7 to MA0, HWCK, HRCK, HRST, HO3 to HO0) are released (set to Hi-Z) and the internal system clock is set to free running, so video output is disabled.	-	0
★	D6	**HMEMOFF** Specifies whether to release field memory.	0: Use (with HH decoding) 1: Release (HO3 to HO0, HWCK, HRCK, and HRST pins: High-impedance state)	-	0
	D5	**HRSTINV** Specifies field memory reset polarity.	0: Active-high type (Example : OKI MSM514222B) 1: Active-low type	-	0
	D4	**HRSTTMG** Specifies the field memory address phase.	0: Write address +0 type (Example : MSM514222B) 1: Write address −1 type (Example : MSM514221B)	-	0
	D3-D0	**HCP** HH carrier phase adjustment	0000: −180 ° to 0111: 0 ° to 1110: +180 ° Note : Carrier phase calculation: (HCP − 7) / 14 × 360 °)	0111	0000

Table 15-2. Write Register Functions (14/14)

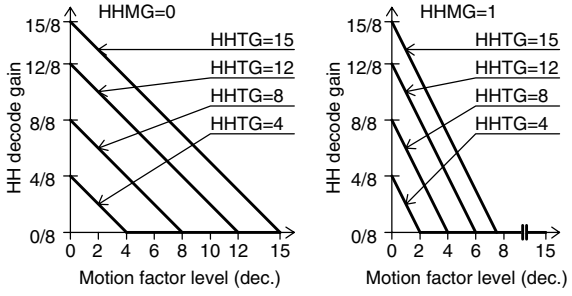
SA	Bit	Name and function	Description	Typical value	Initial value
17	D7	**CNROFS** CNR section test bit	0: Normal mode 1: Test mode	0	0
	D6	**HHMG** Specifies the HH decode motion gain.	0: Decrease the HH decode gain according to the motion factor gradually. 1: Decrease the HH decode gain according to the motion factor abruptly.	1	0
	D5	**HHFG1** Specifies whether to use HH output coring.	0: Coring on (±2 LSB : for 8-bit terms) 1: Coring off	0	0
	D4	**HHFG0** Specifies the gain for forced HH decoding.	0: Motion-adaptive gain processing (the gain is reduced according to the motion factor). 1: Fixed at forced gain (processing always assumes motion factor = 0).	0	0
	D3-D0	**HHTG** Specifies the maximum HH decode gain. (gain for motion signal = 0)	0000: 0/8 times to 1000: 8/8 times to 1111: 15/8 times (k = HHTG/8) HH decode gain characteristic curves based on HHMG, HHTG, and motion factor 	1000	0000

Table 15-3. Read Register Functions

SA	Bit	Name and function	Description	Initial value
00	D7-D6	- Undefined	Undefined	-
	D5	**HHDF** HH decode flag	0: HH decoding not in progress 1: HH decoding in progress	-
	D4	**KILF** Killer detection flag	0: Color signal detected 1: Killer signal (non-burst signal) detected	-
	D3	**NSDF** Horizontal sync signal detection flag	0: Sync signal detected 1: No sync signal detected	-
	D2	**LDSDF** Frame sync nonstandard signal detection flag	0: Standard signal detected 1: Nonstandard signal detected (such as laser disc special playback signal)	-
	D1	**OVSDF** Vertical sync nonstandard signal detection flag	0: Standard signal detected 1: Nonstandard signal detected (such as VCR special playback signal and home TV game signal)	-
	D0	**OHSDF** Horizontal sync nonstandard signal detection flag	0: Standard signal detected 1: Nonstandard signal detected (such as VCR ordinary playback signal)	-
01	D7-D0	**WSL** Noise level detection data	00000000: Closer to low noise 11111111: Closer to high noise	-
02	D7	**ED2** WCV-ID signal detection flag	0: Invalid (no WCV-ID signal detected) 1: Valid (WCV-ID signal detected)	-
	D6-D0	**B3-B9** WCV ID signal decoding result		-
03	D7-D0	**B10-B17** WCV ID signal decoding result		-
04	D7-D0	**VSN**	For device test (undefined value)	-
05	D7-D0	**SVEN**	For device test (undefined value)	-
06	D7-D0	**MVEN**	For device test (undefined value)	-

16. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = +25 °C Unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Digital section supply voltage	DV_{DD}		−0.3 to +4.6	V
Analog section supply voltage	AV_{DD}	0.3 < (DV_{DD} − AV_{DD}) < +0.3	−0.3 to +4.6	V
Input voltage	V_{I5V}	5 V-resistant input pins	−0.3 to +5.5	V
	V_I	Other input pins	−0.3 to V_{DD} + 0.3	V
Output current	I_O		−10 to +10	mA
Package allowable dissipation	P_D	When mounted on an epoxy-glass board (T_A = +70 °C, 100 mm × 100 mm, 2-mm thick)	862	mW
Operating temperature (device ambient temperature)	T_A		−20 to +70	°C
Operating temperature (upper limit to junction temperature)	$T_{J:MAX}$	Thermal resistance between junction and package surface : θ_{JC} = 21 °C/W (calculated value)	+125	°C
Storage temperature	T_{stg}		−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under condition that ensure that the absolute maximum ratings are not exceed.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Digital section supply voltage	DV_{DD}		3.0	3.3	3.6	V
Analog section supply voltage	AV_{DD}	−0.3 < (DV_{DD} − AV_{DD}) < +0.3	3.0	3.3	3.6	V
High-level input voltage	V_{IH}	TTL input pin	2.0		5.5	V
Low-level input voltage	V_{IL}		0		0.8	V
High-level input voltage	V_{IH}	Schmitt input pin	3.0		5.5	V
Low-level input voltage	V_{IL}		0		0.5	V
Reference clock input frequency	f_{XI}	XI pin	19.998	20.000	20.002	MHz
Reference clock input amplitude	V_{XI}		0.8		DV_{DD}	V_{p-p}
Subcarrier input frequency	f_{FSCI}	FSCI pin		3.579545		MHz
Subcarrier input amplitude	V_{FSCI}		0.45		AV_{DD}	V_{p-p}
★ Composite / Y signal Video signal input amplitude	V_{AYI}	AYI pin, Picture + Sync. amp. (140IRE$_{p-p}$), AV_{DD} = 3.3 V, CPP (SA03: D7-D6) = 1x		1.0		V_{p-p}
★ Composite / Y signal Sync. signal input amplitude	$V_{AYI(S)}$	AYI pin, Sync. amp. (40IRE$_{p-p}$), AV_{DD} = 3.3 V, CPP = 1x		286 (±0 dB)	360 (+2 dB)	mV_{p-p}
C signal input amplitude	V_{ACI}	ACI pin, burst amplitude (40IRE$_{p-p}$) part, AV_{DD} = 3.3 V, CPP = 1x		286 (±0 dB)	360 (+2 dB)	mV_{p-p}

Digital Section DC Characteristics (DV_{DD} = 3.3 ± 0.3 V, DGND = 0 V, T_A = –20 to +70 °C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Digital section current drain	DI_{DD}	DVDD and DGND pins			79	122	mA
Input leakage current	I_{LI}	Ordinary input	V_I = DV_{DD} or 0 V	–10	0	+10	μA
High-level input current	I_{IH}	Pull-down type	V_I = DV_{DD}	20	120	210	μA
Low-level input current	I_{IL}	Pull-up type	V_I = 0 V	–180	–80	–30	μA
High-level output current 1	I_{OH1}	3.0 mA type	V_{OH1} = 2.4 V			–3.0	mA
Low-level output current 1	I_{OL1}		V_{OL1} = 0.4 V	+3.0			mA
High-level output current 2	I_{OH2}	1.0 mA type	V_{OH2} = 2.4 V			–1.0	mA
Low-level output current 2	I_{OL2}		V_{OL2} = 0.4 V	+1.0			mA
Low-level output current 3	I_{OL3}	N-ch. open drain	V_{OL3} = 0.4 V	+5.0			mA
Output leakage current	I_{LO}	3-state, open drain	V_O = DV_{DD} to DGND	–10	0	+10	μA

★ **Analog Section (ADC, DAC, f_{SC} DAC, 8f_{SC} PLL) DC Characteristics**

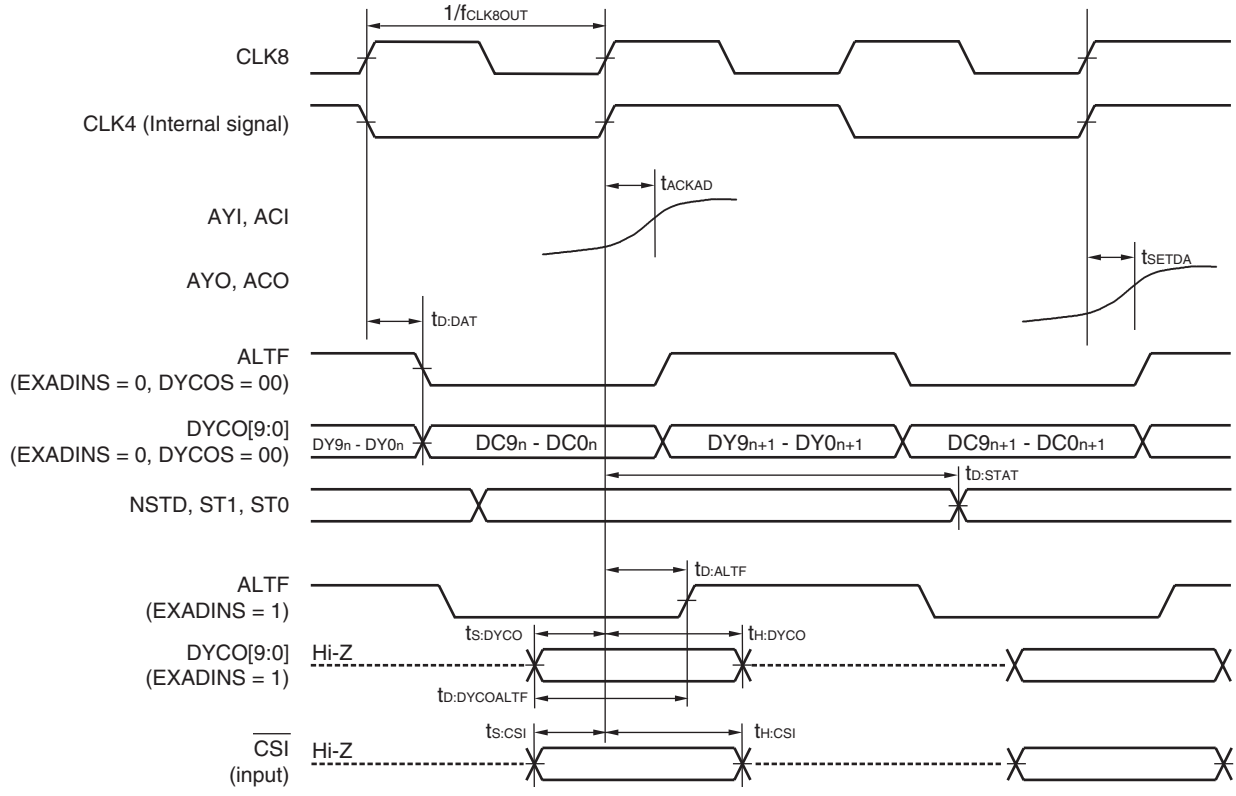
(AV_{DD} = 3.3 ± 0.3 V, AGND = 0 V, T_A = +25 °C Unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Analog section current drain	AI_{DD}	AVDD and AGND pins		75	117	mA
Y-ADC resolution	RES_{ADY}	AYI pin, AV_{DD} = 3.3 V, f_S = 4 f_{SC}, CPP = 1x, PWREFW = 0, ADCLKS = 11 DGAD, DPAD : NTSC 100IRE RAMP	-	10	-	bit
Y-ADC integral linearity error	ILE_{ADY}			±3.0	±6.0	LSB
Y-ADC differential linearity error	$DLE_{AD:Y}$			±1.0	±2.0	LSB
Y-ADC differential gain	$DG_{AD:Y}$			±1.7	±3.0	%
Y-ADC differential phase	$DP_{AD:Y}$			±1.0	±3.0	Deg
C-ADC resolution	RES_{ADC}	ACI pin, AV_{DD} = 3.3 V, f_S = 4 f_{SC}, CPP = 1x, PWREFW = 0, ADCLKS = 11 DGAD, DPAD : NTSC 100IRE RAMP @ 80% of Full Range	-	8	-	bit
C-ADC integral linearity error	ILE_{ADC}			±1.5	±3.0	LSB
C-ADC differential linearity error	$DLE_{AD:C}$			±1.0	±3.0	LSB
C-ADC differential gain	$DG_{AD:C}$			±1.7	±3.5	%
C-ADC differential phase	$DP_{AD:C}$			±1.0	±3.0	Deg
Y-ADC reference voltage 1(low)	V_{RBADY1}	Internal Y-ADC input range 1 V_{p-p} mode AV_{DD} = 3.3 V, CPP = 0x, PWREFW = 0 V_{INT} = 1.8 V, V_{INB} = 0.8 V		1.05		V
Y-ADC reference voltage 1(high)	V_{RTADY1}			1.55		V
Y-ADC analog input range1	V_{INAY1}			1.00		V
Y-ADC clamp pin voltage 1	V_{CLY1}			0.84		V
Y-ADC reference voltage 2(low)	V_{RBADY2}	Internal Y-ADC input range 1.25 V_{p-p} mode AV_{DD} = 3.3 V, CPP = 1x, PWREFW = 0 V_{INT} = 1.925 V, V_{INB} = 0.675 V		0.99		V
Y-ADC reference voltage 2(high)	V_{RTADY2}			161		V
Y-ADC analog input range2	V_{INAY2}			1.25		V
Y-ADC clamp pin voltage 2	V_{CLY2}			0.72		V
C-ADC reference voltage1(low)	V_{RBADC1}	Internal C-ADC input range 1.25 V_{p-p} mode AV_{DD} = 3.3 V, CPP = 1x, PWREFW = 0		2.05		V
C-ADC reference voltage1(high)	V_{RTADC1}			3.30		V
C-ADC reference voltage 1 (V_{RT}-V_{RB} difference voltage)	V_{TBADC1}		1.15	1.25	1.35	V
C-ADC input bias voltage 1	V_{ACI1}			2.68		V
ADC analog input capacitance	C_{INAD}	AYI pin = V_{RBADY1} ACI pin = V_{RBADC1}		25		pF
DAC resolution	RES_{DA}	AYO and ACO pins, AV_{DD} = 3.3 V, f_S = 4f_{SC} DGAD, DPAD : NTSC 140IRE RAMP	-	10	-	bit
DAC integral linearity error	ILE_{DA}			±1.0	±3.0	LSB
DAC differential linearity error	DLE_{DA}			±0.3	±1.0	LSB
DAC differential gain	DG_{DA}			±1.0	±3.0	%
DAC differential phase	DP_{DA}			±0.3	±1.0	deg
DAC full-scale output voltage	V_{FSDA}	AYO and ACO pins, AV_{DD} = 3.3 V	1.7	2.2	2.6	V
DAC zero-scale output voltage	V_{ZSDA}		0.8	1.2	1.6	V
DAC output amplitude	V_{OPPDA}		0.90	1.00	1.10	V_{p-p}
f_{SC} DAC resolution	RES_{FSC}	FSCO pin	-	8	-	bit

Digital Section AC Characteristics (DV_{DD} = 3.3 ± 0.3 V, DGND = 0 V, C_L = 15 pF, $t_r = t_f$ = 2 ns, T_A = –20 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Video data output delay	$t_{D:DAT}$	CLK8↑ → DYCOn, ALTF (EXADINS = 0)	3	9		ns
Internal signal monitor output delay	$t_{D:STAT}$	CLK8↑→ NSTD, ST1, ST0	35	45	55	ns
$\overline{CSI}$ input set-up time	$t_{S:CSI}$	$\overline{CSI}$ → CLK8↑	0			ns
$\overline{CSI}$ input hold time	$t_{H:CSI}$	CLK8↑ → $\overline{CSI}$	15			ns
ALTF output delay + DYCOn input set-up time	$t_{D:DYCOALTF}$	CLK8↑ → ALTF + : $t_{S:DYCO}$: EXADINS = 1, ADCLKS = xx			35	ns
ALTF output delay 0	$t_{D:ALTF0}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 00	3			ns
ALTF output delay 1	$t_{D:ALTF1}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 01	5			ns
ALTF output delay 2	$t_{D:ALTF2}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 10	18		38	ns
ALTF output delay 3	$t_{D:ALTF3}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 11	20		40	ns
DYCOn input set-up time	$t_{S:DYCO}$	DYCOn → CLK8↑ : EXADINS = 1	0			ns
DYCOn hold time	$t_{H:DYCO}$	CLK8↑ → DYCOn : EXADINS = 1	10			ns
Input capacitance	C_I	DV_{DD} = V_I = 0 V, f_{IN} = 1 MHz		10	15	pF

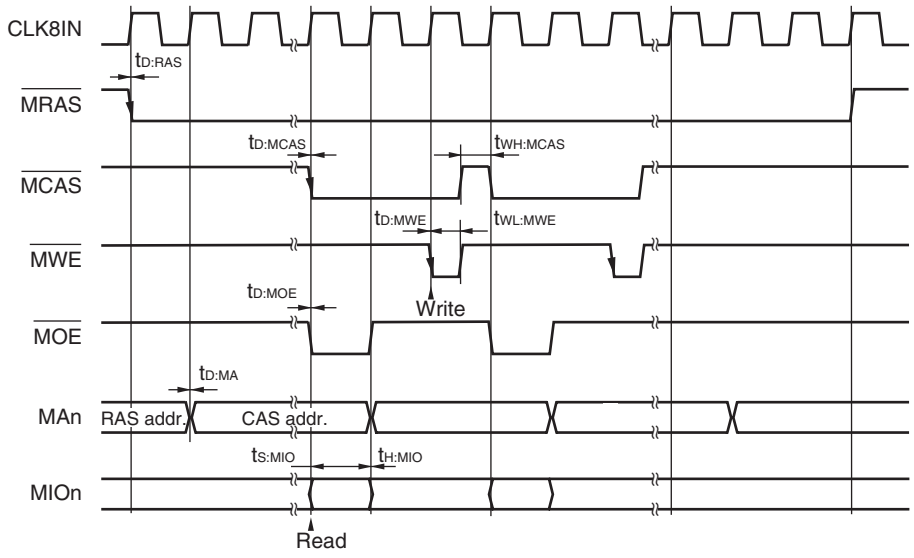
★

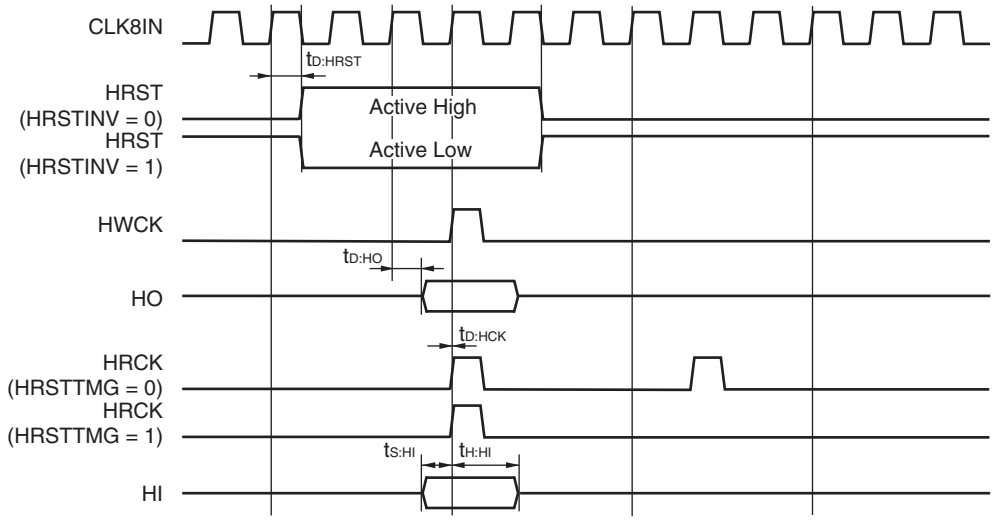


Memory Interface Section AC Characteristics

(DV_{DD} = 3.3 ± 0.3 V, DGND = 0 V, C_L = 15 pF, $t_r = t_f$ = 2 ns, T_A = –20 to + 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{MRAS}$ output delay	$t_{D:RAS}$	CLK8↑ → $\overline{MRAS}$	0		20	ns
$\overline{MCAS}$ output delay	$t_{D:MCAS}$	CLK8↑ → $\overline{MCAS}$	0		15	ns
$\overline{MCAS}$ output high-level pulse width	$t_{WH:MCAS}$	$\overline{MCAS}$ (High)	10			ns
$\overline{MWE}$ output delay	$t_{D:MWE}$	CLK8↑ → $\overline{MWE}$	0		15	ns
$\overline{MWE}$ output low-level pulse width	$t_{WL:MWE}$	$\overline{MWE}$ (Low)	10			ns
$\overline{MOE}$ output delay	$t_{D:MOE}$	CLK8↑ → $\overline{MOE}$	0		15	ns
MAn output delay	$t_{D:MA}$	CLK8↑ → MAn	0		50	ns
MIOn input set-up time	$t_{S:MIO}$	MAX. {MIOn → CLK8↑} + MAX. {$t_{D:MCAS}$, $t_{D:MOE}$ }			15	ns
MIOn input hold time	$t_{H:MIO}$	MAX. {MIOn → CLK8↑ } – MIN. {$t_{D:MOE}$}			0	ns
HW(R)CK output delay	$t_{D:HCK}$	CLK8↑→HWCK,HRCK	0		15	ns
HRST output delay	$t_{D:HRST}$	CLK8↑→HRST	10		40	ns
HI input setup time	$t_{S:HI}$	HIn→HRCK↑			9	ns
HI input hold time	$t_{H:HI}$	HRCK↑→HIn			3	ns
HO output access time	$t_{D:HO}$	HWCK↑→HOn	6		27	ns





Clock and Timing Generation Section AC Characteristics

(DV_{DD} = AV_{DD} = 3.3 ± 0.3 V, DGND = AGND = 0 V, C_L = 15 pF, T_A = –20 to + 70 °C)

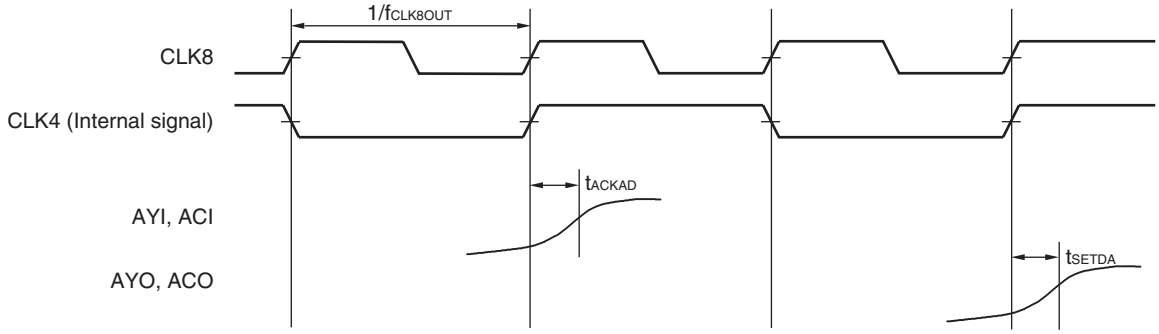
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Subcarrier output frequency	f_{FSCO}	FSCO pin		3.579545		MHz
Subcarrier output amplitude	V_{FSCO}	FSCO pin, AV_{DD} = 3.3 V	1.15	1.30	1.45	V_{p-p}
Clock output frequency	$f_{CLK8OUT}$	CLK8 pin, CKMD pin = DGND,		28.63636		MHz
Clock output duty factor	$D_{CLK8OUT}$	CLK8OFF (SA07:D4) = 0	45	50	55	%
f_{SC} pull-in range (in f_{SC} terms)	f_{bp}	When the burst locked clock operation	±400	±600		Hz
f_H pull-in range (in f_H terms)	f_{hp}	When the line locked clock operation	±400	±500		Hz
Horizontal sync attenuation (Capture range)	V_{hi}	Sync input amplitude, HSSL = 1111, VSSL = 1000	–8	0		dB
Vertical sync attenuation (Capture range)	V_{vi}	(assumed to be 0dB when inputting 40IRE = 59LSB)	–6	0		dB

ADC and DAC Section AC Characteristics (AV_{DD} = 3.3 ± 0.3 V, AGND = 0 V, C_L = 15 pF, T_A = +25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADC acquisition time[Note]	t_{ACKAD}	CLK8↑ → AYI, ACI		7		ns
DAC setting time[Note]	t_{SETDA}	CLK8↑ → AYO, ACO		15		ns

Note Excluding data conversion delay

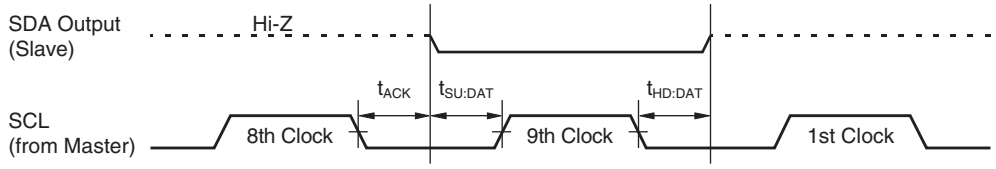
Remark CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 00



I^2C Bus Interface Section AC Characteristics

(DV_{DD} = 3.3 ± 0.3 V, DGND = 0 V, C_L = 15 pF, T_A = –20 to +70 °C)

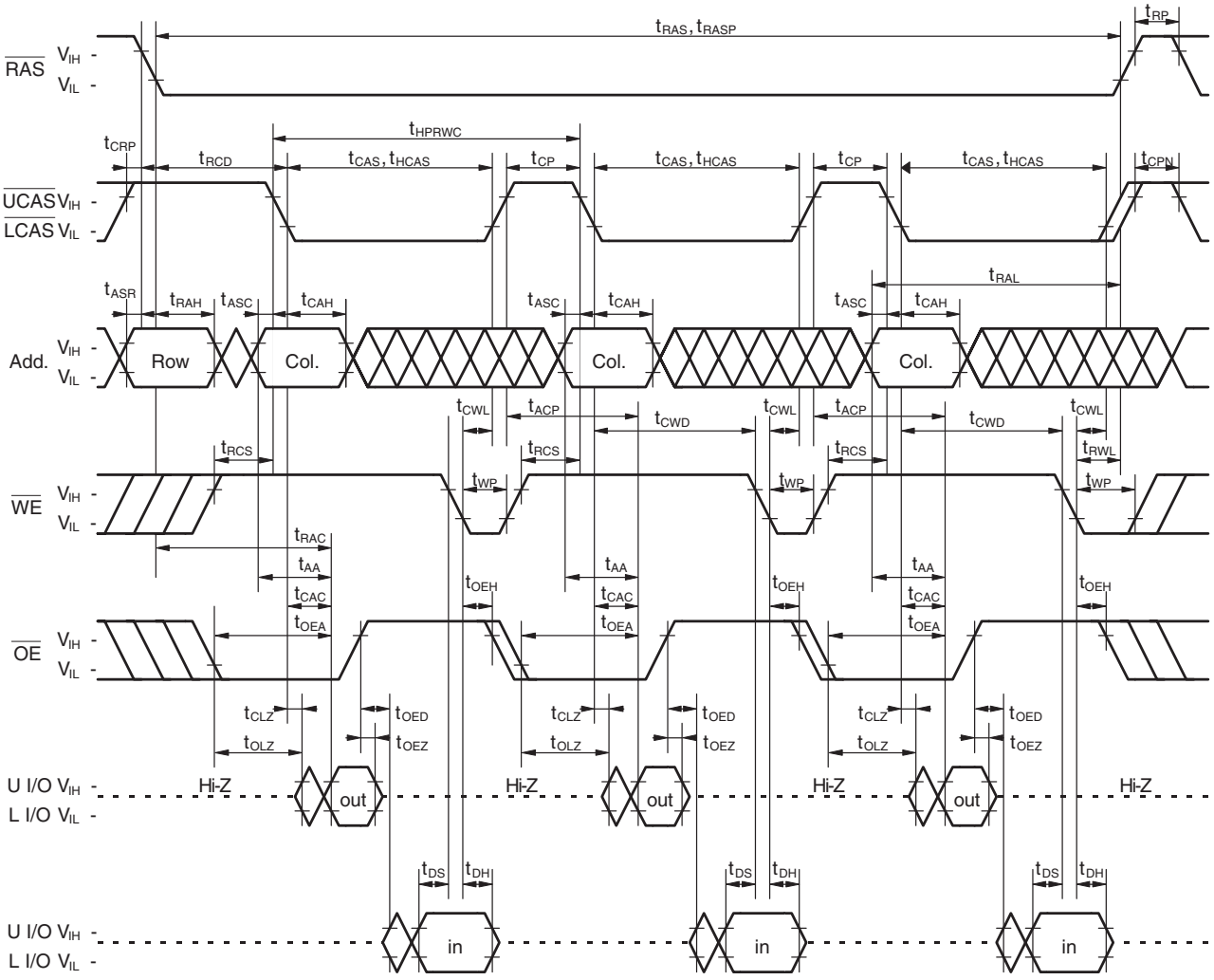
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SDA pin ACK response delay	t_{ACK}	SCL↓ → SDA↓			500	ns
SDA data set-up time	$t_{SU:DAT}$	SDA:L → SCL↑	100			ns
SDA data hold time	$t_{HD:DAT}$	SCL↓ → SDA:Hi-Z	0			ns



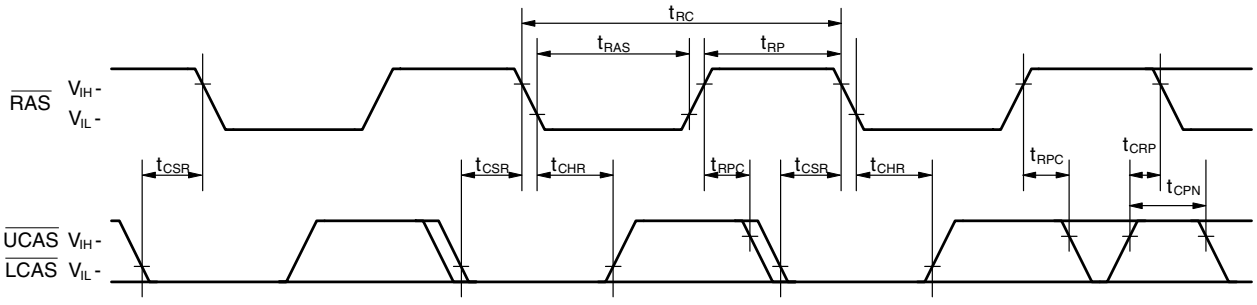
4-Mbit EDO Memory Requirements

Parameter	Symbol	Requirement		Unit
		MIN.	MAX.	
Common to read, write, read modify write cycle				
$\overline{RAS}$ pre-charge time	t_{RP}	70 or less	-	ns
$\overline{CAS}$ pre-charge time	t_{CPN}, t_{CP}	10 or less	-	ns
$\overline{RAS}$ pulse width	t_{RAS}	100 or less	10,000 or more	ns
$\overline{CAS}$ pulse width	t_{CAS}	10 or less	10,000 or more	ns
$\overline{CAS}$ to $\overline{RAS}$ pre-charge time	t_{CRP}	70 or less	-	ns
Row address setup time	t_{ASR}	70 or less	-	ns
Row address hold time	t_{RAH}	70 or less	-	ns
Column address setup time	t_{ASC}	30 or less	-	ns
Column address hold time	t_{CAH}	30 or less	-	ns
$\overline{OE}$ to data delay	t_{OED}	15 or less	-	ns
Refresh cycle	t_{REF}	-	4 or more	ms
Read cycle				
Access time from $\overline{RAS}$	t_{RAC}	-	100 or less	ns
Access time from $\overline{CAS}$	t_{CAC}	-	17 or less	ns
Access time from column address	t_{AA}	-	70 or less	ns
Access time from $\overline{OE}$	t_{OEA}	-	15 or less	ns
Column Address lead time referenced to $\overline{RAS}$	t_{RAL}	70 or less	-	ns
Read command setup time	t_{RCS}	0 or less	-	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0 or more	15 or less	ns
Write cycle				
$\overline{WE}$ pulse width	t_{WP}	10 or less	-	ns
$\overline{WE}$ lead time reference to $\overline{RAS}$	t_{RWL}	70 or less	-	ns
$\overline{WE}$ lead time reference to $\overline{CAS}$	t_{CWL}	10 or less	-	ns
$\overline{OE}$ hold time	t_{OEH}	30 or less	-	ns
Data in setup time	t_{DS}	0 or less	-	ns
Data in hold time	t_{DH}	10 or less	-	ns
Hyper page mode (EDO)				
$\overline{RAS}$ pulse width	t_{RASP}	100 or less	100,000 or more	ns
$\overline{CAS}$ pulse width	t_{HCAS}	10 or less	10,000 or more	ns
Access time from $\overline{CAS}$ pre-charge	t_{ACP}	-	35 or less	ns
★ $\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	70 or less	-	ns
Read modify write cycle time	t_{HPRWC}	100 or less	-	ns
Refresh cycle				
$\overline{CAS}$ setup time	t_{CSR}	70 or less	-	ns
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	70 or less	-	ns
$\overline{RAS}$ pre-charge $\overline{CAS}$ hold time	t_{RPC}	70 or less	-	ns

★ **Hyper Page Mode (EDO) Read Modify Write Cycle**



CAS Before RAS Refresh Cycle



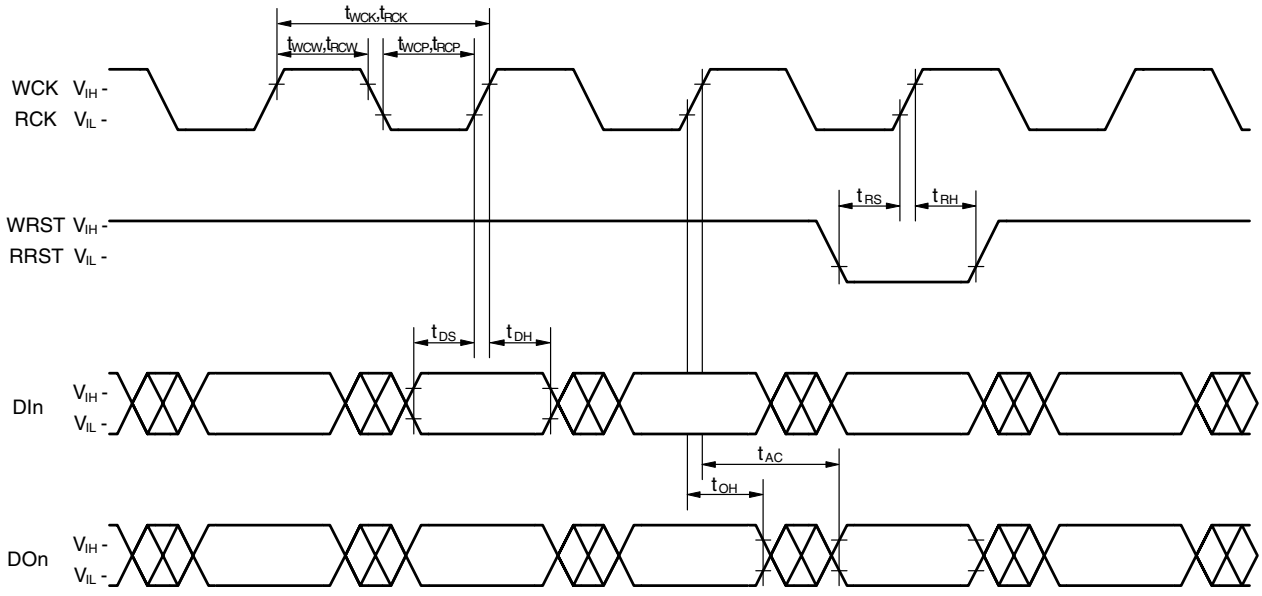
Remark Address, $\overline{WE}$, $\overline{OE}$ = don't care, L I/O, U I/O = high impedance

Caution The above timing chart shows the requirements of the memory only as viewed from this IC.

Field Memory Requirements

Parameter	Symbol	Requirement		Unit
		MIN.	MAX.	
Write clock (WCK) cycle time	t_{WCK}	30 or less	-	ns
Write clock active time	t_{WCW}	12 or less	-	ns
Write clock pre-charge period	t_{WCP}	12 or less	-	ns
Read clock (RCK) cycle time	t_{RCK}	30 or less	-	ns
Read clock active time	t_{RCW}	12 or less	-	ns
Read clock pre-charge period	t_{RCP}	12 or less	-	ns
Access time	t_{AC}		25 or less	ns
Output hold time	t_{OH}	3 or more	-	ns
Input data setup time	t_{DS}	7 or less	-	ns
Input data hold time	t_{DH}	6 or less	-	ns
Reset setup time from WCK or RCK rise	t_{RS}	34 or less	-	ns
Reset hold time from WCK or RCK rise	t_{RH}	34 or less	-	ns
Total of words	-	262,144 or more		word
Bit width	-	4 or more		bit

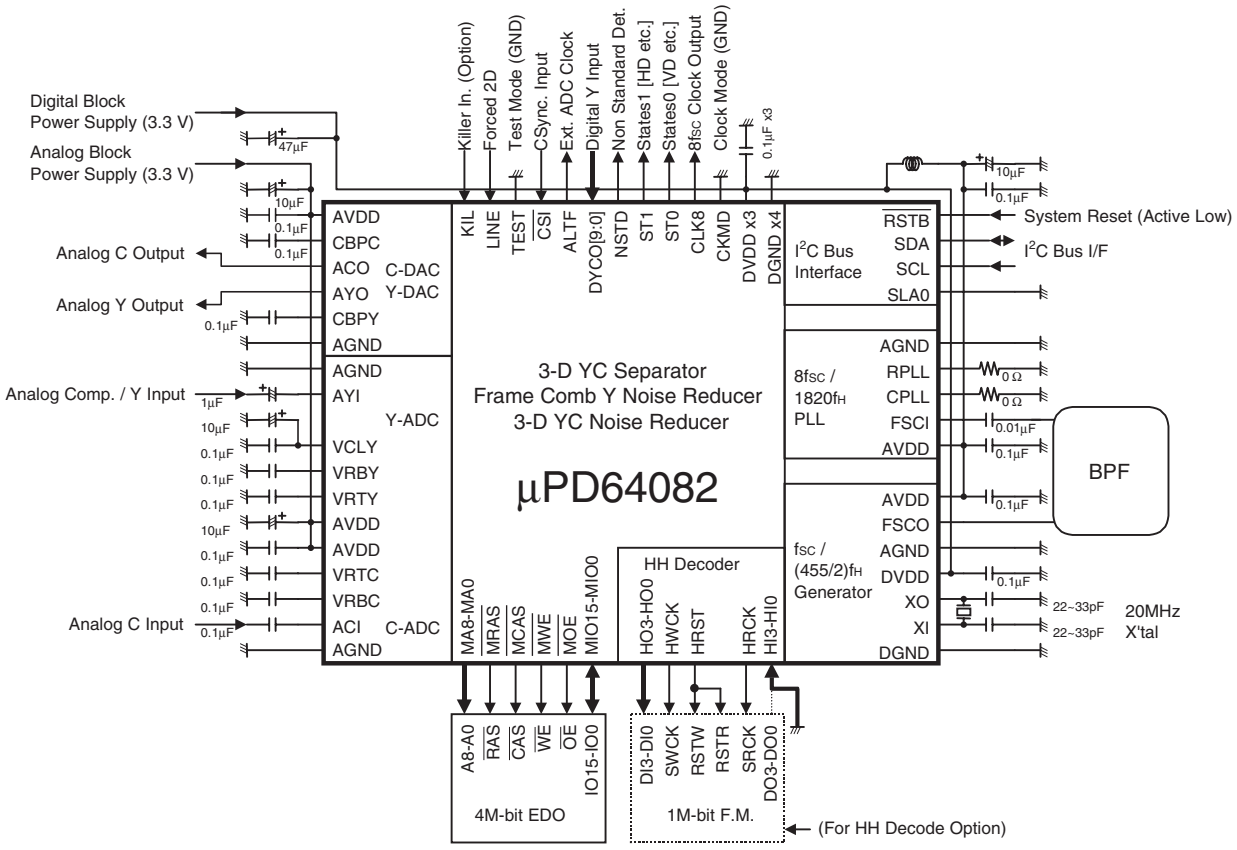
Write/Read Reset Cycle



Remark $\overline{RE}$, $\overline{WE}$, $\overline{OE}$: Low level

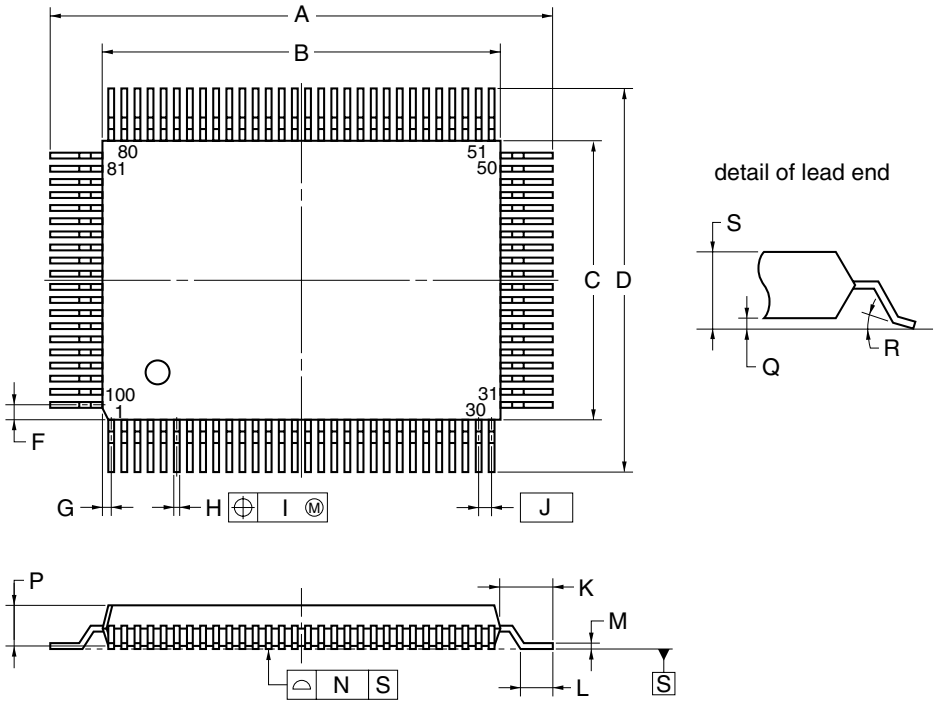
Caution The above timing chart shows the requirements of the field memory only as viewed from this IC.

17. APPLICATION CIRCUIT EXAMPLE



18. PACKAGE DRAWING

100 PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.2±0.2
B	20.0±0.2
C	14.0±0.2
D	17.2±0.2
F	0.8
G	0.6
H	0.32±0.08
I	0.15
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.7
Q	0.125±0.075
R	5°±5°
S	2.825±0.175

S100GF-65-3BA-4

19. RECOMMENDED SOLDERING CONDITIONS

The μPD64082 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 19-1. Surface Mounting Type Soldering Conditions

μPD64082GF-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. Max. (at 210 °C or higher), Count: three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125 °C for 20 hours)	IR35-207-3
VPS	Package peak temperature: 215 °C, Time: 40 sec. Max. (at 200 °C or higher), Count: three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125 °C for 20 hours)	VP15-207-3
Wave soldering	Solder bath temperature: 260 °C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120 °C Max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125 °C for 20 hours)	WS60-207-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	-

Note After opening the dry pack, store it at 25 °C or less and 65 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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