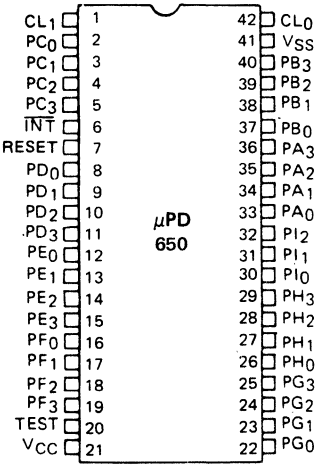
4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD650 is a μCOM-43 4-bit single chip microcomputer manufactured with a low-power-consumption CMOS process, allowing use of a single +5V power supply. The μPD650 provides all of the hardware features of the μCOM-43 family, and executes all 80 instructions of the μCOM-43 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{CC}	Power Supply Positive
V_{SS}	Ground
TEST	Factory Test Pin (Connect to V_{CC})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C
Supply Voltage	-0.3 to +7.0 Volts
Input Voltages (Port A through D, $\overline{INT}$, RESET)	-0.3 to +7.3 Volts
Output Voltages	-0.3 to +7.3 Volts
Output Current (Ports C through I, each bit)	2.5 mA
(Total, all ports)	28mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{CC}		V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Input Voltage Low	V_{IL}	0		0.3 V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Clock Voltage High	$V_{\phi H}$	0.7 V_{CC}		V_{CC}	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	0		0.3 V_{CC}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$ RESET, $V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = 0V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = V_{CC}$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = 0V
Output Voltage High	V_{OH_1}	V_{CC} −0.5			V	Ports C through I, I_{OH} = −1.0 mA
	V_{OH_2}	V_{CC} −2.5			V	Ports C through I, I_{OH} = −2.0 mA
Output Voltage Low	V_{OL_1}			+0.6	V	Ports E through I, I_{OL} = +2.0 mA
	V_{OL_2}			+0.4	V	Ports E through I, I_{OL} = +1.2 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C, D, V_O = 0V
Supply Current	I_{CC}		+0.8	+2.0	mA	

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5 ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μS	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μS	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μS	

CLOCK WAVEFORM