

The electrical characteristics of a particular gate array design are determined after evaluation of samples. This section describes the standard characteristics by a series of tables and graphs.

Tables

Exposure to the absolute maximum ratings in table 5-1 for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The gate array device should not be operated under conditions outside those recommended in table 5-2. The input signal specifications depend on whether the interface is with a CMOS-level or TTL-level device.

Tables 5-3 and 5-4 show dc characteristics and ac characteristics. Some of these signal specifications are dependent on an external CMOS or TTL interface, also. If all input and output signals interface with CMOS-level devices, the supply voltage and ambient temperature limits of the gate array chip are:

$$V_{DD} = 5.0 \text{ volts} \pm 10\%$$

$$T_A = -40 \text{ to } +85^\circ\text{C}$$

If one or more of the signals interface with TTL-level devices:

$$V_{DD} = 5.0 \text{ volts} \pm 5\%$$

$$T_A = -40 \text{ to } +85^\circ\text{C}$$

Table 5-5 lists the maximum internal capacitance that you may expect at the signal ports of the gate array chip.

Table 5-1. Absolute Maximum Ratings

$T_A = +25^\circ\text{C}$

Power supply voltage, V_{DD}	-0.5 to +7.0 V
Input voltage, V_I	-0.5 V to $V_{DD} + 0.5$ V
Input current, I_I	40 mA
Output current, I_O	40 mA
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Table 5-2. Recommended Operating Conditions

Parameter	Symbol	CMOS Level		TTL Level		Unit
		Min	Max	Min	Max	
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	V
Ambient temperature	T_A	-40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.0	V_{DD}	V
Input rise or fall time (1)	t_R, t_F	0	10	0	10	μs
Positive Schmitt trigger voltage (2)	V_P	1.8	4.0	1.2	2.3	V
Negative Schmitt trigger voltage (2)	V_N	0.6	3.1	0.6	1.8	V
Hysteresis voltage (2)	V_H	0.3	1.5	0.3	1.5	V

Note:

(1) For Schmitt trigger input buffers.

(2) $V_{DD} = 5.0$ V

Table 5-3. DC Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$; $T_A = -40\text{ to }+85^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Static current (Note 1)	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Input current						
With pull-up	I_I	25	80	250	μA	$V_I = \text{GND}$
With pull-down	I_I	25	80	250	μA	$V_I = V_{DD}$
Without resistor (Note 1)	I_I		10^{-5}	10	μA	$V_I = V_{DD}$ or GND
Dynamic current	I_{DD}		3		μA	Per cell at 1 MHz
Off-state output leakage current	I_{OZ}			10	μA	$V_O = V_{DD}$ or GND
Low-level output current (Note 2)						
Buffer F001 (Note 3)	I_{OL}	4.0 (4.3)	11		mA	$V_{OL} = 0.4\text{ V}$
Buffer F002	I_{OL}	5.6 (6.0)	15		mA	
Buffer F003 (Note 4)	I_{OL}	12 (13)	15		mA	
High-level output current (Note 2)						
Buffer F001 (Note 3)	I_{OH}	4.0 (4.3)	8		mA	$V_{OH} = V_{DD} - 0.4\text{ V}$
Buffer F002	I_{OH}	5.6 (6.0)	11		mA	
Buffer F003 (Note 4)	I_{OH}	12 (13)	11		mA	
Low-level output voltage	V_{OL}			0.1	V	$I_O = 0\text{ mA}$
High-level output voltage	V_{OH}	$V_{DD} - 0.1$			V	

Note:

- (1) Not applicable to blocks with a pull-up or pull-down resistor or to oscillator blocks.
- (2) Current values in parentheses are for TTL level interface. $V_{DD} = 5\text{ V} \pm 5\%$ and $T_A = -40\text{ to }+85^\circ\text{C}$.
- (3) Current values for FO01 are applicable to these low-drive output buffers:
B003, B004, B008
B0D3, B0D4, B0D8
B0U3, B0U4, B0U8
EXT1, EXT2, EXT3, EXT4
- (4) Current values for FO03 are applicable to these high-drive output buffers:
B005, B006, B009
B0D5, B0D6, B0D9
B0U5, B0U6, B0U9
EXT5, EXT6, EXT7, EXT8

Table 5-4. AC Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$; $T_A = -40\text{ to }+85^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Max operating frequency (Note 1)	$f_{\max}$			70 (75)	MHz	Internal toggle; $F/O = 1$
Delay time, internal gate	t_{PD}		1.4		ns	$F/O = 3$; $L = 3\text{ mm}$
Delay time, input buffer	t_{PD}		2.0		ns	
Delay time, output buffer	t_{PD}		4.0		ns	$C_L = 15\text{ pF}$
Output rise time	t_R		3.2		ns	
Output fall time	t_F		2.2		ns	

Note:

- (1) Frequency in parentheses is for TTL level interface. $V_{DD} = 5\text{ V} \pm 5\%$ and $T_A = -40\text{ to }+85^\circ\text{C}$.

Table 5-5. Input/Output Capacitance

Terminal	Symbol	Limits		Unit	Test Conditions
		Typ	Max		
Input	C_{IN}		10	pF	$V_{DD} = V_I = 0\text{ V}$; $f = 1\text{ MHz}$
Output	C_{OUT}		30	pF	
I/O	$C_{I/O}$		35	pF	

Graphs

Figures 5-1 through 5-5 are graphs depicting the operating characteristics.

Figure	Description
5-1	Input buffers (V_O vs V_I)
5-2	Input buffers (V_I vs V_{DD})
5-3	Input buffers (V_I vs T_A)
5-4	Internal gate delay time
5-5	Output buffers (also see Section 4)

Figure 5-1. Input Buffers; Output Voltage vs Input Voltage

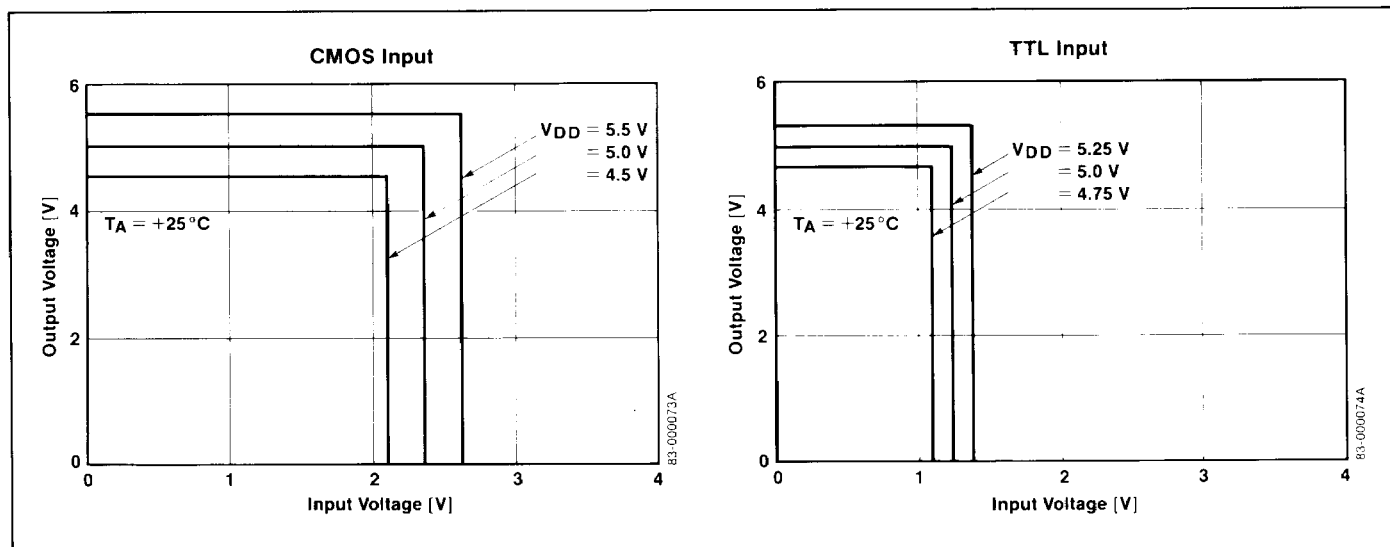


Figure 5-2. Input Buffers; Threshold Voltage vs Supply Voltage

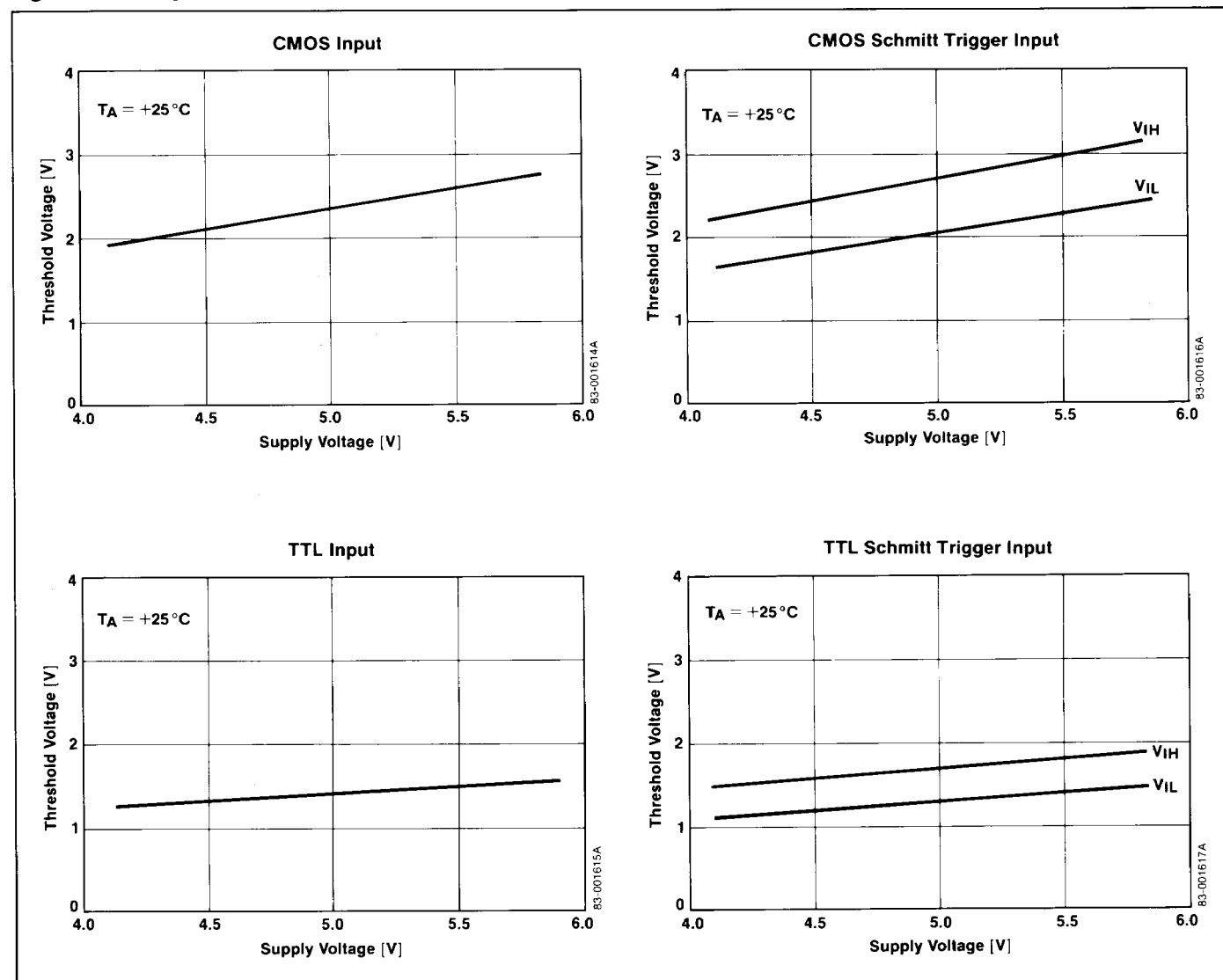


Figure 5-3. Input Buffers; Threshold Voltage vs Ambient Temperature

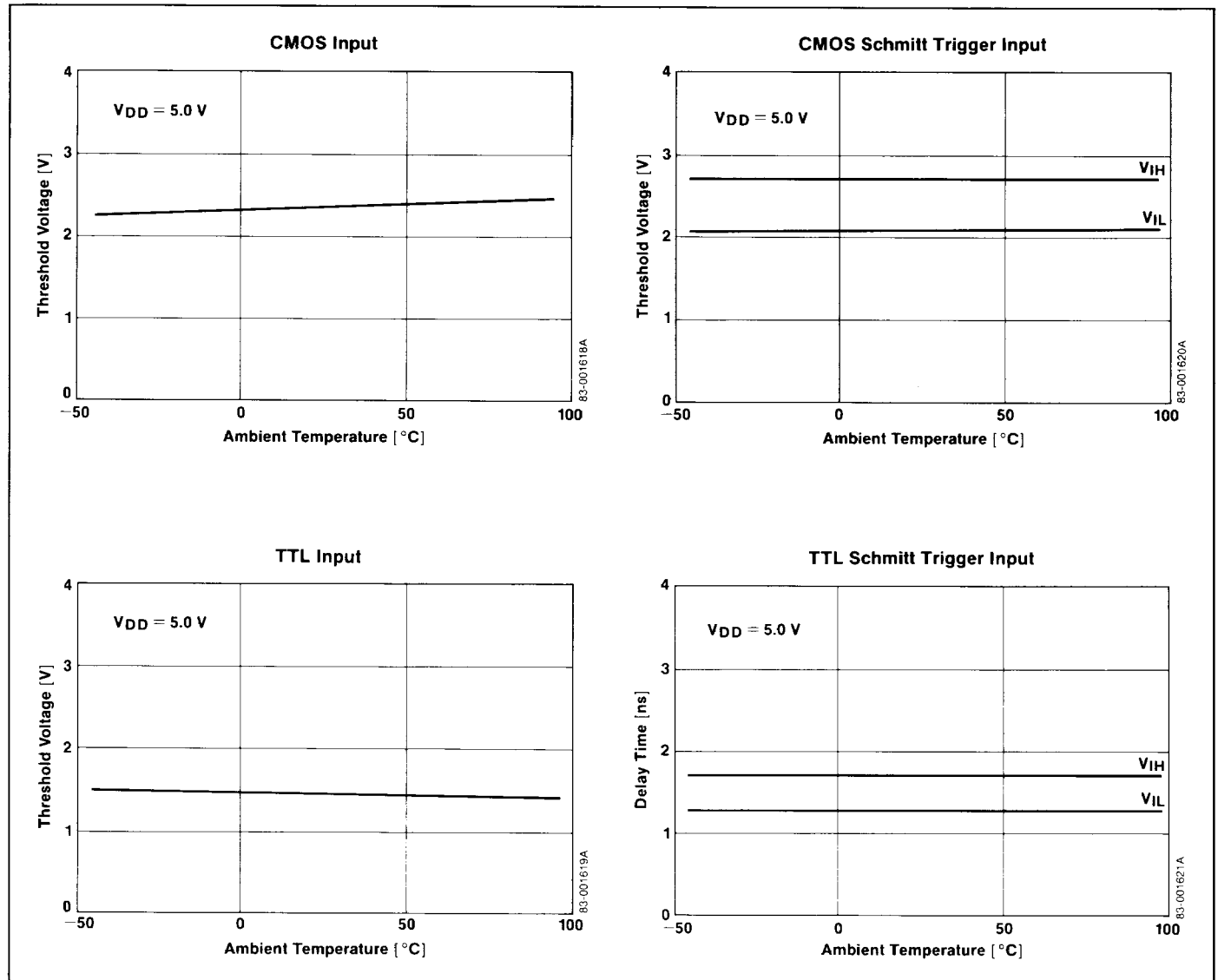


Figure 5-4. Internal Gate Delay Time

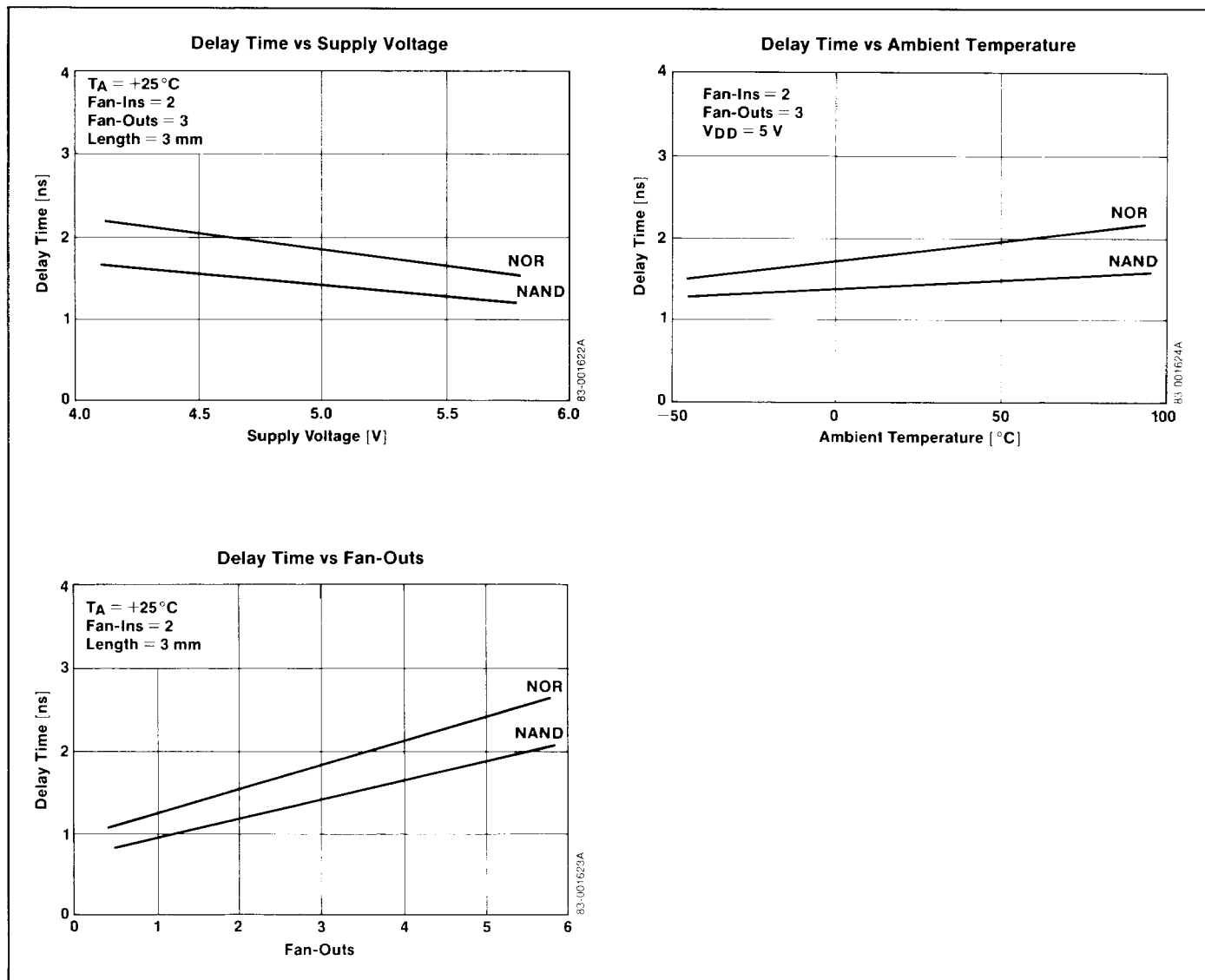


Figure 5-5. Output Buffers (FO01); Output Current vs Output Voltage

