NEC
ELECTRON DEVICE

MOS DIGITAL INTEGRATED CIRCUIT
μPD6529C

AUTOMOTIVE CLOCK
CMOS LSI

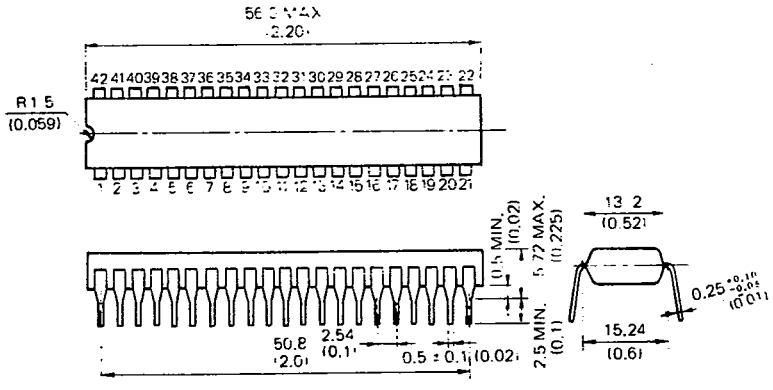
GENERAL DESCRIPTION

The μPD6529C is a monolithic CMOS LSI for crystal controlled automative clocks. The circuits interface directly with fluorescent indicator panel. The display format is 12 hours. It is also provided with a 4-ways display brightness control function and can be driven by an external clock signal.

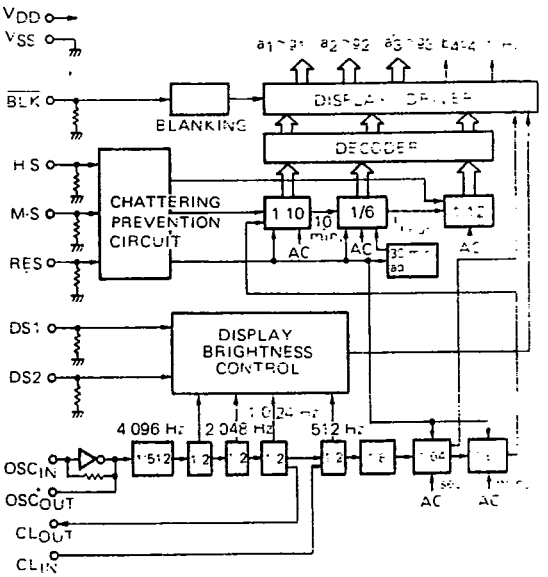
FEATURES

- Crystal controlled oscillator (4.194 304 MHz)
- Direct interface to fluorescent indicator panel (FIP4E8S)
- 12 hours display format
- 4-ways display brightness control (duty controlled dimmer 1, 1/4, 1/8, 1/16)
- External clock drive possible (1 024 Hz)
- Separated hours and minutes set controls (2 Hz)
- On the hour adjustment control (±30minutes)
- 1 024 Hz output
- 42 Pin DIP mold

PACKAGE DIMENSIONS
in millimeters (inches)



BLOCK DIAGRAM



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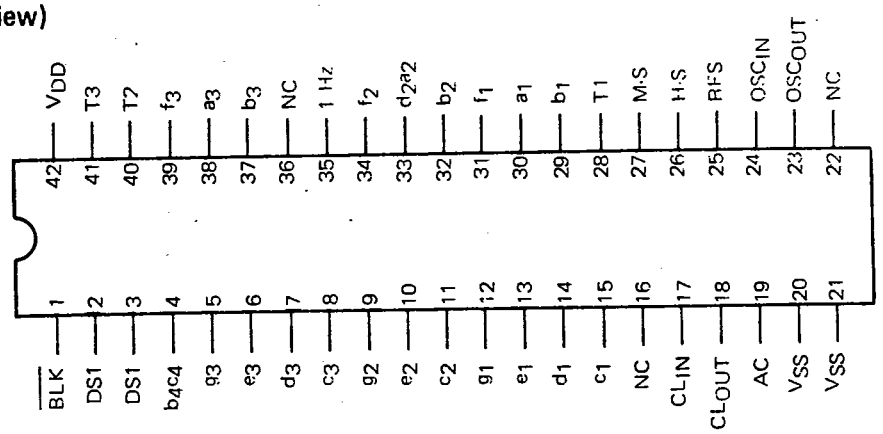
CONNECTION DIAGRAM
(Top View)



PIN NO.	SYMBOL INPUT	SYMBOL OUTPUT	PIN NAME	INTERNAL STATE
1	$\overline{BLK}$		Blanking input	Pull down
2	DS1		Dimmer input 1	
3	DS2		Dimmer input 2	
4		b_4c_4	Segment output	P-ch Open Drain
5		g_3		
6		e_3		
7		d_3		
8		c_3		
9		g_2		
10		e_2		
11		c_2		
12		g_1		
13		e_1		
14		d_1		
15		c_1		
16	NC			
17	CL_{IN}		Ex. Clock input	
18		CL_{OUT}	Clock output	
19	AC		Clear input	Pull down
20	V_{SS}		–Power supply	
21	V_{SS}			

PIN NO.	SYMBOL INPUT	SYMBOL OUTPUT	PIN NAME	INTERNAL STATE
22	NC			
23		OSC_{OUT}	OSC output	
24	OSC_{IN}		OSC input	
25	RES		RES input	Pull down
26	H·S		Hour adj. input	
27	M·S		Minute adj. input	
28	T1		Test pin 1	
29		b_1	Segment output	P-ch Open Drain
30		a_1		
31		f_1		
32		b_2		
33		$d_2{\cdot}a_2$		
34		f_2		
35		1 Hz	1 Hz signal	
36	NC			
37		b_3	Segment output	P-ch Open Drain
38		a_3		
39		f_3		
40	T2		Test pin 2	
41	T3		Test pin 3	
42		V_{DD}	+Power supply	

ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Power supply voltage	$V_{DD}-V_{SS}$	−0.3	to	+8.0	V
Input voltage	V_{IN}	V_{SS}−0.3	to	V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{DD}−20	to	V_{DD}+0.3	V
Operating temperature	T_{opt}	−40	to	+85	°C
Storage temperature	T_{stg}	−55	to	+125	°C

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	$V_{DD}-V_{SS}$	3.0	–	7.0	V
High Level Input Voltage	V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Low Level Input Voltage	V_{IL}	V_{SS}	–	0.3 V_{DD}	V
External Clock Duty	CL_D	40	50	60	%

ELECTRICAL CHARACTERISTICS 1 (Unless otherwise noted $V_{DD}-V_{SS}$=6.0 V, T_a=25 °C, RH≤70 %, C_D=C_G=15 pF, Xtal=4.194 304 MHz)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I_{DD}	No output loads	–	–	1	mA
High Level Output Current 1, Note 1	$\|I_{OH1}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	300	–	–	μA
High Level Output Current 2, Note 2	$\|I_{OH2}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	500	–	–	μA
AC Response Time	T_{AC}	$V_{DD}-V_{SS}$=3.0~7.0 V V_{IN}=0.7 V_{DD}~V_{DD}	–	–	100	μS
Low Level Output Current, Note 3	I_{OL}	$V_{DD}-V_{SS}$=3.0 V, $V_{OUT}-V_{SS}$=0.5 V	500	–	–	μA
High Level Input Current 1, Note 4	I_{IH1}	V_{IN}=V_{DD}	–	15	30	μA
High Level Input Current 2, Note 5	I_{IH2}	V_{IN}=V_{DD}	–	120	600	μA
Low Level Input Current	$\|I_{IL}\|$	V_{IN}=V_{SS}	–	–	50	μA
External Clock Duty	C_{LD}		40	50	60	%

ELECTRICAL CHARACTERISTICS 2 (Unless otherwise noted $V_{DD}-V_{SS}$=3.0 to 7.0 V, T_a=−40 to +85 °C, RH≤70 %, C_D=C_G=15 pF, Xtal=4.194 304 MHz)

CHARACTERISTIC	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I_{DD}	No output loads	–	–	2	mA
High Level Output Current 1, Note 1	$\|I_{OH1}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	250	–	–	μA
High Level Output Current 1, Note 2	$\|I_{OH2}\|$	$V_{DD}-V_{SS}$=3.0 V, $V_{DD}-V_{OUT}$=0.5 V	400	–	–	μA

Note 1) for segments other than those specified in Note 2

Note 2) for segments b4C4 and a2d2, 1 Hz and CL_{OUT}

Note 3) for CL_{OUT}

Note 4) for DS1, DS2, RES, H·S, M·S, and $\overline{BLK}$

Note 5) for T1, T2, T3 and AC

INTERFACE SIGNAL DESCRIPTION

[1] H·S input (pin 26)

Put this pin (26) to High Level (V_{DD}) and the Hour counter is fast fed at 2 Hz. No counting up from Minutes to Hours is provided.

[2] M·S input (pin 27)

Put this pin (27) to High Level (V_{DD}) and the Minutes counter is fast fed at 2 Hz. No counting up from Seconds to Minutes is provided.

[3] RES input (pin 25)

Put this pin (25) to High Level (V_{DD}) and the adjustment to a right o'clock is made within ±30 minutes range, as shown below.

① XX o'clock 00 minute 00 second → RES → XX o'clock 00 minute 00 second
XX o'clock 29 minutes 59 seconds

② XX o'clock 30 minutes 00 second → RES → (XX+1) o'clock 00 minute 00 second
XX o'clock 59 minutes 59 seconds

[4] $\overline{BLK}$ input (pin 1)

Put this pin (25) to Low Level (open) and the display outputs are turned off (Blanking).

During Blanking, H·S, M·S and RES inputs are ineffective.

Return this pin to High Level and the display outputs are recovered.

[5] DS1 input (pin 2) and DS 2 input (pin 3)

Combine DS1 and DS2 as shwn below and the display brightness is dimmed accordingly.

DS2	DS1	Output ON Duty Ratio	Clock Mode
L	L	1	Internal, External
L	H	1/4	↓
H	L	1/8	
H	H	1/16	

Dimmer Freqency : 512 Hz

- Internal Clock Mode
  4.194 304 MHz crystal oscillator is used.
- External Clock Mode
  1 024 Hz signal is input to CL_{IN} pin.

[6] AC input (pin 19)

Put this pin to High Level (V_{DD}) and this IC is reset to display 1 o'clock 00 minute (00 second).

[7] CL_{IN} input (pin 17)

When this IC is to be driven by a crystal oscillator, put this pin to Low Level (V_{SS}).

When this IC is to be driven by an external clock, input a 1 024 Hz signal voltage within the specified input voltage range.

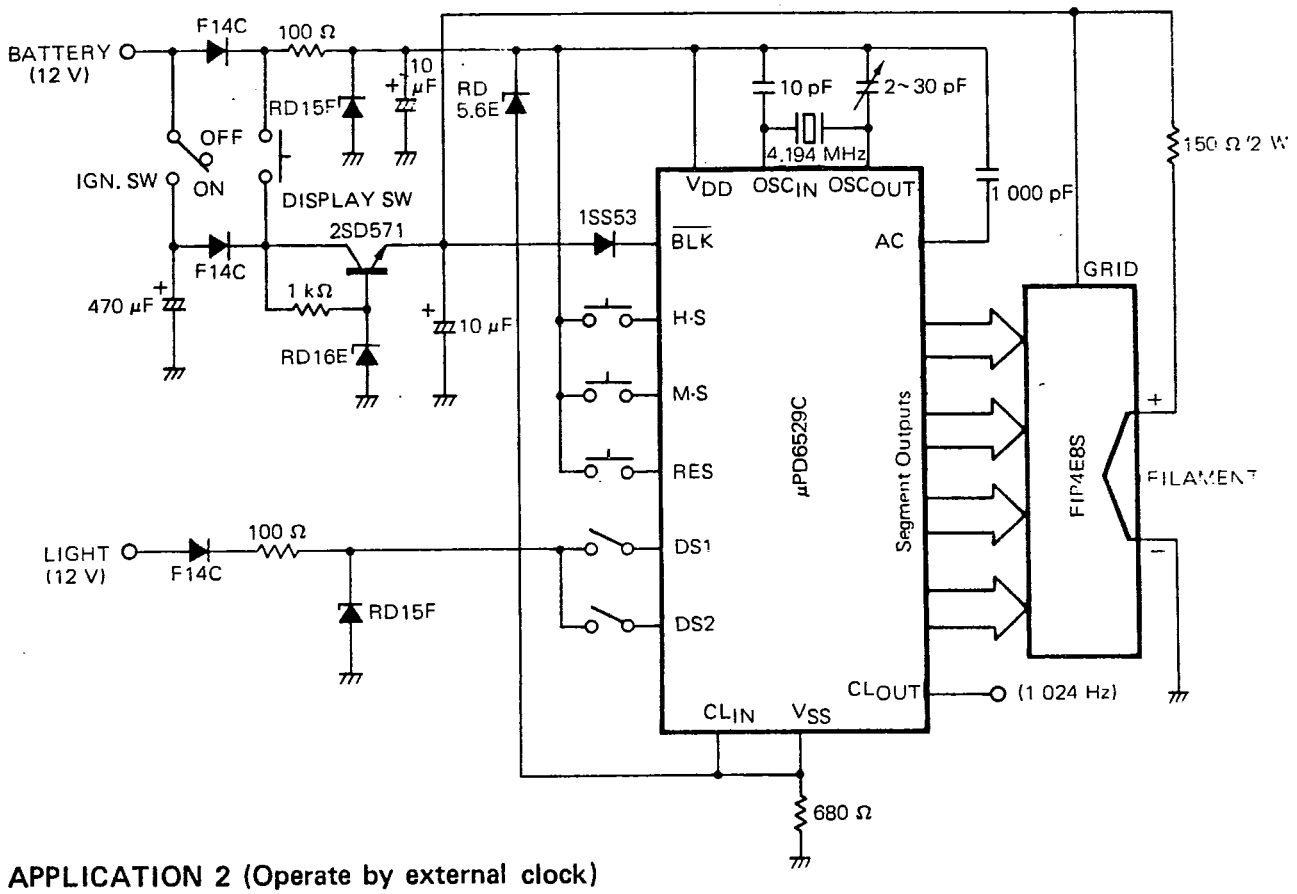
[8] CL_{OUT} output (pin 18)

A 1 024 Hz signal with 50 % duty is output on this pin (as a CMOS output). When this IC is operated on an external clock, this output is suppressed.

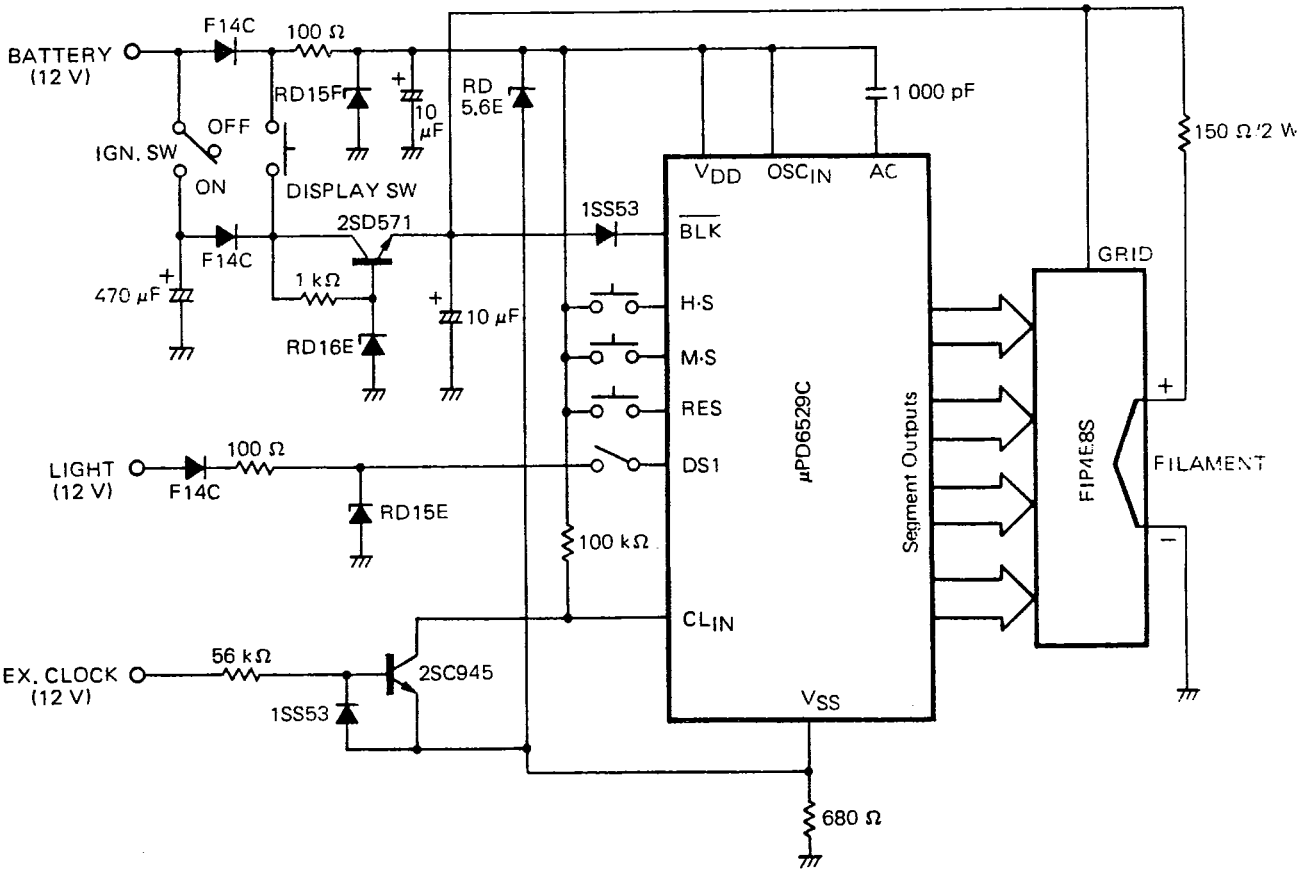
[9] T1 (pin 28), T2 (pin 40) and T3 (pin 41)

These pins are provided for the LSI testing and should be kept on Low Level (V_{SS}) during operation.

APPLICATION 1



APPLICATION 2 (Operate by external clock)



NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

The application circuits above shown are not intended to give any mass production design that needs deliberate considerations on possible deviations and thermal dependencies of component parts characteristics.

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