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NEC Electronics Inc.

CMOS-6/6A/6V/6X 1.0-MICRON CMOS GATE ARRAYS

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Description

NEC's CMOS-6 gate array families (CMOS-6, CMOS-6A, CMOS-6V and CMOS-6X) are high performance, sub-micron effective channel length CMOS products created for high-integration ASIC applications.

The device processing includes 1.0-micron (drawn) silicon-gate CMOS technology and three-layer (CMOS-6) and two-layer (CMOS-6A, CMOS-6V, CMOS-6X) metallization. This technology features channelless (sea-of-gates) architecture in densities from 2,244 to 177,408 available gates, with an internal gate delay of 270 ps (F/O=1; L=0). Output drive is variable to 24 mA. Slew-rate buffers are also available.

CMOS-6 products are fully supported by NEC's advanced ASIC design technology. NEC's OpenCAD® integration system lets the designer choose the most powerful design tools and services available.

NEC offers advanced packaging solutions including TQFP, PQFP and CPGA. These heat-sink-equipped packages give CMOS-6 devices the performance edge in high-integration applications.

Features

- ❑ Channelless, 1.0 µm CMOS high-density architecture
- ❑ Variable output drive: 4.5, 9.0, 13.5, 18.0, or 24 mA
- ❑ Slew-rate output buffers
- ❑ Free size memory blocks to 64 Kbytes
- ❑ Powerful block library with more than 400 macros
- ❑ 3.3V characterized block library
- ❑ High I/O to gate ratio for CMOS-6V and CMOS-6X
- ❑ Compatible with CMOS-5 Block Library
- ❑ Designs may be migrated to NEC's 0.6-micron CMOS-8 and Universal PCI families and to the 0.5-micron CMOS-8L and CMOS-8LCX families
- ❑ TQFP packaging available

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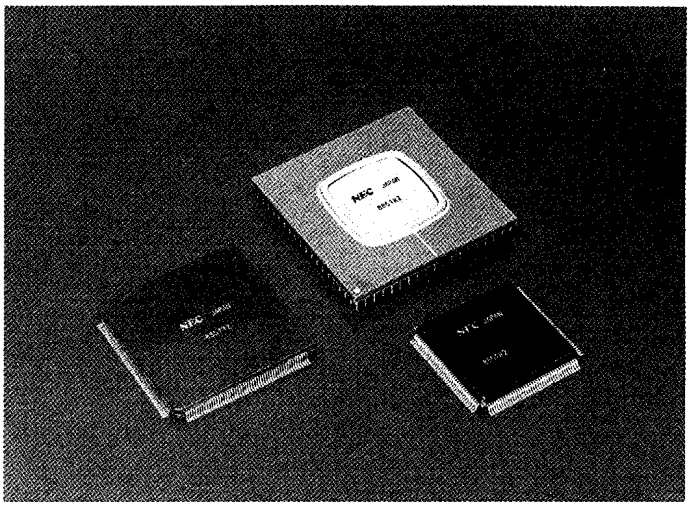
Figure 1. Sample CMOS-6/6A/6V/6X Packages



Gate Array Sizes

Device (µPD)	Raw Gates	Est. Usable Gates All Random*	Max. I/O	Total Pads
CMOS-6X Devices (2-layer metal)				
65612	2,244	1,571	64	80
65622	4,260	2,982	84	100
65626	5,760	4,032	104	120
65632	8,148	5,704	104	120
CMOS-6A Devices (2-layer metal)				
65630	5,376	3,800	84	100
65636	8,000	5,600	100	116
65640	11,520	8,100	120	136
65646	16,240	11,400	140	156
65650	21,120	14,800	160	176
65654	30,720	21,500	192	208
65656	40,500	28,300	188	220
65662	70,300	49,100	252	288
CMOS-6V Devices (2-layer metal)				
65631	5,544	3,900	140	156
65641	11,520	8,100	160	176
65644	14,040	9,800	160	176
65647	16,240	11,400	160	176
65648	18,600	13,000	160	176
65651	21,120	14,800	220	236
65652	26,640	18,600	220	236
65655	30,720	21,500	220	236
CMOS-6 Devices (3-layer metal)				
65658	42,240	31,700	220	236
65664	72,576	54,400	288	304
65672	119,232	89,400	368	384
65676	177,408	133,100	448	464

Notes: Actual gate utilitization may vary depending on circuit implementation. Representative utilization is 75% for three-layer metal; 70% for two-layer metal. Depending on package and circuit specification, some pads

Circuit Architecture

CMOS-6 products are built with NEC's 1-micron channelless architecture. As shown in figure 2, CMOS gate array chips are divided into I/O and internal core areas. The I/O cell area contains input and output buffers that isolate the internal core from high-energy external signals. The internal core area is an array of basic gates, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design. These p-channel and n-channel transistors are sized to offer a superb ratio of speed to silicon area.

Note: One cell equals one logic gate (2-input NAND). See figure 3.

Figure 2. Chip Layout and Internal Gate Configuration

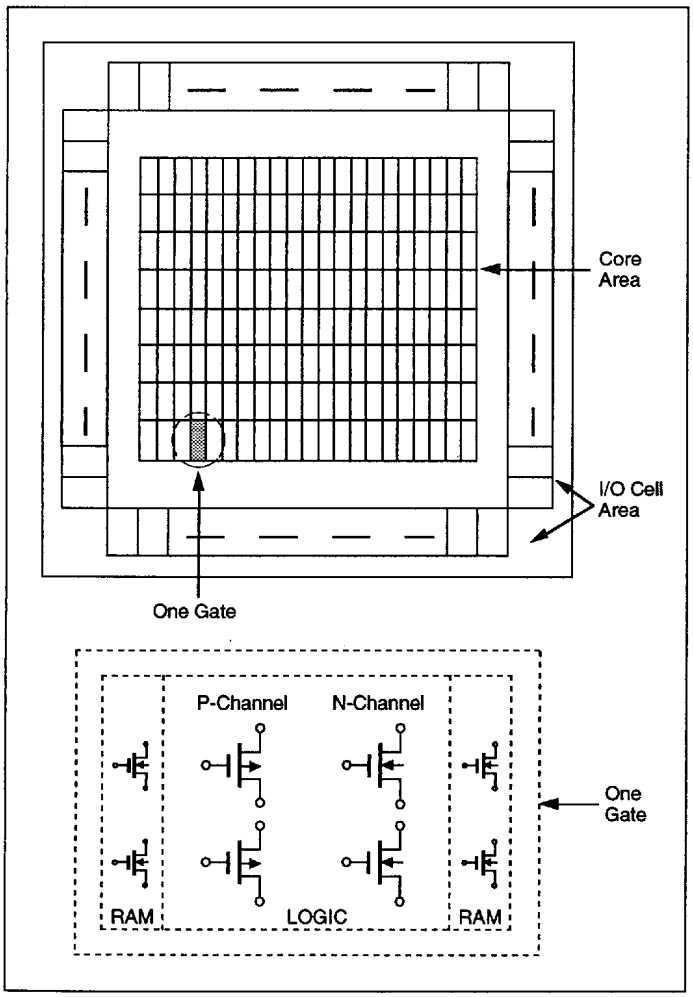
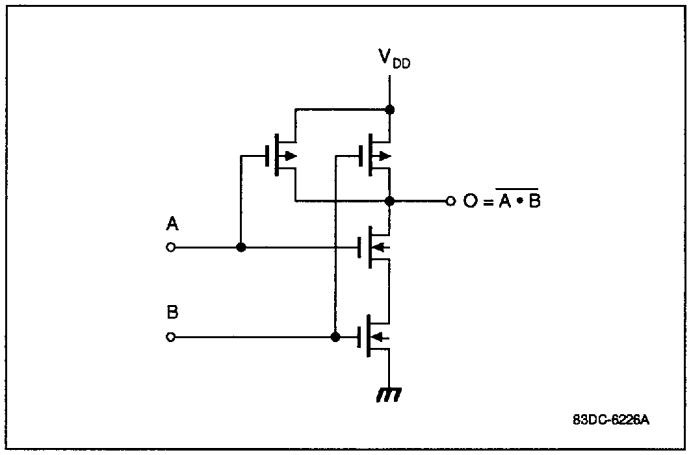


Figure 3. Gate Configured as a 2-Input NAND (L302)



Output Slew-Rate Selection

Fast rise and fall times of CMOS output buffers can cause system noise and signal overshoot. When an unterminated line is being driven by a buffer, the maximum line length is determined by the rise and fall time of the output buffers and the round-trip signal delay of the line.

As a general rule, the round-trip delay of the line should not exceed the rise or fall time of the driving signal. Transmission lines that are longer than those determined by the above rule can cause system performance degradation because of reflections and ringing. One benefit of slew-rate output buffers is that longer interconnections on a PC board (and routing flexibility) are possible with slew-rate output buffers.

The ASIC designer can slow down the output edge rate by selecting the slew-rate output buffer and thus allowing for a longer line.

Also, as the slew-rate buffers inject less noise than their non-slew-rate counterparts into the internal power and ground busses of the devices, the slew-rate buffers require fewer power pairs for simultaneous switching outputs.

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CMOS-6 gate array families. Additional design information is available in NEC's CMOS-6/6A/6V/6X Block Library and CMOS-6/6A/6V/6X Design Manual. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +6.5 V
Input/output voltage, V_I / V_O	–0.5 V to V_{DD} + 0.5 V
Latch-up current, I_{LATCH}	>1 A (typ)
Output current, I_O	
4.5-mA drive	10 mA
9-mA drive	20 mA
13.5-mA drive	30 mA
18-mA drive	40 mA
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz, T_A = +25°C

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note:

(1) Values include package pin capacitance.

Power Consumption

Description	Limits (max)	Unit	Test Conditions
Internal cell	8	µW/MHz	F/O = 3; L = 3 mm
Input block	46	µW/MHz	F/O = 3; L = 3 mm
Output block	980	µW/MHz	C_L = 15 pF

Recommended Operating Conditions

		CMOS Level		TTL Level		
Parameter	Symbol	Min	Max	Min	Max	Unit
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	V
Ambient temperature	T_A	–40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.2	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	ms
Positive Schmitt-trigger voltage	V_P	1.8	4.0	1.2	2.4	V
Negative Schmitt-trigger voltage	V_N	0.6	3.1	0.6	1.8	V
Hysteresis voltage	V_H	0.3	1.5	0.3	1.5	V

AC Characteristics

V_{DD} = 5 V ± 10%; T_A = –40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	120			MHz	D-F/F; F/O = 2
Delay time, 2-input NAND gate						
Standard gate (F302)	t_{PD}		310		ps	F/O = 1; L = 0 mm
			460		ps	F/O = 2; L = 0.5 mm
Power gate (F322)	t_{PD}		280		ps	F/O = 1; L = 0 mm
			355		ps	F/O = 2; L = 0.5 mm
Delay time, buffer						
Input (FI01)	t_{PD}		841		ps	F/O = 2; L = 0.5 mm
Output (FO01)	t_{PD}		3.92		ns	C_L = 15 pF
Output rise time	t_R		1.54		ns	C_L = 15 pF
Output fall time	t_F		1.42		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 5 V ± 10%; T_A = −40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (1)	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Input leakage current						
Regular	I_I		10^{-5}	±10	μA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	−45	−131	−320	μA	V_I = GND
5 kΩ pull-up	I_I	−0.35	−1.0	−2.2	mA	V_I = GND
50 kΩ pull-down	I_I	45	131	320	μA	$V_I = V_{DD}$
Off-state output leakage current	I_{OZ}			±10	μA	$V_O = V_{DD}$ or GND
Input clamp voltage (5)	V_{IC}	−1.2			V	I_I = −18 mA
Output short circuit current (2)	I_{OS}			−250	mA	V_O = 0 V
Low-level output current (CMOS) (3)						
4.5 mA	I_{OL}	4.5			mA	V_{OL} = 0.4 V
9 mA	I_{OL}	9.0			mA	V_{OL} = 0.4 V
13.5 mA	I_{OL}	13.5			mA	V_{OL} = 0.4 V
18 mA	I_{OL}	18.0			mA	V_{OL} = 0.4 V
24 mA	I_{OL}	24.0			mA	V_{OL} = 0.4 V
High-level output current (CMOS) (3)						
4.5 mA	I_{OH}	−2.5			mA	$V_{OH} = V_{DD}$ −0.4 V
9 mA	I_{OH}	−5.0			mA	$V_{OH} = V_{DD}$ −0.4 V
13.5 mA	I_{OH}	−7.5			mA	$V_{OH} = V_{DD}$ −0.4 V
18 mA	I_{OH}	−10.0			mA	$V_{OH} = V_{DD}$ −0.4 V
24 mA	I_{OH}	−14.0			mA	$V_{OH} = V_{DD}$ −0.4 V
Low-level output current (TTL) (4)						
9 mA	I_{OL}	9.0			mA	V_{OL} = 0.4 V
18 mA	I_{OL}	18.0			mA	V_{OL} = 0.4 V
High-level output current (TTL) (4)						
9 mA	I_{OH}	−0.5			mA	V_{OH} = 2.4 V
18 mA	I_{OH}	−1.0			mA	V_{OH} = 2.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage (CMOS) (3)	V_{OH}	V_{DD}−0.1			V	I_{OH} = 0 mA
High-level output voltage (TTL) (4)	V_{OH}	2.6	3.4		V	I_{OH} = 0 mA

Notes:

(1) The maximum value reflects the use of pull-up/pull-down resistors and oscillator blocks. Contact an NEC ASIC Design Center for assistance in calculation.

(2) Rating is for only one output operating in this mode for less than 1 second.

(3) CMOS-level output buffer (V_{DD} = 5 V ± 10%, T_A = −40 to +85°C).

(4) TTL-level output buffer (V_{DD} = 5 V ± 5%, T_A = 0 to +70°C).

(5) The input clamp voltage is voltage clamped when an input signal is at negative voltage. Input signal undershoot or ringing is clamped at this voltage.

NEC's ASIC Design System

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time-to-market. Designers can combine today's most popular third-party software tools with proprietary NEC tools to maximize design quality and minimize design time.

NEC's OpenCAD® Design System is a front-end to back-end ASIC design package that merges several advanced CAE/CAD tools into a single structure. Designers can now choose a single CAE platform, or mix and match tools from a variety of third-party vendors.

The design flow combines tools for floorplanning, logic synthesis, automatic test generation, accelerated fault-grading, full-timing simulation, and advanced place-and-route algorithms. This flexible design environment thereby ensures accurate, on schedule ASICs.

A top-down modeling methodology is possible using the HDL specification approach. Designers can concentrate their design effort at a higher level of abstraction, specifying, modeling, and simulating their designs at a systems level. This leaves the details of the gate-level implementation to the synthesis tools.

After verification confirms the design's functionality, designers are then free to explore various functional and architectural trade-offs, and can optimize chip performance while minimizing chip area. An engineer can evaluate several architectures and select the best solution before committing the design to silicon.

One of the key benefits of NEC's ASIC design flow is that post place-and-route simulation can be accomplished at the customer's site, since NEC offers designers a choice of simulators within the "Golden simulator" category.

Golden simulator status means that upon receiving post place-and-route simulation results from a customer, NEC can then proceed directly to photomask production, bypassing any additional post-simulation steps. This can save a significant amount of design time.

The floorplanner tool provides realistic estimates of wire length by grouping hierarchical blocks into specific physical locations on the chip. This results in a more accurate simulation because critical path interconnect delays are minimized. The floorplanner also provides graphical I/O assignment capabilities and generates a delay file for post-floorplanner simulation.

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Figure 4. HDL Specification Design Flow