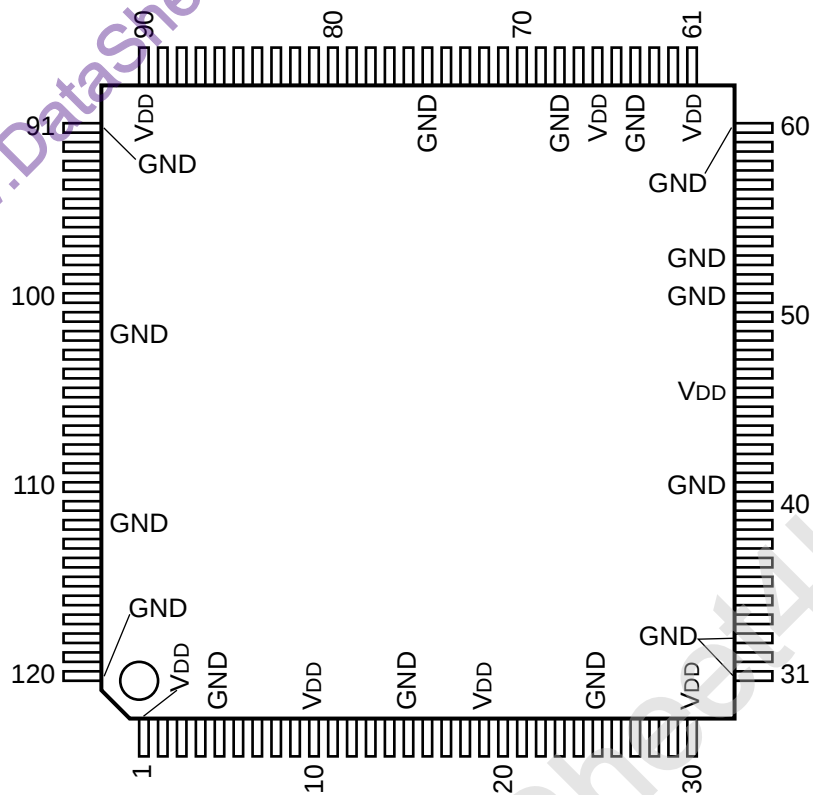

NETW-VCP INTERFACE

—TOP VIEW—



<u>2</u>	VA0	VD0	<u>18</u>
<u>3</u>	VA1	VD1	<u>17</u>
<u>4</u>	VA2	VD2	<u>16</u>
		VD3	<u>14</u>
<u>38</u>	HA0	VD4	<u>13</u>
<u>37</u>	HA1	VD5	<u>12</u>
<u>36</u>	HA2	VD6	<u>7</u>
<u>35</u>	HA3	VD7	<u>6</u>
<u>81</u>	PA0	HD0	<u>50</u>
<u>80</u>	PA1	HD1	<u>49</u>
<u>79</u>	PA2	HD2	<u>48</u>
<u>78</u>	PA3	HD3	<u>47</u>
<u>77</u>	PA4	HD4	<u>45</u>
<u>76</u>	PA5	HD5	<u>44</u>
<u>74</u>	PA6	HD6	<u>43</u>
<u>73</u>	PA7	HD7	<u>42</u>
<u>85</u>	RBA1	PC0	<u>70</u>
<u>87</u>	RBB1	PC1	<u>69</u>
<u>93</u>	RBA2	PC2	<u>59</u>
<u>95</u>	RBB2	PC3	<u>58</u>
<u>99</u>	RBA3	PC4	<u>57</u>
<u>101</u>	RBB3	PC5	<u>56</u>
		PC6	<u>55</u>
<u>63</u>	XIN	PC7	<u>54</u>
<u>67</u>	TEST		
<u>71</u>	PB	PE0	<u>29</u>
<u>82</u>	CK8K1	PE1	<u>28</u>
<u>83</u>	CK64K1	PE2	<u>27</u>
<u>88</u>	CK8K2	PE3	<u>26</u>
<u>89</u>	CK64K2	PE4	<u>24</u>
<u>96</u>	CK8K3	PE5	<u>23</u>
<u>97</u>	CK64K3	PE6	<u>22</u>
<u>104</u>	ST1	PE7	<u>21</u>
<u>106</u>	RT1		
<u>107</u>	RD1	PF	<u>20</u>
		HINT	<u>32</u>
<u>8</u>	VCS	XOUT	<u>62</u>
<u>9</u>	VRD	CLK12M	<u>65</u>
<u>11</u>	VWR	PD	<u>72</u>
<u>34</u>	HCS	TBA1	<u>84</u>
<u>39</u>	HRD	TBB1	<u>86</u>
<u>40</u>	HWR	TBA2	<u>92</u>
<u>52</u>	RESET	TBB2	<u>94</u>
<u>103</u>	NETINT	TBA3	<u>98</u>
<u>114</u>	TDMSL	TBB3	<u>100</u>
		SD1	<u>105</u>
<u>108</u>	ST2/PRIFS	SD2/PRIDX	<u>109</u>
<u>110</u>	RT2/PRICK	NETW8K	<u>113</u>
<u>111</u>	RD2/PRIDR	TDMFS	<u>116</u>
<u>115</u>	TDMOP	TDMCK	<u>117</u>
<u>119</u>	TDMDX	TDMDR	<u>118</u>

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V _{DD}	31	—	GND	61	—	V _{DD}	91	—	GND
2	I	VA0	32	O	HINT	62	O	XOUT	92	O	TBA2
3	I	VA1	33	—	GND	63	I	XIN	93	I	RBA2
4	I	VA2	34	I	HCS	64	—	GND	94	O	TBB2
5	—	GND	35	I	HA3	65	O	CLK12M	95	I	RBB2
6	I/O	VD7	36	I	HA2	66	—	V _{DD}	96	I	CK8K3
7	I/O	VD6	37	I	HA1	67	I	TEST	97	I	CK64K3
8	I	VCS	38	I	HA0	68	—	GND	98	O	TBA3
9	I	VRD	39	I	HRD	69	O	PC1	99	I	RBA3
10	—	V _{DD}	40	I	HWR	70	O	PC0	100	O	TBB3
11	I	VWR	41	—	GND	71	I	PB	101	I	RBB3
12	I/O	VD5	42	I/O	HD7	72	O	PD	102	—	GND
13	I/O	VD4	43	I/O	HD6	73	I	PA7	103	I	NETINT
14	I/O	VD3	44	I/O	HD5	74	I	PA6	104	I	ST1
15	—	GND	45	I/O	HD4	75	—	GND	105	O	SD1
16	I/O	VD2	46	—	V _{DD}	76	I	PA5	106	I	RT1
17	I/O	VD1	47	I/O	HD3	77	I	PA4	107	I	RD1
18	I/O	VD0	48	I/O	HD2	78	I	PA3	108	I	ST2/PRIFS
19	—	V _{DD}	49	I/O	HD1	79	I	PA2	109	O	SD2/PRIDX
20	O	PF	50	I/O	HD0	80	I	PA1	110	I	RT2/PRICK
21	O	PE7	51	—	GND	81	I	PA0	111	I	RD2/PRIDR
22	O	PE6	52	I	RESET	82	I	CK8K1	112	—	GND
23	O	PE5	53	—	GND	83	I	CK64K1	113	O	NETW8K
24	O	PE4	54	O	PC7	84	O	TBA1	114	I	TDMSL
25	—	GND	55	O	PC6	85	I	RBA1	115	I	TDMOP
26	O	PE3	56	O	PC5	86	O	TBB1	116	O	TDMFS
27	O	PE2	57	O	PC4	87	I	RBB1	117	O	TDMCK
28	O	PE1	58	O	PC3	88	I	CK8K2	118	O	TDMDR
29	O	PE0	59	O	PC2	89	I	CK64K2	119	I	TDMDX
30	—	V _{DD}	60	—	GND	90	—	V _{DD}	120	—	GND

INPUT

CK64K1-3	; EACH 64kHz CLOCK FOR ISDN BRI
CK8K1-3	; EACH 8kHz (OCTET TIMING) CLOCK FOR ISDN BRI
HA0-3	; ADDRESS FROM THE HOST CPU
$\overline{HCS}$	; CHIP SELECT FROM THE HOST CPU
$\overline{HRD}$	; READ ENABLE FROM THE HOST CPU
$\overline{HWR}$	; WRITE PULSE FROM THE HOST CPU
$\overline{NETINT}$	; INTERRUPT
PA0-7, PB	; INPUT PORTS
RBA1-3,	; EACH RECEIVING DATA FOR ISDN BRI
RBB1-3	
RD1	; RECEIVING DATA FOR EXCLUSIVE USE LINE (TA) I/F
RD2/PRIDR	; RECEIVING DATA FOR EXCLUSIVE USE LINE (TA) I/F
$\overline{RESET}$	; RESET
RT1	; RECEIVING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
RT2/PRICK	; RECEIVING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
ST1	; TRANSMITTING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
ST2/PRIFS	; TRANSMITTING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
TDMDX	; SERIAL DATA FOR TDM BUS
$\overline{TEST}$	; TEST MODE SETTING TERMINAL
TDMOP	; SERIAL DATA FROM THE SECOND VCP
$\overline{TDSL}$	; IN PRI MODE, DURING THIS TERMINAL IS ACTIVE, TREATS DATA FROM TDMDR AS INPUT SIGNAL FROM TDMOP
VA0-2	; ADDRESS FROM VCP
$\overline{VCS}$	; CHIP SELECT FROM VCP
$\overline{VRD}$	; READ ENABLE FROM VCP
$\overline{VWR}$	; WRITE PULSE FROM VCP
XIN	; CRYSTAL OSCILLATOR (12.288MHz)

OUTPUT

CLK12M	; 12.288MHz CLOCK
HINT	; INTERRUPT TO THE HOST CPU
NETW8K	; 8kHz PULSE SIGNAL DIVIDE CIRCUIT CLOCK
PC0-7, PD,	; OUTPUT PORTS
PE0-7, PF	
SD1	; TRANSMITTING DATA FOR EXCLUSIVE USE LINE (TA) I/F
SD2/PRIDX	; TRANSMITTING DATA FOR EXCLUSIVE USE LINE (TA) I/F
TBA1-3,	; EACH TRANSMITTING DATA FOR ISDN BRI
TBB1-3	
TDMCK	; CLOCK (3.072MHz) FOR TDM BUS
TDMDR	; SERIAL DATA FOR TDM BUS
TDMFS	; FRAME SYNC (8kHz) FOR TDM BUS
XOUT	; CRYSTAL OSCILLATOR (12.288MHz)

INPUT/OUTPUT

HD0-7	; DATA BUS FROM THE HOST CPU
VD0-7	; DATA BUS FROM VCP

