NEC Electronics Inc.

μPD70337 (V35 Software Guard) 16-Bit Microcomputer: Software-Secure, Single-Chip, CMOS

Description

The μPD70337 (V35 Software Guard) is a high-performance, 16-bit, single-chip microcomputer with a 16-bit external data bus. The μPD70337 is fully software compatible with the μPD70108/116 (V20®/V30®) as well as the μPD70320/330 (V25™/V35™).

The μPD70337 allows external executable code to be encrypted by a user-defined translation table. The μPD70337 will automatically decode the encrypted op-codes internally before the instructions are moved into the instruction execution register. As a result, the μPD70337 offers identical performance to the standard V35 even during security mode operation. The security feature may be selected by hardware and/or software, and may be switched from one state to the other under software control.

The μPD70337 has the same complement of internal peripherals as the standard V35 and maintains compatibility with existing drivers. Other than the additional mode select pin, the μPD70337 also maintains pin compatibility with other members of the standard V35 family.

Note: The electrical specifications of the V35 Software Guard and the standard V35 are the same. The instruction sets are also the same except BRKS and BRKN are added to control the Security and Normal operational modes. For electrical specifications and standard instructions, refer to the μPD70330/332 (V35) Data Sheet.

Features

- Security and normal operational modes
- System clock speeds to 8 MHz (16-MHz crystal)
- 16-bit CPU and internal data paths
- Functional compatibility with V35
- Software upward compatible with μPD8086
- New and enhanced V-Series instructions
- 6-byte prefetch queue
- Two-channel on-chip DMA controller
- Minimum instruction cycle: 250 ns at 8 MHz
- Internal 256-byte RAM memory
- 1-megabyte memory address space; 64K-byte I/O space
- Eight internal RAM-mapped register banks
- Four multifunction I/O ports
  - 8-bit analog comparator port
  - 20 bidirectional port lines
  - Four input-only port lines
- Two independent full-duplex serial channels
- Priority interrupt controller
  - Standard vectored service
  - Register bank switching
  - Macroservice
- Pseudo SRAM and DRAM refresh controller
- Two 16-bit timers
- On-chip time base counter
- Programmable wait state generator
- Two standby modes: STOP and HALT

Ordering Information

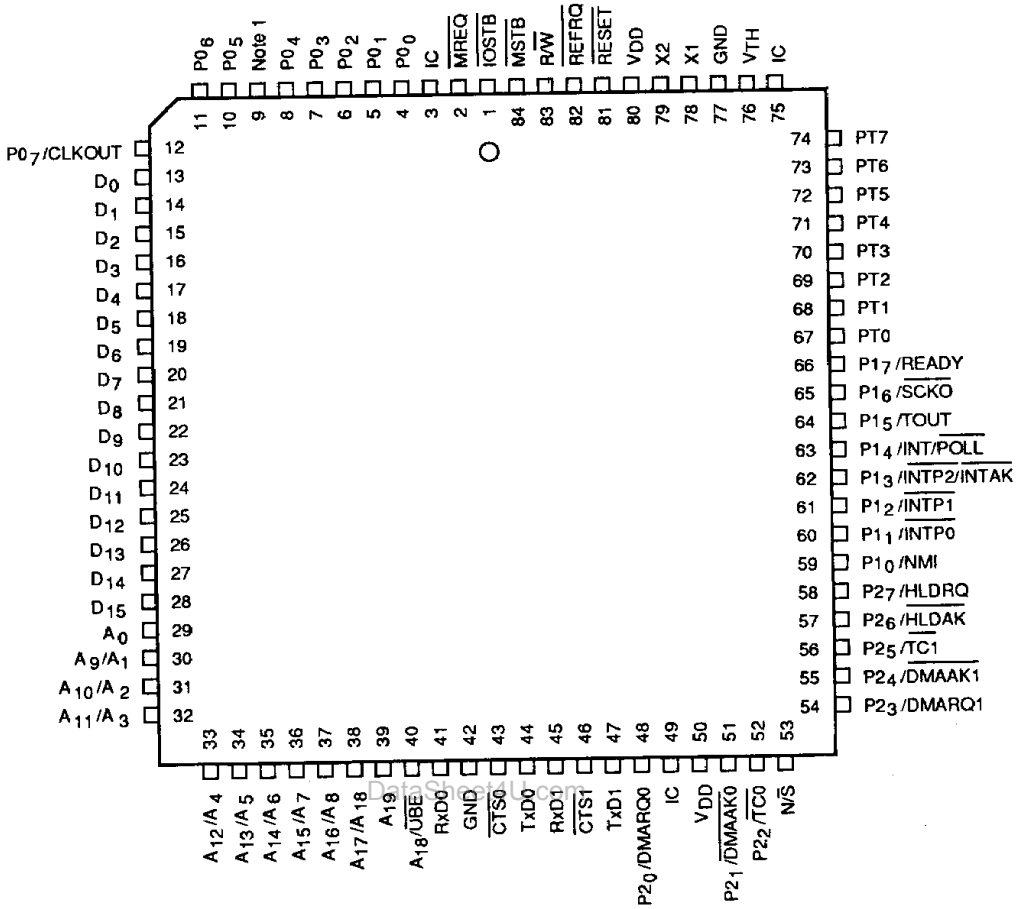
Part Number	Clock (MHz)	Package
μPD70337L-8-xxx	8	84-pin PLCC
GJ-8-xxx	8	94-pin plastic QFP

4g

V20 and V30 are registered trademarks of NEC Corporation.
V35 and V35 are trademarks of NEC Corporation.

Pin Configurations

84-Pin PLCC



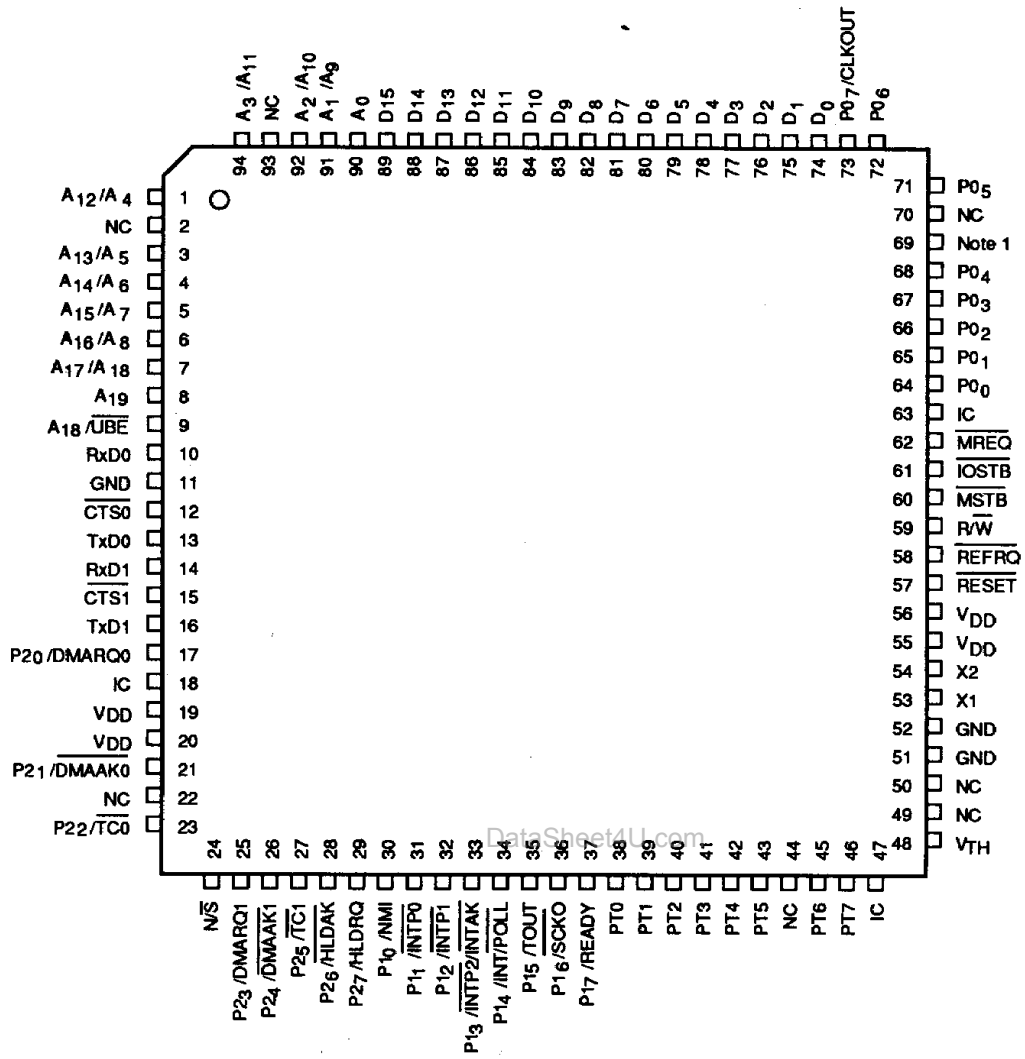
Notes:

(1) Connect pin 9 to GND through a 5- to 10-kΩ resistor.

(2) All IC pins should be tied together and pulled up to V_{DD} with a 10- to 20-kΩ resistor.

83SL-7209B

94-Pin Plastic QFP



Notes:

(1) Connect pin 69 to GND through a 5- to 10kΩ resistor.

(2) All IC pins should be tied together and pulled up to V_{DD} with a 10- to 20-kΩ resistor.

83SL-7210B

4g

Pin Identification

Symbol	Function
A_0-A_{19}	Address bus outputs
CLKOUT	System clock output
$\overline{CTS0}$	Clear-to-send input, serial channel 0
$\overline{CTS1}$	Clear-to-send input, serial channel 1
D_0-D_{15}	Bidirectional data bus
$\overline{DMAAK0}$	DMA acknowledge output, DMA controller channel 0
$\overline{DMAAK1}$	DMA acknowledge output, DMA controller channel 1
DMARQ0	DMA request input, DMA controller channel 0
DMARQ1	DMA request input, DMA controller channel 1
$\overline{HLDAK}$	Hold acknowledge output
HLDRQ	Hold request input
INT	Interrupt request input
$\overline{INTAK}$	Interrupt acknowledge output
$\overline{INTP0}$	Interrupt request 0 input
$\overline{INTP1}$	Interrupt request 1 input
$\overline{INTP2}$	Interrupt request 2 input
$\overline{IOSTB}$	I/O read or write strobe output
$\overline{MREQ}$	Memory request output
$\overline{MSTB}$	Memory strobe output
NMI	Nonmaskable interrupt request
N/$\overline{S}$	Normal mode/security mode select input
$P0_0$-$P0_7$	I/O port 0
$P1_0$-$P1_7$	I/O port 1
$P2_0$-$P2_7$	I/O port 2
$\overline{POLL}$	Input on $\overline{POLL}$ synchronizes the CPU and external devices
PT0-PT7	Comparator port input lines
READY	Ready signal input controls insertion of wait states
$\overline{REFRQ}$	DRAM refresh request output
$\overline{RESET}$	Reset signal input
R/$\overline{W}$	Read/write strobe output
RxD0	Receive data input, serial channel 0
RxD1	Receive data input, serial channel 1
$\overline{SCK0}$	Serial clock output
$\overline{TC0}$	Terminal count output; DMA completion, channel 0
$\overline{TC1}$	Terminal count output; DMA completion, channel 1
TOUT	Timer output
TxD0	Transmit data output, serial channel 0
TxD1	Transmit data output, serial channel 1
$\overline{UBE}$	Upper byte enable
X1, X2	Connections to external frequency control source (crystal, ceramic resonator, or clock)

Symbol	Function
V_{DD}	+5-volt power source input (two pins)
V_{TH}	Threshold voltage input to comparator circuits
GND	Ground reference (two pins)
IC	Internal connection; must be tied to V_{DD} externally through a pullup resistor

PIN FUNCTIONS

A_0-A_{19} (Address Bus)

To support dynamic RAMs, the 20-bit address is multiplexed on 11 lines. When $\overline{MREQ}$ is asserted, A_9-A_{17} are valid. When $\overline{MSTB}$ or $\overline{IOSTB}$ is asserted, A_1-A_8 and A_{18} are valid. A_{18} is also multiplexed with $\overline{UBE}$ and is valid when $\overline{MREQ}$ is asserted. Therefore A_{18} is active throughout the bus cycle. A_{19} and A_0 are not multiplexed but have dedicated pins and are valid throughout the bus cycle.

CLKOUT (Clock Out)

The system clock (CLK) is distributed from the internal clock generator to the CPU and output to peripheral hardware at the CLKOUT pin. This pin is sampled at system reset.

$\overline{CTS0}$ (Clear-to-Send 0)

This is the CTS pin of the channel 0 serial interface. In asynchronous mode, a low-level input on $\overline{CTS0}$ enables transmit operation. In I/O interface mode, $\overline{CTS0}$ is the receive clock pin.

$\overline{CTS1}$ (Clear-to-Send 1)

This is the CTS pin of the channel 1 serial interface. In asynchronous mode, a low-level input on $\overline{CTS1}$ enables transmit operation.

D_0-D_{15} (Data Bus)

D_0-D_{15} is the 16-bit data bus.

$\overline{DMAAK0}$ and $\overline{DMAAK1}$ (DMA Acknowledge)

These are the DMA acknowledge outputs of the DMA controller, channels 0 and 1. Signals are not output during DMA memory-to-memory transfer operations (burst mode, single-step mode).

$\overline{DMARQ0}$ and $\overline{DMARQ1}$ (DMA Request)

These are the DMA request inputs of the DMA controller, channels 0 and 1.

HLDAK (Hold Acknowledge)

The HLDAK output signal indicates that the hold request (HLDRQ) has been accepted. When HLDAK is active (low), the following lines go to the high-impedance state with internal 4700-Ω pullup resistors: A_0-A_{19}, D_0-D_7, IOSTB, MREQ, MSTB, REFRQ, and R/W.

HLDRQ (Hold Request)

The HLDRQ input from an external device requests that the μPD70335 relinquish the address, data, and control buses to an external bus master.

INT (Interrupt)

The INT input is a vectored interrupt request from an external device that can be masked by software. The active high level is detected in the last clock cycle of an instruction. The external device confirms that the INT interrupt request has been accepted by the INTAK signal output from the CPU.

The INT signal must be held high until the first INTAK signal is output. Together with INTAK, INT is used for operation with an interrupt controller such as μPD71059.

INTAK (Interrupt Acknowledge)

The INTAK output is the acknowledge signal for the software-maskable interrupt request INT. The INTAK signal goes low when the CPU accepts INT. The external device inputs the interrupt vector to the CPU via data bus D_0-D_7 in synchronization with INTAK.

INTP0, INTP1, INTP2 (Interrupt from Peripheral 0, 1, 2)

The INTPn inputs (n = 0, 1, 2) are external interrupt requests that can be masked by software. The INTPn input is detected at the effective edge specified by external interrupt mode register INTM.

The INTPn input is also used to release the HALT mode.

IOSTB (I/O Strobe)

A low-level output on IOSTB indicates that the I/O bus cycle has been initiated and that the I/O address output on A_0-A_{15} is valid.

MREQ (Memory Request)

A low-level output on MREQ indicates that the memory or I/O bus cycle has started and that address bits A_0, A_9-A_{17}, A_{18} and A_{19} are valid.

MSTB (Memory Strobe)

Together with MREQ and R/W, MSTB controls memory-accessing operations. MSTB should be used either to enable data buffers or as a data strobe. During memory write, a low-level output on MSTB indicates that data on the data bus is valid. A low-level output on MSTB indicates that multiplexed address bits A_1-A_8, A_{18}, and UBE are valid.

NMI (Nonmaskable Interrupt)

The NMI input is an interrupt request that cannot be masked by software. The NMI is always accepted by the CPU; therefore, it has priority over any other interrupt.

The NMI input is detected at the effective edge specified by external interrupt mode register INTM. Sampled in each clock cycle, NMI is accepted when the active level lasts for some clock cycles. When the NMI is accepted, a number 2 vector interrupt is generated after completion of the instruction currently being executed.

The NMI input is also used to release the CPU standby mode.

N/S (N Mode/S Mode)

Normal or security mode is selected by a fixed high level (N) or low level (S) at this pin. This pin is sampled at system reset and at the acceptance of interrupts.

$P0_0$-$P0_7$ (Port 0)

Port 0 is an 8-bit bidirectional I/O port.

$P1_0$-$P1_7$ (Port 1)

Lines $P1_4$-$P1_7$ are individually programmable as an input, output, or control function. The status of $P1_0$- $P1_3$ can be read but these lines are always control functions.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ are the lines of port 2, an 8-bit bidirectional I/O port. These lines can also be used as control signals for the on-chip DMA controllers.

POLL (Poll)

The POLL input is checked by the POLL instruction. If the level is low, execution of the next instruction is initiated. If the level is high, the POLL input is checked every five clock cycles until the level becomes low. The POLL functions are used to synchronize the CPU program and the operation of external devices.

4g

Note: $\overline{POLL}$ is effective when $P1_4$ is specified for the input port mode; otherwise, $\overline{POLL}$ is assumed to be at low level when the POLL instruction is executed.

PT0-PT7 (Port with Comparator)

The PT input is compared with a threshold voltage that is programmable to one of 16 voltage steps individually for each of the eight lines.

READY (Ready)

After READY is de-asserted low, the CPU will synchronize and insert at least two wait states into a read or write cycle to memory or I/O. This allows the processor to accommodate devices whose access times are longer than normal execution allows.

$\overline{REFRQ}$ (Refresh Request)

This output pulse can refresh nonstatic RAM. It can be programmed to meet system specifications and is internally synchronized so that refresh cycles do not interfere with normal CPU operation.

$\overline{RESET}$ (Reset)

This input signal is asynchronous. A low on $\overline{RESET}$ for a certain duration resets the CPU and all on-chip peripherals regardless of clock operation. The reset operation has priority over all other operations.

The reset signal is used for normal initialization/startup and also for releasing the STOP or HALT mode. After the reset signal returns high, program execution begins from address FFFF0H.

R/$\overline{W}$ (Read/Write Strobe)

When the memory bus cycle is initiated, the R/$\overline{W}$ signal output to external hardware indicates a read (high- level) or write (low-level) cycle. It can also control the direction of bidirectional buffers.

RxD0, RxD1 (Receive Data 0, 1)

These pins input data from serial channels 0 and 1.

In the asynchronous mode, when receive operation is enabled, a low level on the RxD0 or RxD1 input pin is recognized as the start bit and receive operation is initiated.

In the I/O interface mode (channel 0 only), receive data is input to the serial register at the rising edge of the receive clock.

$\overline{SCK0}$ (Serial Clock)

The $\overline{SCK0}$ output is the transmit clock of serial channel 0.

$\overline{TC0}$, $\overline{TC1}$ (Terminal Count 0, 1)

The $\overline{TC0}$ and $\overline{TC1}$ outputs go low when the terminal count of DMA service channels 0 and 1, respectively, reach zero, indicating DMA completion.

TOUT (Timer Output)

The TOUT signal is a square-wave output from the internal timer.

TxD0, TxD1 (Transmit Data 0, 1)

These pins output data from serial channels 0 and 1.

In the asynchronous mode, the transmit signal is in a frame format that consists of a start bit, 7 or 8 data bits (least significant bit first), parity bit, and stop bit. The TxD0 and TxD1 pins become mark state (high level) when transmit operation is disabled or when the serial register has no transmit data.

In the I/O interface mode (channel 0 only), the frame has 8 data bits and the most significant bit is transmitted first.

$\overline{UBE}$ (Upper Byte Enable)

$\overline{UBE}$ is a high-order memory bank selection signal output. $\overline{UBE}$ and A_0 determine which bytes of the data bus will be used. UBE is used with A_0 to select the even/odd banks as follows.

Operand	$\overline{UBE}$	A_0	Number of Bus Cycles
Even address word	0	0	1
Odd address word	0	1	2
	1	0	
Even address byte	1	0	1
Odd address byte	0	1	1

X1, X2 (Clock Control)

The frequency of the internal clock generator is controlled by an external crystal or ceramic resonator connected across pins X1 and X2. The crystal frequency is the same as the clock generator frequency f_X. By programming the PRC register, the system clock frequency f_{CLK} is selected as f_X divided by 2, 4, or 8.

As an alternative to the crystal or ceramic resonator, the positive and negative phases of an external clock (with frequency f_X) can be connected to pins X1 and X2.

V_{DD} (Power Supply)

+5-volt power source (two pins).

V_{TH} (Threshold Voltage)

Comparator port PT0-PT7 uses threshold voltage V_{TH} to determine the analog reference points. The actual threshold to each comparator line is programmable to $V_{TH} \times n/16$ where $n = 1$ to 16.

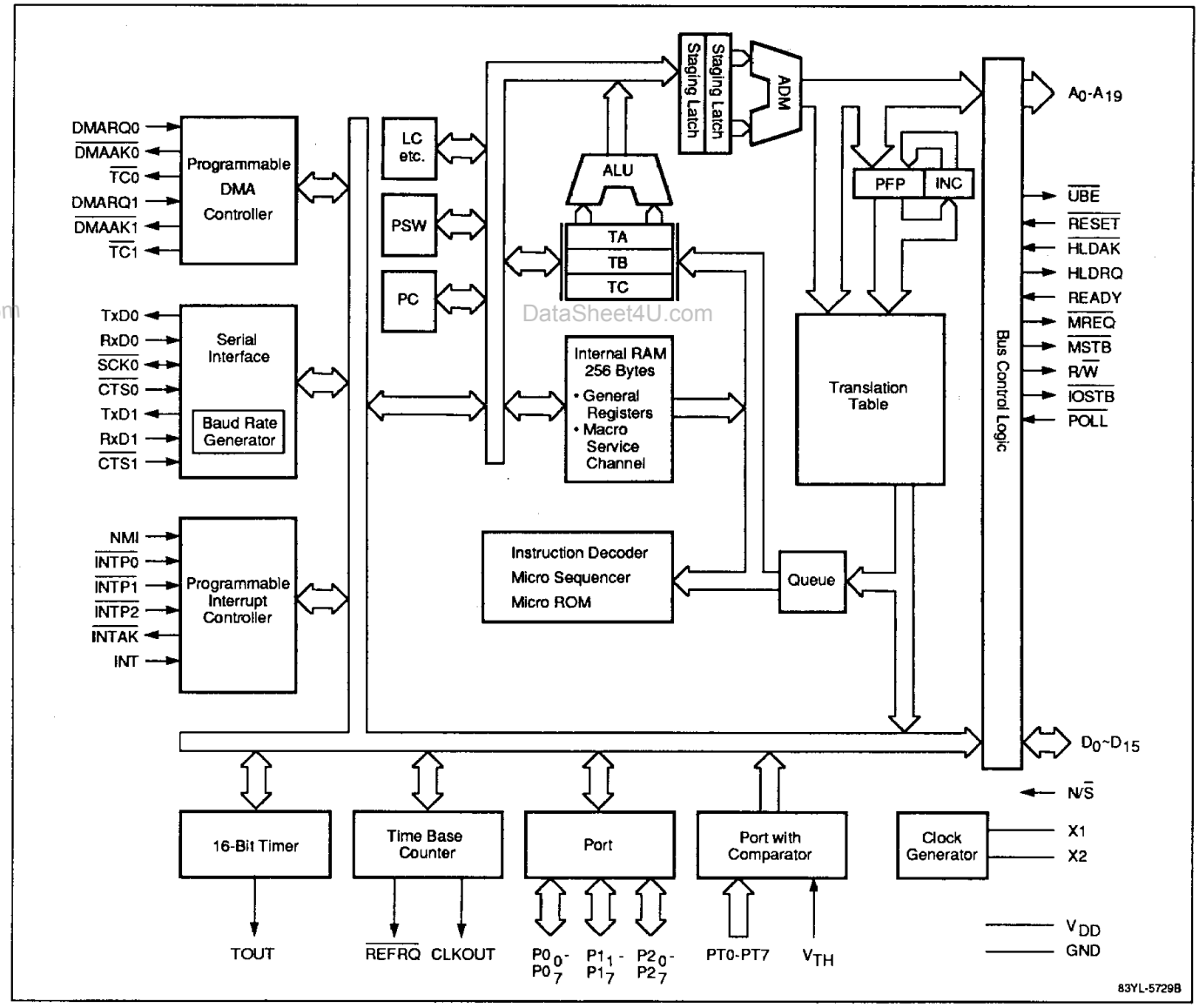
GND (Ground)

Ground reference (two pins).

IC (Internal Connection)

Internal connection; must be tied to V_{DD} externally through a 10-kΩ to 20-kΩ resistor.

μPD70337 Block Diagram



V25/V35 FAMILY

This addition to the V25/V35 family of high-integration microcomputers—the V35 Software Guard (V35S)—offers a direct DRAM interface with an external 16-bit data path. It supports both native V25/V35 operational modes as well as the enhanced security mode of operation. The security mode allows external code memory to be encrypted, thus preventing the unauthorized inspection of proprietary algorithms.

V35S Comparison to V25S

The V35S is fully software compatible with the μPD8088/8086 and the μPD70118/70116 (V20/V30) instruction set. Because the V35S is a ROMless part, all code must be located in external memory. The external memory may contain both encrypted opcodes and/or normal V-series opcodes.

The V35S contains the same core and peripherals as the V25 Software Guard (V25S). The main difference between the two is confined to the external bus interface and bus control logic. While the V25S is designed with an 8-bit external interface, the V35S provides the full 16-bit external data path.

The V35S external data bus is non-multiplexed; however, the 20-bit address bus is multiplexed to provide a direct DRAM style RAS/CAS bus cycle. As a result, the nominal bus cycle is three CLKOUT states. During the first bus state, the address lines output the high 9 bits of the physical address, A_{17}-A_9. During the second bus state, the address lines output low address bits A_8-A_1. Address lines A_{19} and A_0 are not multiplexed and are valid during the entire bus cycle. Address line A_{18} is multiplexed with the Upper Byte Enable signal (UBE) and is valid as an address during bus state one. During 16-bit transfers to odd addresses (UBE = 0 and A_0 = 1), two 8-bit bus cycles are performed.

The memory control signals of the V35S and V25S are identical; however, certain timing specifications are different, particularly for static memory interfaces. Refer to the V35 Data Sheet for these timing parameters. Typically, the MREQ signal is used to generate the DRAM RAS control signal, and the MSTB signal is used to generate the CAS signal. Like the V25S, the V35S provides an output from the internal refresh control unit, which is also typically gated into the DRAM RAS signal.

Another function of the V35S that is different from the V25S is the operation of the READY input pin. This pin is sampled in the middle of the second bus cycle (BAW1) on the V25S; the V35S samples one clock period later in the middle of BAW2.

Other than these bus controller differences, the V35S is identical to the V25S in its operation. All internal peripherals are programmed and operate in the same manner as those of the V25S. The instruction sets of the two processors are identical, and internally both processors operate on 16-bit data paths. Additionally, the security mode of the V35S functions identically to that of the V25S, although it fetches 16-bits of opcode per fetch cycle.

V35S Comparison to Standard V35

The V35S contains the same peripherals and maintains full upward functional compatibility with the standard V35. All internal functional units operate and are programmed the same as those of the V35. The instruction set is also a direct superset of the standard V35, containing all instructions of the V35 and adding only two to select the secure/normal operational modes.

The pinouts of the V35S and the V35 are the same except for two pins.

(1) $\overline{EA}$ on the V35 is IC on the ROMless V35S.

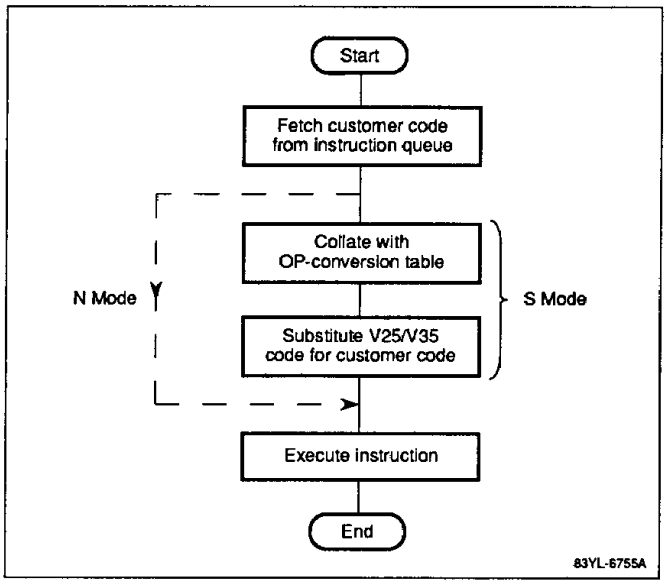
(2) N/$\overline{S}$ on the V35S is IC on the V35.

All other pins on the V35S perform identical functions to corresponding pins on the V35.

SECURITY MODE OPERATION

The security mode of the μPD70337 is designed to protect proprietary user software algorithms by encoding the user's programs resident in external system EPROM or ROM memory. The process encodes only the first byte of each opcode via a linear translation table. The decoding process is performed in real time within the μPD70337 and thus does not impact system performance. The flowchart of the conversion process is shown in figure 1.

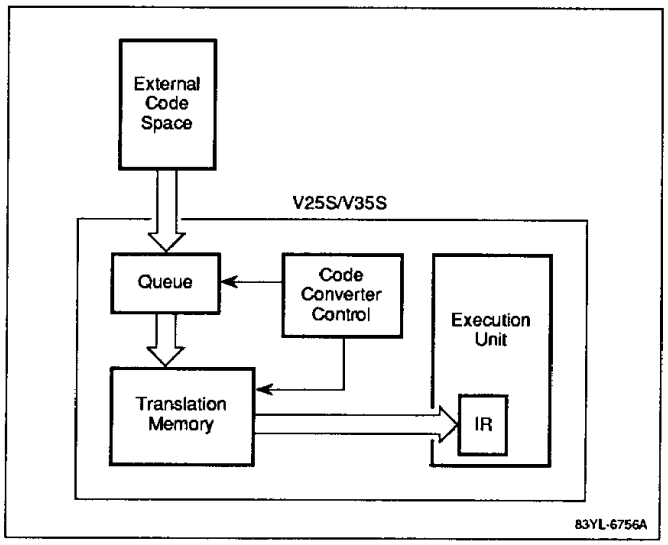
Figure 1. Opcode Translation Flowchart



The user-defined translation table is inserted into each μPD70337 mask at the factory. The μPD70337 can be dynamically switched from secure mode to normal mode, thus providing an additional measure of security as well as compatibility with existing ROM versions of V35 software. Note, however, that the V35 Software Guard does not support internal ROM.

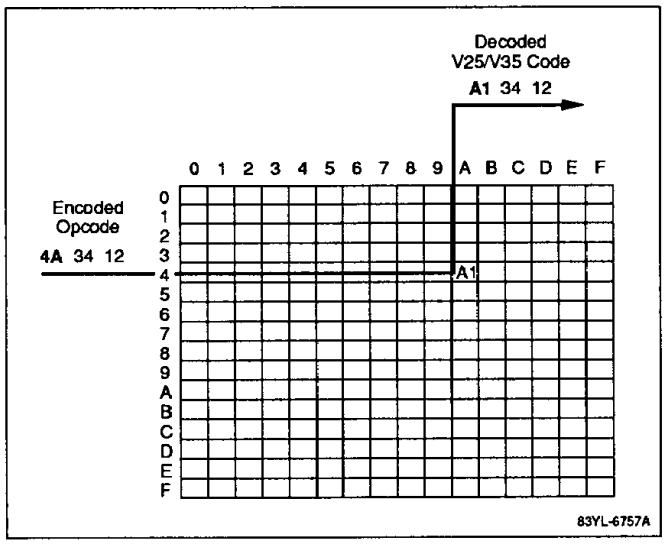
The opcode translator is effectively a look-up table that is inserted between the instruction prefetch queue and the instruction register of the μPD70337. A conceptual diagram of this is in figure 2.

Figure 2. Code Converter Functional Diagram



The code converter uses the encrypted opcode from the prefetch queue as an address, and provides the correct V35 opcode as data to the instruction register. An example of this is shown in figure 3. Again, only the first byte of each opcode is decoded, and subsequent bytes are passed directly from the prefetch unit to the execution unit.

Figure 3. Opcode Converter Translation Table



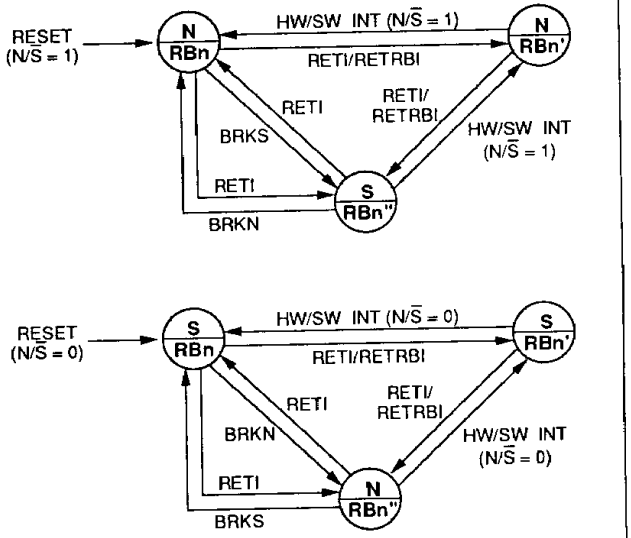
Mode Switching

The transition from normal V35 instruction execution to secure instruction decoding and execution can be performed in either hardware or software. The hardware trigger source is provided by the N/$\overline{S}$ pin of the μPD70337. This pin is listed as an internal connection pin on standard V35 systems, and as such, should be pulled up to V_{DD} through a resistor. Thus, a μPD70337 used in a standard V35 design will execute in normal mode identically to the standard V35.

The state of the N/$\overline{S}$ pin is read by the processor at system reset and determines the operational mode of the device at that point. Regardless of the state of this pin, the μPD70337 will begin program execution using register bank 7 as the default register set. (See figure 4.) If the processor samples the N/$\overline{S}$ pin in the low state, the first opcode fetched from the reset address will be decoded using the on-chip translation table. The N/$\overline{S}$ pin has an internal pull-up resistor that will set the device to normal mode operation with no external connections. The N/$\overline{S}$ pin should be set in hardware to a fixed logic state.

4g

Figure 4. Operational Mode State Transition Diagram



Software control of the operating mode is performed by the BRKS (Break for Secure Operation) and the BRKN (Break for Normal Operation) instructions. These opcodes are undefined codes on the standard V35 and should not be ported to standard V35 processor environments. These instructions are detailed in the instruction set section.

The operational state of the μPD70337 is specified by bit 15 (MD) of the Program Status Word (PSW). The remainder of the PSW (figure 5) is identical to that of the standard V35. Since portability of V35 and V35 Software Guard systems is sometimes desired, bit 15 of the PSW should always be written as a logical 1 in standard V35 systems. As with the V25/V35, the upper 4 bits of the PSW cannot be updated by POP; the upper 8 bits of the PSW cannot be updated by MOV.

Consult the μPD70327 (V25 Software Guard) data sheet for additional details of secure mode operation

Figure 5. Program Status Word (PSW)

MD	RB2	RB1	RB0	V	DIR	IE	BRK
15							8

S	Z	F1	AC	F0	P	BRKI	CY
7							0

Status Flag		Control Flags	
V	Overflow bit	DIR	Direction of string processing
S	Sign	IE	Interrupt enable
Z	Zero	BRK	Break (after every instruction)
AC	Auxiliary carry	RBn	Current register bank flags
P	Parity	BRKI	I/O trap enable
CY	Carry	F0, F1	General-purpose user flags (accessed by flag SFR)
		MD	Normal/security mode select

Operation Timing

Operational execution of the standard V35 and that of the V35 Software Guard are identical regardless of the operational mode selected for the V35 Software Guard. However, since the μPD70337 is a ROMless device, all memory cycles are nominally three system clock periods long. (This is in contrast to the one clock cycle ROM code fetch of the μPD70332.) Due to its ROMless nature, the μPD70337 does not support the $\overline{EA}$ pin of the standard V35, and this pin (labeled IC) should be fixed to a logical high level in the hardware.

ELECTRICAL SPECIFICATIONS

The electrical specifications of the V35 Software Guard and the standard V35 are the same. Refer to the μPD70330/332 (V35) Data Sheet.

INSTRUCTION SET

The instruction sets of the V35 Software Guard and the standard V35 are the same except for the addition of two mode change instructions for the V35 Software Guard (BRKS and BRKN) described below.

BRKS Instruction

The BRKS instruction switches operation to security (S) mode and generates a vectored interrupt. In S mode, the fetched operation code is executed after conversion in accordance with the built-in translation table.

The RETI instruction is used to return to the operating mode prior to execution of the BRKS instruction.

BRKN Instruction

The BRKN instruction switches operation to normal (N) mode and generates a vectored interrupt. In N mode, the fetched instruction is executed as a μPD70330/70332 (V35) operation code.

The RETI instruction is used to return to the operating mode prior to execution of the BRKN instruction.

Opcodes

Clock counts and opcodes applicable to the added mode change instructions are in tables 1 and 2.

Table 1. Instruction Clock Counts

Mnemonic	Operand	*Clocks
BRKS	imm8 (≠3)	56 + 10T [44 + 10T]
BRKN	imm8 (≠3)	56 + 10T [44 + 10T]

* Clock counts are specified for internal RAM enabled and [Internal RAM disabled].

Table 2. Mode Change Instructions

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	3	2	1	0	No. of Bytes	Flags
BRKS	imm8 (≠3)	(SP – 1, SP – 2) ← PSW, (SP – 3, SP – 4) ← PS, (SP – 5, SP – 6) ← PC, SP ← SP – 6 IE ← 0, BRK ← 0, MD ← 0 PC ← (n x 4 + 1, n x 4) PS ← (n x 4 + 3, n x 4 + 2) n = imm8	1	1	1	1	0	0	0	1	2	Not applicable
BRKN	imm8 (≠3)	(SP – 1, SP – 2) ← PSW, (SP – 3, SP – 4) ← PS, (SP – 5, SP – 6) ← PC, SP ← SP – 6 IE ← 0, BRK ← 0, MD ← 1 PC ← (n x 4 + 1, n x 4) PS ← (n x 4 + 3, n x 4 + 2) n = imm8	0	1	1	0	0	0	1	1	2	Not applicable

4g