μPD71084
Clock Pulse Generator/Driver

Description

The μPD71084 is a clock pulse generator/driver for microprocessors including the V20® and V30® and their peripherals using NEC's high-speed CMOS technology.

Features

- CMOS technology
- Clock pulse generator/driver for μPD70108/70116 or other CMOS or NMOS CPUs and their peripherals
- Frequency source can be crystal or external clock input
- Reset signal with Schmitt-trigger circuit for CPU or peripherals
- Bus ready signal with two-bus system synchronization
- Clock synchronization with other μPD71084s
- Single +5 V ±10% power supply
- Industrial temperature range: −40 to +85°C

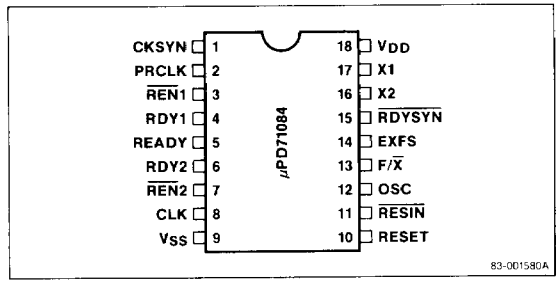
Ordering Information

Part Number	CLK Out, Max	Package
μPD71084C-8	8 MHZ	18-pin plastic DIP
C-10	10 MHz	
G-8	8 MHz	20-pin plastic SOP

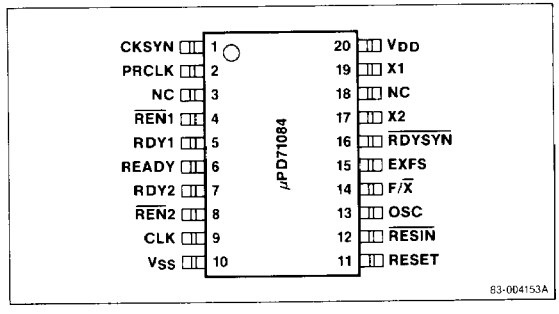
V20 and V30 are registered trademarks of NEC Corporation.

Pin Configurations

18-Pin Plastic DIP



20-Pin Plastic SOP



5i

Pin Identification

Symbol	Function
CKSYN	Clock synchronization input
PRCLK	Peripheral clock output
$\overline{REN1}$	Bus ready enable input 1
RDY1	Bus ready input 1
READY	Ready output
RDY2	Bus ready input 2
$\overline{REN2}$	Bus ready enable input 2
CLK	Processor clock output
V_{SS}	Ground potential
RESET	Reset output
$\overline{RESIN}$	Reset input
OSC	Oscillator output
F/$\overline{X}$	External frequency source/crystal select
EXFS	External frequency source input
$\overline{RDYSYN}$	Ready synchronization select input
X2	Crystal input
X1	Crystal input
V_{DD}	+5 V power supply
NC	No connection

PIN FUNCTIONS

X1, X2 (Crystal)

When the F/$\overline{X}$ input is low, a crystal connected to X1 and X2 will be the frequency source to generate clocks for a CPU and its peripherals. The crystal frequency should be three times the frequency of CLK.

EXFS (External Frequency)

EXFS is the external frequency input in the external TTL frequency source mode (F/$\overline{X}$ high). A TTL-level clock signal three times the frequency of the CLK output should be used for the source.

F/$\overline{X}$ (Frequency/Crystal Select)

F/$\overline{X}$ input selects whether an external TTL-level input or an external crystal input is the frequency source of the CLK output. When F/$\overline{X}$ is low, CLK is generated from the crystal connected to X1 and X2. When F/$\overline{X}$ is high, CLK is generated from an external TTL-level frequency input on the EXFS pin. At the same time, the internal oscillator circuit will stop and the OSC output will be high.

CLK (Processor Clock)

CLK output supplies the CPU and its local bus peripherals. CLK is a 33% duty cycle clock, one-third the frequency of the frequency source. The CLK output is +0.4 V higher than the other outputs.

PRCLK (Peripheral Clock)

PRCLK output supplies a 50% duty cycle clock at one-half the CLK frequency to drive peripheral devices.

OSC (Oscillator)

OSC outputs a signal at the same frequency as the crystal input. When EXFS is selected, the OSC output is powered down, and its output will be high.

CKSYN (Clock Synchronization)

CKSYN input synchronizes one μPD71084 to other μPD71084s. A high level at CKSYN resets the internal counter, and a low level enables it to count.

$\overline{RESIN}$ (Reset)

This Schmitt-trigger input generates the RESET output. It is used as a power-on reset.

RESET (Reset)

This output is a reset signal for the CPU. Reset timing is provided by the $\overline{RESIN}$ input to a Schmitt-trigger input gate and a flip-flop which will synchronize the reset timing to the falling edge of CLK. Power-on reset can be provided by a simple RC circuit on the $\overline{RESIN}$ input.

RDY1, RDY2 (Bus Ready)

A peripheral device drives the RDY1 or RDY2 inputs to signal that the data on the system bus has been received or is ready to be sent. $\overline{REN1}$ and $\overline{REN2}$ enable the RDY1 and RDY2 signals.

$\overline{REN1}$, $\overline{REN2}$ (Address Enable)

$\overline{REN1}$ and $\overline{REN2}$ inputs qualify their respective RDY inputs.

$\overline{RDYSYN}$ (Ready Synchronization Select)

$\overline{RDYSYN}$ input selects the mode of READY signal synchronization. A low-level signal makes the synchronization a two-step process. Two-step synchronization is used when RDY1 or RDY2 are not synchronized to the microprocessor clock and therefore cannot be guaranteed to meet the READY setup time. A high-level signal makes synchronization a one-step process. One-step

synchronization is used when RDY1 and RDY2 are synchronized to the processor clock. See Block Diagram.

READY (Ready)

The READY output signal to the processor is synchronized by the RDY inputs to the processor CLK. READY is cleared after RDY goes low and the guaranteed hold time of the processor has been met.

CRYSTAL

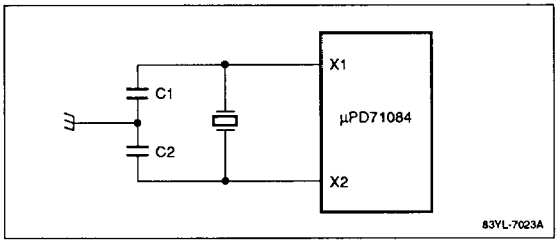
The oscillator circuit of the μPD71084 works with a parallel-resonant, fundamental mode, "AT-cut" crystal connected to pins X1 and X2.

Figure 1 shows the recommended circuit configuration. Capacitors C1 and C2 are required for frequency stability. The values of C1 and C2 (C1 = C2) can be calculated from the load capacitance (C_L) specified by the crystal manufacturer.

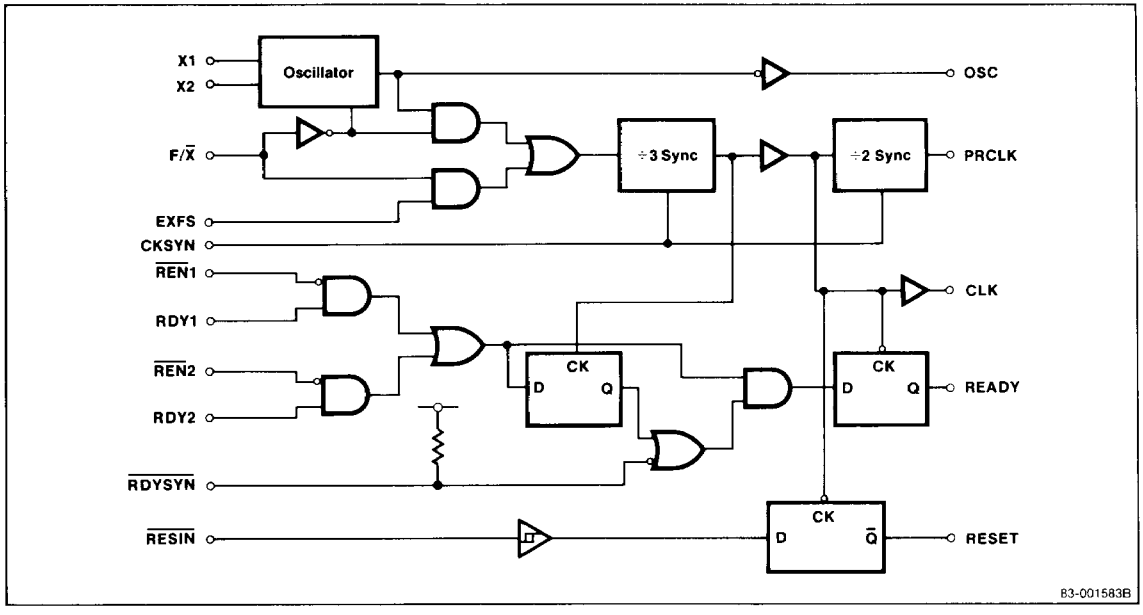
$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

C_S is any stray capacitance in parallel with the crystal, such as the μPD71084 input capacitance C_I

Figure 1. Crystal Configuration Circuit



μPD71084 Block Diagram



5i

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C; V_{SS} = 0 V

Power supply voltage, V_{DD}	−0.5 to + 7.0 V
Input voltage, V_I	−1.0 V to V_{DD} + 1.0 V
Output voltage, V_O	−0.5 V to V_{DD} + 0.5 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C
Power dissipation, P_D (DIP)	500 mW
Power dissipation, P_D (SOP)	200 mW

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

DC Characteristics

T_A = −40 to +85°C; V_{DD} = 5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Input voltage, high	V_{IH}	2.2		V	
		2.6		V	$\overline{RESIN}$ input
Input voltage, low	V_{IL}		0.8	V	
Output voltage, high	V_{OH}	V_{DD} − 0.4		V	CLK output, I_{OH} = −4 mA
		V_{DD} − 0.8		V	I_{OH} = −4 mA
Output voltage, low	V_{OL}		0.45	V	I_{OL} = 4 mA
Input leakage current	I_{IN}	−1.0	1.0	μA	
		−400	1.0	μA	$\overline{RDYSYN}$ input
$\overline{RESIN}$ hysteresis		0.25		V	
Power supply current (static)	I_{DD}		200	μA	
Power supply current (dynamic)	I_{DDdyn}		30	mA	f_{in} = 24 MHz

Capacitance

T_A = 25°C; V_{DD} = +5 V

Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_{in}		12	pF	f = 1 MHz

AC Characteristics

T_A = −40 to +85°C; V_{DD} 5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
EXFS high	t_{EHEL}	16		ns	At 2.2 V
EXFS low	t_{ELEH}	16		ns	At 0.8 V
EXFS period	t_{ELEL}	40		ns	
XTAL frequency		12	25	MHz	
RDY1, 2 setup to CLK ↓	t_{R1VCL}, t_{R1VCH}	35		ns	
RDY1, 2 hold to CLK ↓	t_{CLR1X}	0		ns	
$\overline{RDYSYN}$ setup to CLK ↓	t_{RSYVCL}	50		ns	
$\overline{RDYSYN}$ hold to CLK	t_{CLRSYX}	0		ns	
$\overline{REN}$1, 2 setup to RDY1, 2	t_{A1R1V}	15		ns	
$\overline{REN}$1, 2 hold to CLK ↓	t_{CLA1X}	0		ns	
CKSYN setup to EXFS	t_{YHEH}	20		ns	
CKSYN hold to EXFS	t_{EHYL}	20		ns	
CKSYN width	t_{YHYL}	$2t_{ELEL}$		ns	
$\overline{RESIN}$ setup to CLK	t_{I1HCL}	65		ns	
$\overline{RESIN}$ hold to CLK	t_{CLI1H}	20		ns	
CLK cycle period	t_{CLCL}	125		ns	
CLK high	t_{CHCL}	41		ns	3 V, f_{OSC} = 24 MHz (Note 1)
		1/3 (t_{CLCL}) +2		ns	1.5 V, f_{OSC} ≤ 24 MHz (Note 2)
CLK low	t_{CLCH}	68		ns	1.5 V, f_{OSC} = 24 MHz (Note 1)
		2/3 (t_{CLCL}) −15		ns	1.5 V, f_{OSC} ≤ 24 MHz (Note 2)
CLK rise and fall time	t_{CLH}, t_{CHL}		10	ns	1.5 to 3.5 V, 3.5 to 1.5 V
PRCLK high	t_{PHPL}	t_{CLCL} − 20		ns	(Note 3)
PRCLK low	t_{PLPH}	t_{CLCL} − 20		ns	(Note 3)
READY inactive to CLK ↓	t_{RYLCL}		8	ns	
READY active to CLK ↑	t_{RYHCH}		8	ns	

Parameter	Symbol	Min	Max	Unit	Conditions
CLK to RESET delay	t_{CLIL}		40	ns	
CLK to PRCLK ↑ delay	t_{CLPH}		22	ns	
CLK to PRCLK ↓ delay	t_{CLPL}		22	ns	
OSC CLK ↑ delay	t_{OLCH}	−5	22	ns	
OSC CLK ↓ delay	t_{OLCL}	2	35	ns	
Signal rise time (except CLK)	t_{LH}		20	ns	0.8 to 2.0 V
Signal fall time (except CLK)	t_{HL}		12	ns	2.0 to 0.8 V

Notes:

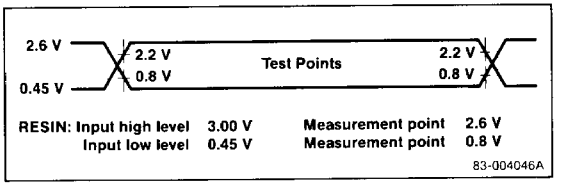
(1) Test points are specified in accordance with V-Series CMOS peripherals.

(2) Test points are specified in accordance with the μPD8284.

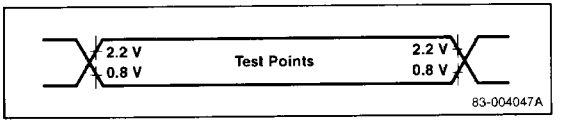
(3) t_{PHPL} + t_{PLPH} total must meet a minimum of 250 ns.

Timing Waveforms

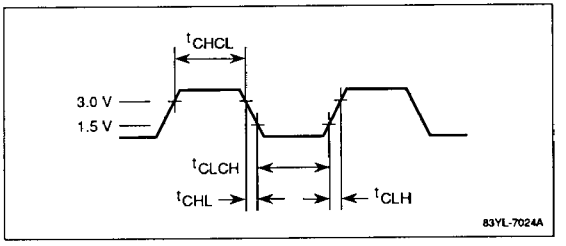
AC Test Input (Except $\overline{RESIN}$)



AC Test Output (Except CLK)

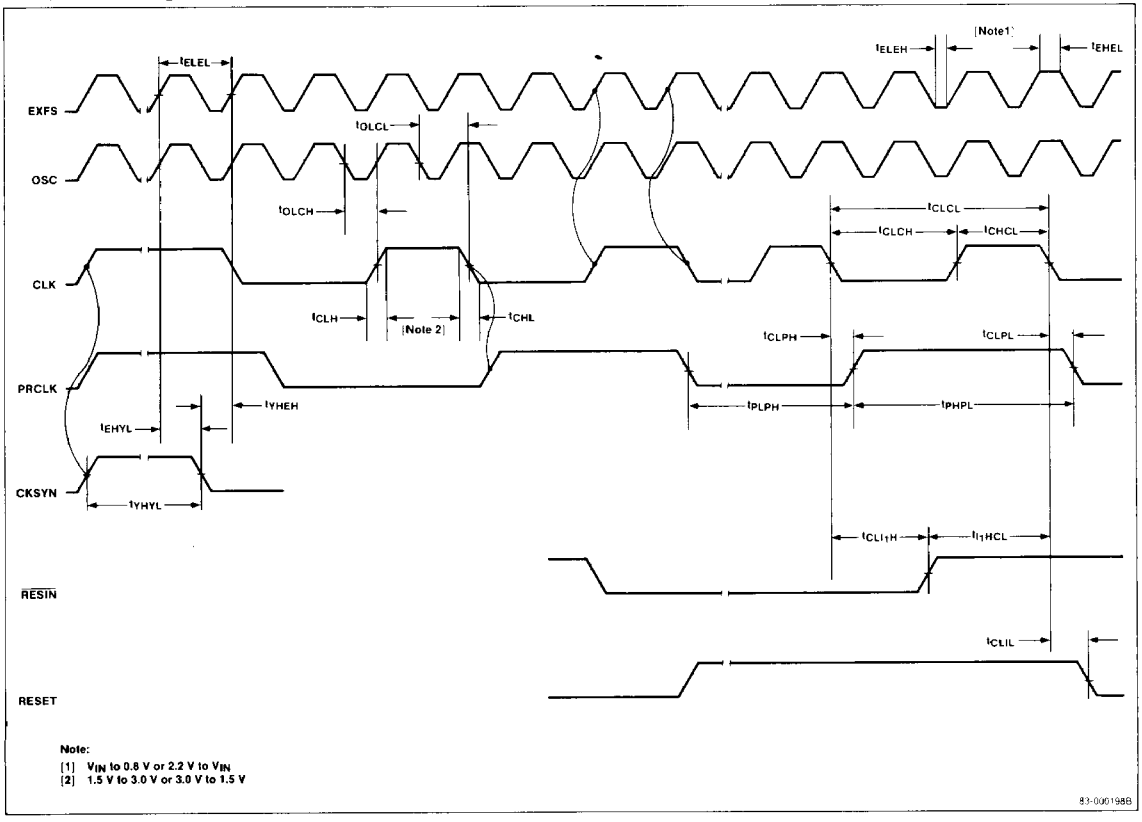


CLK Output

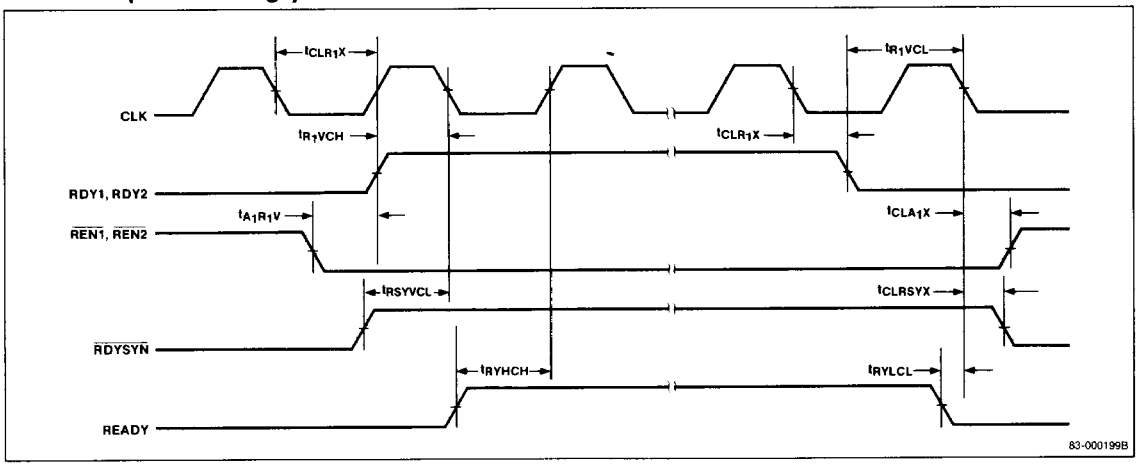


5i

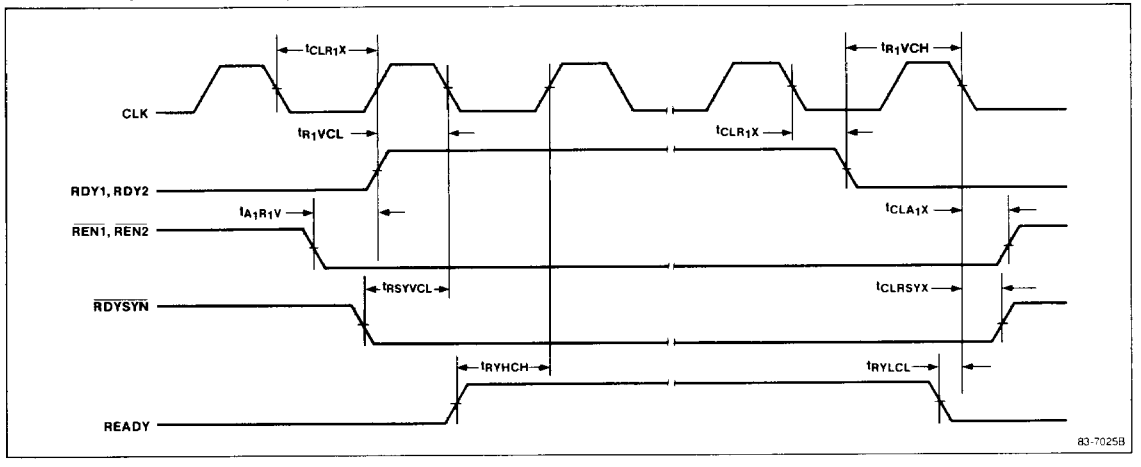
CLK, RESET Signals



READY Pin ($\overline{RDSYN}$ = High)

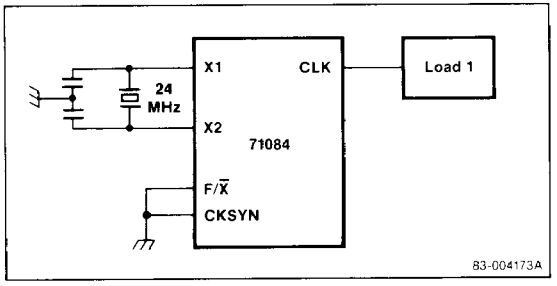


READY Pin ($\overline{RDSYN}$ = Low)

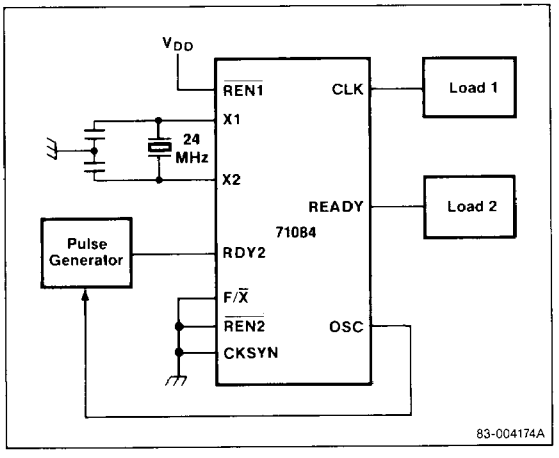


5i

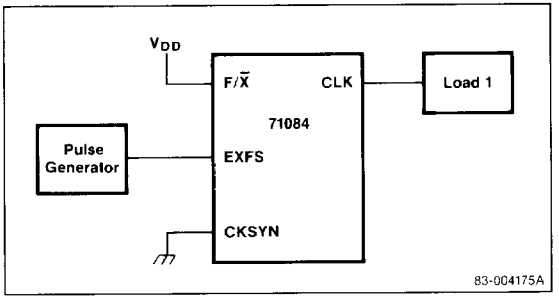
Test Circuit for CLK High or Low Time (Crystal Oscillation Mode)



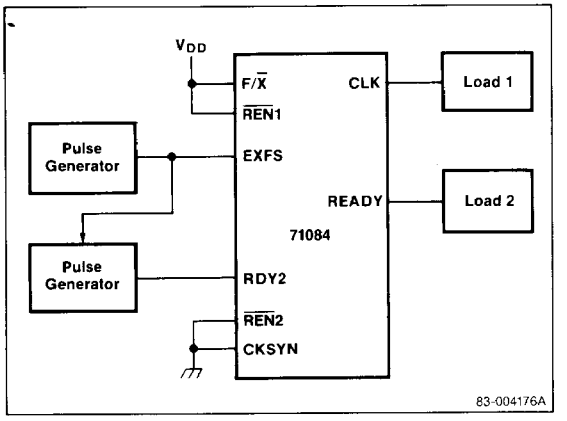
Test Circuit for CLK to READY (Crystal Oscillation Mode)



Test Circuit for CLK High or Low Time (EXFS Oscillation Mode)



Test Circuit for CLK to READY (EXFS Oscillation Mode)



Loading Circuits