NEC

MOS INTEGRATED CIRCUIT

μPD720400

PCI Express – PCI/PCI-X Bridge

(Ver 1.08)

μPD720400 is a PCI Express to PCI/PCI-X Bridge chip that supports the PCI Express Base Specification Revision1.1 and PCI Express to PCI/PCI-X Bridge Specification Revision1.0. μPD720400 contains a PCI Express Serdes circuit with an x8 Lane structure as a primary interface and two 64bits PCI/PCI-X bus interface circuits.

Ordering Information

Part number	Package	Chip Version	Remark
μPD720400FF-RN1	648-pin Tape BGA (35x35)	Ver.4.1	
μPD720400FF-RN1-A	648-pin Tape BGA (35x35)	Ver.4.1	Lead-free product
μPD720400AFF-RN1	648-pin Tape BGA (35x35)	Ver.4.3	
μPD720400AFF-RN1-A	648-pin Tape BGA (35x35)	Ver.4.3	Lead-free product
μPD720400CFF-RN1	648-pin Tape BGA (35x35)	Ver.4.5	
μPD720400CFF-RN1-A	648-pin Tape BGA (35x35)	Ver.4.5	Lead-free product

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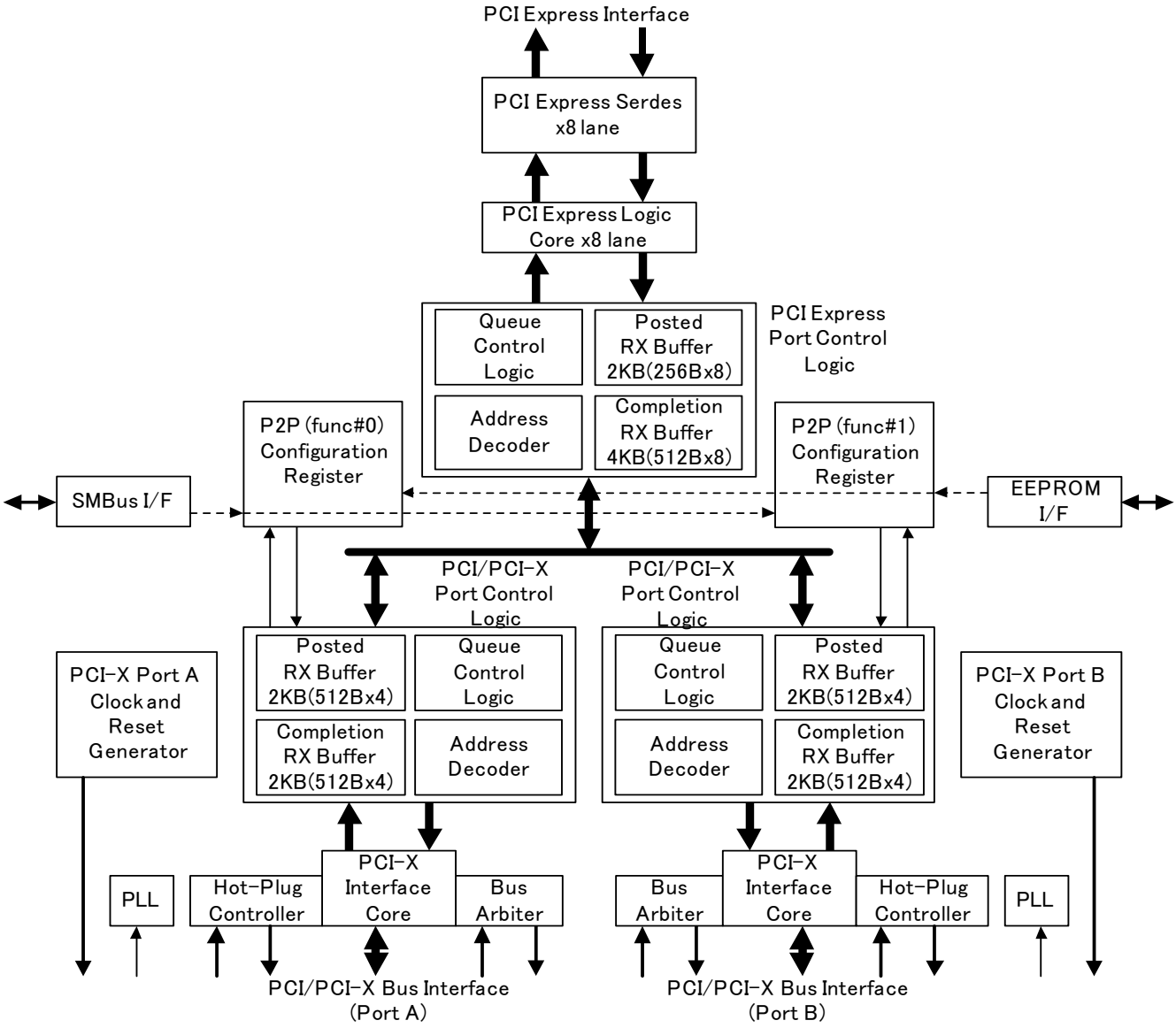
1. Features

- PCI Express Interface
  - Compliant with The PCI Express Base Specification Revision 1.1
  - Contains x8Lane 2.5Gbps full-duplex serial interface PCI Express Serdes
  - Supports 1 Virtual Channel
  - Supports 256 byte Max Payload Size
  - Supports PCI Express Advanced Error Logging
  - Supports Data Poisoning
  - Supports ECRC checking and generation
- PCI/PCI-X Interface
  - Compliant with the PCI Local Bus Specification Revision 3.0, PCI-X Protocol/Electrical and Mechanical Addendum to the PCI Local Bus Specification Revision 2.0a
  - Compliant with PCI-PCI Bridge Specification Revision 1.2 and PCI Express to PCI/PCI-X Bridge Specification Revision 1.0
  - Supports two PCI/PCI-X bus interfaces
  - Supports 133MHz Single Data Rate 64 bit PCI-X mode (PCI-X Mode1) and 66MHz 64 bit PCI mode
  - Supports 3.3V signaling (not supports 5V tolerant signaling)
  - Supports LOCK# transaction
  - Contains arbitration fucntions for up to 4 external agents at each PCI/PCI-X port
  - Supports PCI bus parking function
- SMBus Interface
  - Conforms to SMBus Specification Version 2.0
  - SMBus Slave interface
  - Supports Read/Write access to internal configuration and memory mapped registers
  - Supports Packet Error Checking (PEC)
  - Supports SMBus Alert
- EEPROM Interface
  - Parameter loading from Serial EEPROM (set in Configuration registers)
- Hot Plug Controller
  - Compliant with PCI SHPC and Subsystem Specification Revision 1.0
  - Supports Hot Plug Controller functions at each PCI/PCI-X port
  - Supports Hot Plug Slot controls in both parellel and serial modes
  - Supports interface for ACPI Hot Plug handling as well as OSHP (Operating System Hot Plug)
- Power Management
  - Compliant with to PCI Bus Power Management Interface Specification Revision1.1
  - Supports D0, D1 and D3 power states

  - Supports S3 wake-up by PME Messaging
  - Supports PCI Express Active State Power Management L0s and L1
- Memory Buffer Architecture
  - Contains a 4K byte completion data reception buffer and a 2K byte Posted data reception buffer in the PCI Express interface port
  - Contains a 2K byte completion data reception buffer and a 2K byte Posted data reception buffer in the PCI/PCI-X interface port
  - 8 Posted Transactions managed by a PCI Express interface
  - 8 Non-posted Split Transactions managed by a PCI Express interface
  - 4 Posted Transactions managed by each PCI/PCI-X interface port
  - 4 Non-posted Split Transactions managed by each PCI/PCI-X interface port
  - 4 Delayed Transactions managed by each PCI/PCI-X interface
  - Supports Parity Protection of built-in SRAM data
- Testing
  - Supports IEEE® 1149.1 JTAG

2. Block Diagram

Figure 2-1 Block Diagram of μPD720400



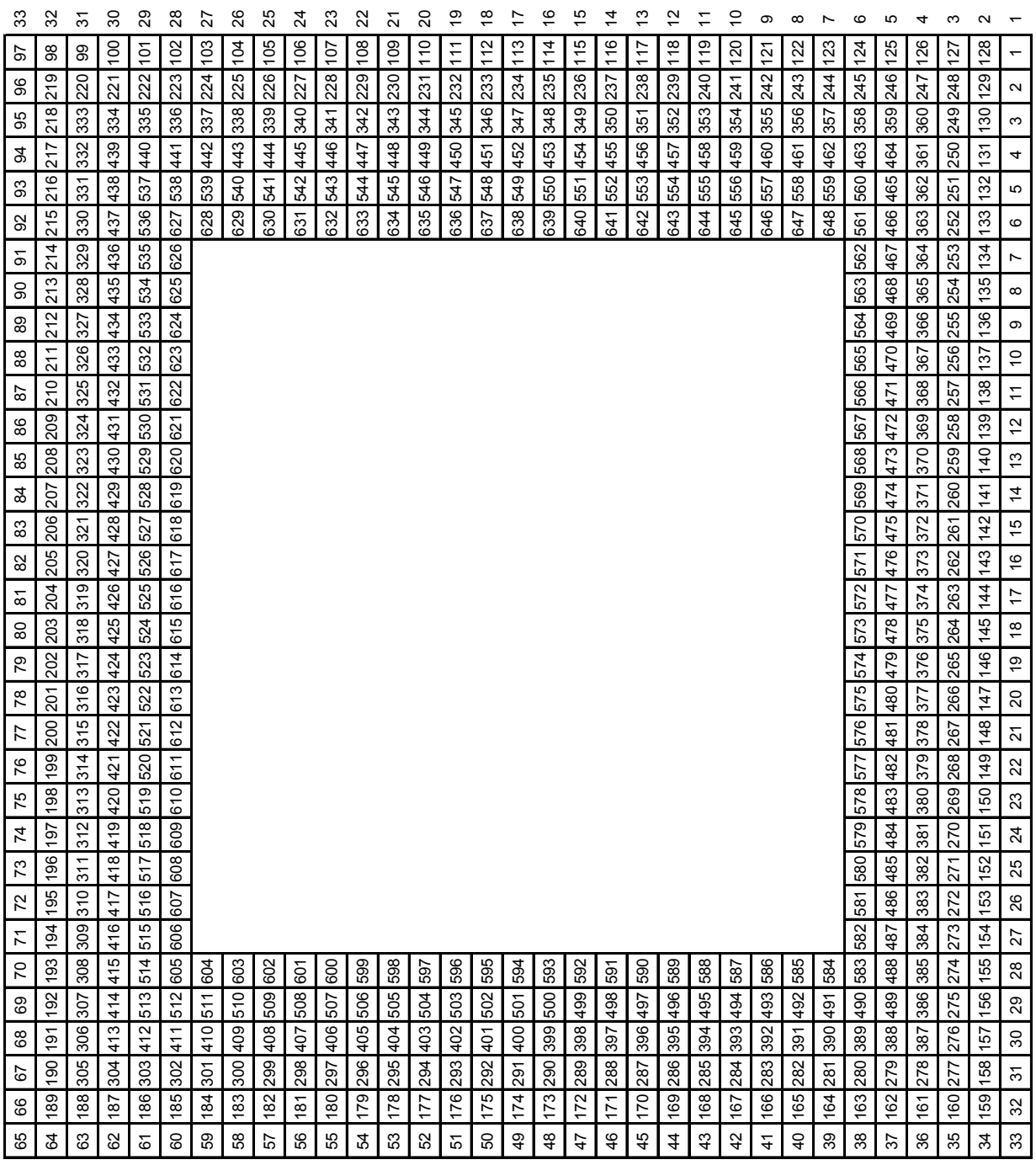
PCI Express Serdes	x8Lane Full duplex Serializer/Deserializer function
PCI Express Logic Core	PCI Express Logical Protocol (Logical Physical Layer, Data Link Layer, Transaction Layer (Flow Control Management)) function
PCI Express Port Control Logic	PCI Express port reception buffer control, address decoding process, transaction queue control function
PCI/PCI-X Port Control Logic	PCI/PCI-X port reception buffer control, address decoding process, transaction queue control function
PCI-X Interface Core	64bits PCI/PCI-X Master, Target processing function
Bus Arbiter	PCI/PCI-X bus arbitration function
Hot-Plug Controller	SHPC compatible Hot-Plug Controller processing function
P2P Configuration Register	Type 1 PCI-PCI Bridge Configuration Register
PCI-X Port Clock and Reset Generator	PCI/PCI-X Clock generation and Reset generation
PLL	Feedback PCI Cock Skew rectification PLL
SMBus I/F	SMBus Slave controller function
EEPROM I/F	Serial EEPROM Master controller function

3. Pin Connection

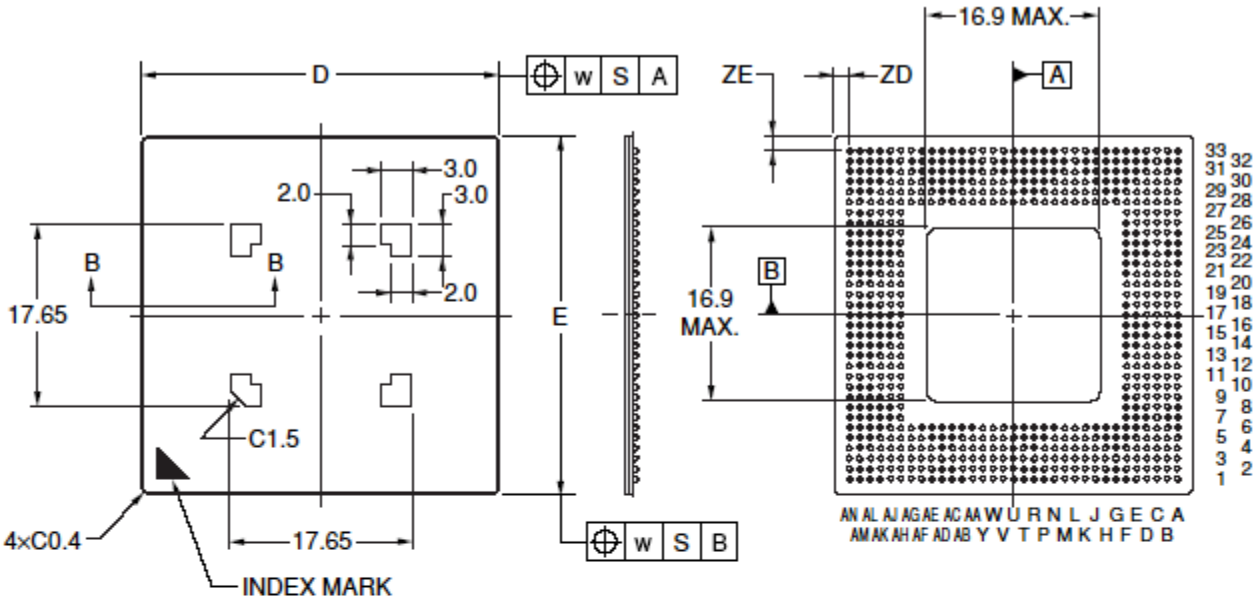
- **648-pin tape BGA (35 x 35 mm)**

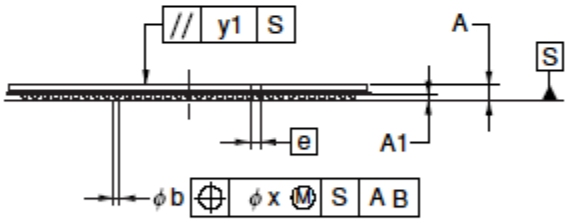
  μPD720400

Bottom view

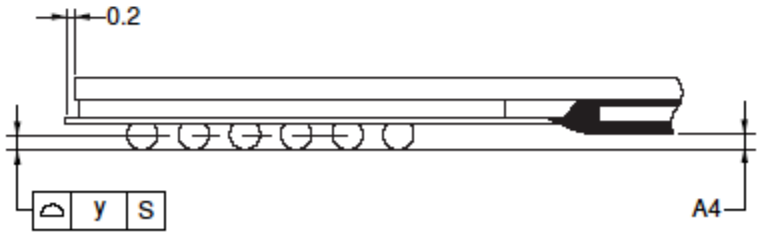


648-PIN TAPE BGA (35x35)





SECTION B-B



(UNIT:mm)

ITEM	DIMENSIONS
D	35.00±0.20
E	35.00±0.20
w	0.30
e	1.00
A	1.30±0.30
A1	0.50±0.10
A4	0.25 MIN.
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.50
ZE	1.50

P648FF-100-RN1

3.1. Pin List (numerical order)

PKG	NAME	PKG	NAME	PKG	NAME	PKG	NAME
A01	N.C.	B18	SA_AD30	D02	SMB_ADD1	E19	VSS
A02	N.C.	B19	SA_AD27	D03	N.C.	E20	VSS
A03	N.C.	B20	SA_AD24	D04	N.C.	E21	VSS
A04	VDD3.3	B21	SA_AD22	D05	N.C.	E22	VSS
A05	SB_CLKM	B22	SA_AD19	D06	SD_TESTEN	E23	N.C.
A06	SB_AD13	B23	SA_CBE2B	D07	N.C.	E24	VSS
A07	SB_AD15	B24	SA_TRDYB	D08	SB_PERRB	E25	N.C.
A08	SB_SERRB	B25	SA_LOCKB	D09	VDD1.5	E26	VSS
A09	SB_PCIXCAP_I	B26	SA_SERRB	D10	N.C.	E27	N.C.
A10	SB_PCIXCAP_P	B27	SA_AD15	D11	VDD1.5	E28	N.C.
A11	SB_TRDYB	B28	SA_PAR	D12	N.C.	E29	N.C.
A12	SB_FRAMEB	B29	SB_HPCM1	D13	SB_AD20	E30	N.C.
A13	SB_AD17	B30	SA_HPCM0	D14	N.C.	E31	SA_SLOTM1
A14	SB_AD21	B31	VDD3.3	D15	VDD1.5	E32	TMC2
A15	SB_CBE3B	B32	N.C.	D16	N.C.	E33	SA_AD10
A16	SB_AD26	B33	N.C.	D17	N.C.	F01	SB_AD10
A17	SB_AD29	C01	SMB_ADD0	D18	N.C.	F02	SB_AD11
A18	SA_AD29	C02	ROSC_N5	D19	N.C.	F03	SMB_ADD3
A19	SA_AD26	C03	N.C.	D20	N.C.	F04	SMB_ADD4
A20	SA_CBE3B	C04	N.C.	D21	N.C.	F05	N.C.
A21	SA_AD21	C05	VDD3.3	D22	N.C.	F06	N.C.
A22	SA_AD18	C06	SB_SLOTM1	D23	SA_AD17	F07	N.C.
A23	SA_FRAMEB	C07	N.C.	D24	VDD1.5	F08	N.C.
A24	SA_DEVSELB	C08	SB_CBE1B	D25	N.C.	F09	VDD3.3
A25	SA_PCIXCAP_P	C09	N.C.	D26	N.C.	F10	VDD3.3
A26	SA_PCIXCAP_I	C10	SB_DEVSELB	D27	N.C.	F11	VDD3.3
A27	SA_AD14	C11	N.C.	D28	SB_HPCM0	F12	VDD3.3
A28	SA_AD12	C12	SB_AD16	D29	N.C.	F13	VDD1.5
A29	SA_AD11	C13	SB_AD19	D30	N.C.	F14	VDD3.3
A30	SA_CLKM	C14	SB_AD23	D31	ROSC_N9	F15	VDD3.3
A31	EPR_EN	C15	SB_AD25	D32	SA_SLOTM2	F16	VDD3.3
A32	VDD3.3	C16	SB_AD28	D33	TMC1	F17	VDD3.3
A33	N.C.	C17	SB_AD31	E01	SB_AD12	F18	VDD1.5
B01	VSS	C18	SA_AD31	E02	N.C.	F19	VDD3.3
B02	N.C.	C19	SA_AD28	E03	SMB_ADD2	F20	VDD1.5
B03	N.C.	C20	SA_AD25	E04	N.C.	F21	VDD3.3
B04	N.C.	C21	SA_AD23	E05	N.C.	F22	VDD1.5
B05	SB_SLOTM2	C22	SA_AD20	E06	N.C.	F23	VDD3.3
B06	CTRI	C23	SA_AD16	E07	SB_SLOTM0	F24	VDD3.3
B07	SB_AD14	C24	SA_IRDYB	E08	VSS	F25	VDD3.3
B08	SB_PAR	C25	SA_STOPB	E09	N.C.	F26	VDD1.5
B09	SB_LOCKB	C26	SA_PERRB	E10	VSS	F27	VDD3.3
B10	SB_STOPB	C27	SA_CBE1B	E11	VSS	F28	N.C.
B11	SB_IRDYB	C28	SA_AD13	E12	VSS	F29	N.C.
B12	SB_CBE2B	C29	SA_HPCM1	E13	N.C.	F30	SA_SLOTM0
B13	SB_AD18	C30	N.C.	E14	VSS	F31	DC_TEST_MODE
B14	SB_AD22	C31	N.C.	E15	N.C.	F32	SA_M66EN_O
B15	SB_AD24	C32	N.C.	E16	VSS	F33	SA_M66EN
B16	SB_AD27	C33	N.C.	E17	VSS	G01	SB_CBE0B
B17	SB_AD30	D01	DBT_MODE	E18	VSS	G02	SB_AD9

PKG	NAME	PKG	NAME	PKG	NAME	PKG	NAME
G03	SB_M66EN	L05	VSS	R28	VDD3.3	W30	N.C.
G04	SB_M66EN_O	L06	VDD3.3	R29	N.C.	W31	SA_AD45
G05	N.C.	L28	VDD3.3	R30	SA_AD57	W32	SA_AD44
G06	N.C.	L29	VSS	R31	SA_AD56	W33	SA_AD43
G28	N.C.	L30	N.C.	R32	SA_AD55	Y01	SB_AD41
G29	VSS	L31	SA_REQ64B	R33	SA_AD54	Y02	SB_AD42
G30	N.C.	L32	SA_ACK64B	T01	SB_AD53	Y03	SB_AD43
G31	SA_AD9	L33	SA_CBE7B	T02	SB_AD54	Y04	N.C.
G32	SA_AD8	M01	SB_CBE4B	T03	SB_AD55	Y05	VSS
G33	SA_CBE0B	M02	SB_CBE5B	T04	N.C.	Y06	VDD3.3
H01	SB_AD6	M03	SB_CBE6B	T05	VSS	Y28	VDD1.5
H02	SB_AD7	M04	N.C.	T06	VDD1.5	Y29	VSS
H03	SB_AD8	M05	VSS	T28	N.C.	Y30	N.C.
H04	VDD1.5	M06	VDD1.5	T29	VSS	Y31	SA_AD42
H05	VSS	M28	VDD3.3	T30	N.C.	Y32	SA_AD41
H06	VDD3.3	M29	VSS	T31	SA_AD53	Y33	SA_AD40
H28	VDD3.3	M30	SA_CBE6B	T32	SA_AD52	AA01	SB_AD37
H29	VSS	M31	SA_CBE5B	T33	SA_AD51	AA02	SB_AD38
H30	N.C.	M32	SA_CBE4B	U01	SB_AD50	AA03	SB_AD39
H31	SA_AD7	M33	SA_PAR64	U02	SB_AD51	AA04	SB_AD40
H32	SA_AD6	N01	SB_AD62	U03	SB_AD52	AA05	N.C.
H33	SA_AD5	N02	SB_AD63	U04	N.C.	AA06	VDD1.5
J01	SB_AD3	N03	SB_PAR64	U05	VSS	AA28	VDD3.3
J02	SB_AD4	N04	N.C.	U06	VDD3.3	AA29	VSS
J03	SB_AD5	N05	VSS	U28	VDD3.3	AA30	N.C.
J04	N.C.	N06	VDD3.3	U29	VSS	AA31	SA_AD39
J05	N.C.	N28	VDD1.5	U30	VDD1.5	AA32	SA_AD38
J06	VDD3.3	N29	N.C.	U31	N.C.	AA33	SA_AD37
J28	VDD1.5	N30	N.C.	U32	SA_AD50	AB01	SB_AD34
J29	N.C.	N31	SA_AD63	U33	SA_AD49	AB02	SB_AD35
J30	N.C.	N32	SA_AD62	V01	SB_AD47	AB03	SB_AD36
J31	SA_AD4	N33	SA_AD61	V02	SB_AD48	AB04	N.C.
J32	SA_AD3	P01	SB_AD59	V03	SB_AD49	AB05	VSS
J33	SA_AD2	P02	SB_AD60	V04	N.C.	AB06	VDD3.3
K01	SB_AD0	P03	SB_AD61	V05	VSS	AB28	VDD1.5
K02	SB_AD1	P04	N.C.	V06	VDD3.3	AB29	VSS
K03	SB_AD2	P05	VSS	V28	VDD3.3	AB30	SA_AD36
K04	VDD1.5	P06	VDD1.5	V29	VSS	AB31	SA_AD35
K05	VSS	P28	VDD3.3	V30	N.C.	AB32	SA_AD34
K06	VDD3.3	P29	VSS	V31	SA_AD48	AB33	SA_AD33
K28	VDD3.3	P30	VDD1.5	V32	SA_AD47	AC01	SB_AD32
K29	VSS	P31	SA_AD60	V33	SA_AD46	AC02	SB_AD33
K30	VDD1.5	P32	SA_AD59	W01	SB_AD44	AC03	N.C.
K31	N.C.	P33	SA_AD58	W02	SB_AD45	AC04	VDD1.5
K32	SA_AD1	R01	SB_AD56	W03	SB_AD46	AC05	VSS
K33	SA_AD0	R02	SB_AD57	W04	VDD1.5	AC06	VDD3.3
L01	SB_CBE7B	R03	SB_AD58	W05	N.C.	AC28	VDD3.3
L02	SB_REQ64B	R04	N.C.	W06	VDD3.3	AC29	N.C.
L03	SB_ACK64B	R05	VSS	W28	VDD3.3	AC30	VDD1.5
L04	N.C.	R06	VDD3.3	W29	VSS	AC31	SA_GNT0B

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PKG	NAME	PKG	NAME	PKG	NAME	PKG	NAME
AC32	SA_GNT1B	AH01	AVDD2	AJ18	VSS	AL02	N.C.
AC33	SA_AD32	AH02	SB_REQ3B	AJ19	VSS	AL03	N.C.
AD01	SB_GNT3B	AH03	SB_REQ2B	AJ20	VSS	AL04	N.C.
AD02	SB_GNT2B	AH04	N.C.	AJ21	VSS	AL05	N.C.
AD03	SB_GNT1B	AH05	N.C.	AJ22	VSS	AL06	N.C.
AD04	N.C.	AH06	N.C.	AJ23	VAUX_DET	AL07	N.C.
AD05	VSS	AH07	VSS	AJ24	SMB_CLK	AL08	N.C.
AD06	VDD3.3	AH08	VDD1.5	AJ25	SA_SOL	AL09	N.C.
AD28	VDD3.3	AH09	TDI	AJ26	VSS	AL10	N.C.
AD29	VSS	AH10	VDD1.5	AJ27	SA_INTAB	AL11	N.C.
AD30	SA_PCLK0	AH11	VDD1.5	AJ28	N.C.	AL12	N.C.
AD31	SA_PCLK1	AH12	VDD1.5	AJ29	N.C.	AL13	N.C.
AD32	SA_PCLK2	AH13	VDD1.5	AJ30	N.C.	AL14	N.C.
AD33	SA_GNT2B	AH14	VDD1.5	AJ31	N.C.	AL15	N.C.
AE01	SB_GNT0B	AH15	AVDD1	AJ32	PX_REF133	AL16	N.C.
AE02	SB_PCLK3	AH16	AVSS1	AJ33	SA_PMEB	AL17	N.C.
AE03	SB_PCLK2	AH17	VDD1.5	AK01	SB_PMEB	AL18	N.C.
AE04	N.C.	AH18	VDD1.5	AK02	N.C.	AL19	N.C.
AE05	N.C.	AH19	VDD1.5	AK03	N.C.	AL20	N.C.
AE06	AVDD2	AH20	VDD1.5	AK04	N.C.	AL21	N.C.
AE28	N.C.	AH21	VDD1.5	AK05	SB_INTBB	AL22	N.C.
AE29	N.C.	AH22	VDD1.5	AK06	SB_SILB	AL23	N.C.
AE30	AVSS2	AH23	VDD1.5	AK07	SB_SORB	AL24	N.C.
AE31	N.C.	AH24	PE_WAKEB	AK08	TCK	AL25	N.C.
AE32	SA_PCLK3	AH25	VDD1.5	AK09	TRSTB	AL26	N.C.
AE33	SA_GNT3B	AH26	VSS	AK10	N.C.	AL27	N.C.
AF01	SB_PCLK1	AH27	N.C.	AK11	VDD1.5	AL28	N.C.
AF02	SB_PCLK0	AH28	N.C.	AK12	VSS	AL29	N.C.
AF03	AVSS2	AH29	N.C.	AK13	VDD1.5	AL30	N.C.
AF04	N.C.	AH30	SA_REQ0B	AK14	VSS	AL31	N.C.
AF05	VSS	AH31	SA_REQ1B	AK15	VDD1.5	AL32	N.C.
AF06	VDD1.5	AH32	SA_REQ2B	AK16	VSS	AL33	VSS
AF28	VDD1.5	AH33	SA_REQ3B	AK17	VSS	AM01	N.C.
AF29	AVSS2	AJ01	SB_REQ1B	AK18	VDD1.5	AM02	N.C.
AF30	AVDD2	AJ02	SB_REQ0B	AK19	VSS	AM03	ROSC_N8
AF31	AVDD2	AJ03	VSS	AK20	VSS	AM04	SB_INTCB
AF32	N.C.	AJ04	N.C.	AK21	VDD1.5	AM05	SB_SID
AF33	SA_PCLK4	AJ05	N.C.	AK22	VSS	AM06	SB_SOL
AG01	SB_PCLK4	AJ06	SB_INTAB	AK23	N.C.	AM07	EPR_CLK
AG02	AVSS2	AJ07	SB_SOC	AK24	RSM_PWRGD	AM08	PE_TX0N
AG03	SB_PCLK_I	AJ08	VSS	AK25	SMB_DAT	AM09	PE_TX1N
AG04	N.C.	AJ09	TDO	AK26	SA_SOD	AM10	PE_TX2N
AG05	VDD3.3	AJ10	VSS	AK27	SA_SID	AM11	PE_TX3N
AG06	N.C.	AJ11	VSS	AK28	SA_INTBB	AM12	PE_TX4N
AG28	VDD1.5	AJ12	VSS	AK29	ROSC_EN	AM13	PE_TX5N
AG29	VSS	AJ13	VSS	AK30	N.C.	AM14	PE_TX6N
AG30	N.C.	AJ14	VSS	AK31	N.C.	AM15	PE_TX7N
AG31	VDD3.3	AJ15	VSS	AK32	ROSC_N7	AM16	PE_REF100N
AG32	N.C.	AJ16	AVSS1	AK33	VDD3.3	AM17	N.C.
AG33	SA_PCLK_I	AJ17	VSS	AL01	N.C.	AM18	PE_RX0N

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PKG	NAME	PKG	NAME	PKG	NAME	PKG	NAME
AM19	PE_RX1N						
AM20	PE_RX2N						
AM21	PE_RX3N						
AM22	PE_RX4N						
AM23	PE_RX5N						
AM24	PE_RX6N						
AM25	PE_RX7N						
AM26	SMB_ALERTB						
AM27	SA_SOC						
AM28	SA_SIC						
AM29	SA_INTCB						
AM30	N.C.						
AM31	N.C.						
AM32	N.C.						
AM33	N.C.						
AN01	N.C.						
AN02	VDD3.3						
AN03	SB_INTDB						
AN04	SB_SIC						
AN05	SB_SOD						
AN06	EPR_DAT						
AN07	TMS						
AN08	PE_TX0P						
AN09	PE_TX1P						
AN10	PE_TX2P						
AN11	PE_TX3P						
AN12	PE_TX4P						
AN13	PE_TX5P						
AN14	PE_TX6P						
AN15	PE_TX7P						
AN16	PE_REF100P						
AN17	N.C.						
AN18	PE_RX0P						
AN19	PE_RX1P						
AN20	PE_RX2P						
AN21	PE_RX3P						
AN22	PE_RX4P						
AN23	PE_RX5P						
AN24	PE_RX6P						
AN25	PE_RX7P						
AN26	PWRGD						
AN27	SA_SORB						
AN28	SA_SILB						
AN29	SA_INTDB						
AN30	VDD3.3						
AN31	N.C.						
AN32	N.C.						
AN33	N.C.						

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3.2. Pin List (alphabetical order)

NAME	PKG	NAME	PKG	NAME	PKG	NAME	PKG
AVDD1	AH15	N.C.	D26	N.C.	W30	N.C.	AL12
AVDD2	AE06	N.C.	D27	N.C.	Y04	N.C.	AL13
AVDD2	AF30	N.C.	D29	N.C.	Y30	N.C.	AL14
AVDD2	AF31	N.C.	D30	N.C.	AA05	N.C.	AL15
AVDD2	AH01	N.C.	E02	N.C.	AA30	N.C.	AL16
AVSS1	AH16	N.C.	E04	N.C.	AB04	N.C.	AL17
AVSS1	AJ16	N.C.	E05	N.C.	AC03	N.C.	AL18
AVSS2	AE30	N.C.	E06	N.C.	AC29	N.C.	AL19
AVSS2	AF03	N.C.	E09	N.C.	AD04	N.C.	AL20
AVSS2	AF29	N.C.	E13	N.C.	AE04	N.C.	AL21
AVSS2	AG02	N.C.	E15	N.C.	AE05	N.C.	AL22
CTRI	B06	N.C.	E23	N.C.	AE28	N.C.	AL23
DBT_MODE	D01	N.C.	E25	N.C.	AE29	N.C.	AL24
DC_TEST_MODE	F31	N.C.	E27	N.C.	AE31	N.C.	AL25
EPR_CLK	AM07	N.C.	E28	N.C.	AF04	N.C.	AL26
EPR_DAT	AN06	N.C.	E29	N.C.	AF32	N.C.	AL27
EPR_EN	A31	N.C.	E30	N.C.	AG04	N.C.	AL28
N.C.	A01	N.C.	F05	N.C.	AG06	N.C.	AL29
N.C.	A02	N.C.	F06	N.C.	AG30	N.C.	AL30
N.C.	A03	N.C.	F07	N.C.	AG32	N.C.	AL31
N.C.	A33	N.C.	F08	N.C.	AH04	N.C.	AL32
N.C.	B02	N.C.	F28	N.C.	AH05	N.C.	AM01
N.C.	B03	N.C.	F29	N.C.	AH06	N.C.	AM02
N.C.	B04	N.C.	G05	N.C.	AH27	N.C.	AM17
N.C.	B32	N.C.	G06	N.C.	AH28	N.C.	AM30
N.C.	B33	N.C.	G28	N.C.	AH29	N.C.	AM31
N.C.	C03	N.C.	G30	N.C.	AJ04	N.C.	AM32
N.C.	C04	N.C.	H30	N.C.	AJ05	N.C.	AM33
N.C.	C07	N.C.	J04	N.C.	AJ28	N.C.	AN01
N.C.	C09	N.C.	J05	N.C.	AJ29	N.C.	AN17
N.C.	C11	N.C.	J29	N.C.	AJ30	N.C.	AN31
N.C.	C30	N.C.	J30	N.C.	AJ31	N.C.	AN32
N.C.	C31	N.C.	K31	N.C.	AK02	N.C.	AN33
N.C.	C32	N.C.	L04	N.C.	AK03	PE_REF100N	AM16
N.C.	C33	N.C.	L30	N.C.	AK04	PE_REF100P	AN16
N.C.	D03	N.C.	M04	N.C.	AK10	PE_RX0N	AM18
N.C.	D04	N.C.	N04	N.C.	AK23	PE_RX0P	AN18
N.C.	D05	N.C.	N29	N.C.	AK30	PE_RX1N	AM19
N.C.	D07	N.C.	N30	N.C.	AK31	PE_RX1P	AN19
N.C.	D10	N.C.	P04	N.C.	AL01	PE_RX2N	AM20
N.C.	D12	N.C.	R04	N.C.	AL02	PE_RX2P	AN20
N.C.	D14	N.C.	R29	N.C.	AL03	PE_RX3N	AM21
N.C.	D16	N.C.	T04	N.C.	AL04	PE_RX3P	AN21
N.C.	D17	N.C.	T28	N.C.	AL05	PE_RX4N	AM22
N.C.	D18	N.C.	T30	N.C.	AL06	PE_RX4P	AN22
N.C.	D19	N.C.	U04	N.C.	AL07	PE_RX5N	AM23
N.C.	D20	N.C.	U31	N.C.	AL08	PE_RX5P	AN23
N.C.	D21	N.C.	V04	N.C.	AL09	PE_RX6N	AM24
N.C.	D22	N.C.	V30	N.C.	AL10	PE_RX6P	AN24
N.C.	D25	N.C.	W05	N.C.	AL11	PE_RX7N	AM25

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NAME	PKG	NAME	PKG	NAME	PKG	NAME	PKG
PE_RX7P	AN25	SA_AD23	C21	SA_DEVSELB	A24	SB_AD3	J01
PE_TX0N	AM08	SA_AD24	B20	SA_FRAMEB	A23	SB_AD4	J02
PE_TX0P	AN08	SA_AD25	C20	SA_GNT0B	AC31	SB_AD5	J03
PE_TX1N	AM09	SA_AD26	A19	SA_GNT1B	AC32	SB_AD6	H01
PE_TX1P	AN09	SA_AD27	B19	SA_GNT2B	AD33	SB_AD7	H02
PE_TX2N	AM10	SA_AD28	C19	SA_GNT3B	AE33	SB_AD8	H03
PE_TX2P	AN10	SA_AD29	A18	SA_HPCM0	B30	SB_AD9	G02
PE_TX3N	AM11	SA_AD30	B18	SA_HPCM1	C29	SB_AD10	F01
PE_TX3P	AN11	SA_AD31	C18	SA_INTAB	AJ27	SB_AD11	F02
PE_TX4N	AM12	SA_AD32	AC33	SA_INTBB	AK28	SB_AD12	E01
PE_TX4P	AN12	SA_AD33	AB33	SA_INTCB	AM29	SB_AD13	A06
PE_TX5N	AM13	SA_AD34	AB32	SA_INTDB	AN29	SB_AD14	B07
PE_TX5P	AN13	SA_AD35	AB31	SA_IRDYB	C24	SB_AD15	A07
PE_TX6N	AM14	SA_AD36	AB30	SA_LOCKB	B25	SB_AD16	C12
PE_TX6P	AN14	SA_AD37	AA33	SA_M66EN	F33	SB_AD17	A13
PE_TX7N	AM15	SA_AD38	AA32	SA_M66EN_O	F32	SB_AD18	B13
PE_TX7P	AN15	SA_AD39	AA31	SA_PAR	B28	SB_AD19	C13
PE_WAKEB	AH24	SA_AD40	Y33	SA_PAR64	M33	SB_AD20	D13
PWRGD	AN26	SA_AD41	Y32	SA_PCIXCAP_I	A26	SB_AD21	A14
PX_REF133	AJ32	SA_AD42	Y31	SA_PCIXCAP_P	A25	SB_AD22	B14
ROSC_EN	AK29	SA_AD43	W33	SA_PCLK_I	AG33	SB_AD23	C14
ROSC_N5	C02	SA_AD44	W32	SA_PCLK0	AD30	SB_AD24	B15
ROSC_N7	AK32	SA_AD45	W31	SA_PCLK1	AD31	SB_AD25	C15
ROSC_N8	AM03	SA_AD46	V33	SA_PCLK2	AD32	SB_AD26	A16
ROSC_N9	D31	SA_AD47	V32	SA_PCLK3	AE32	SB_AD27	B16
RSM_PWRGD	AK24	SA_AD48	V31	SA_PCLK4	AF33	SB_AD28	C16
SA_ACK64B	L32	SA_AD49	U33	SA_PERRB	C26	SB_AD29	A17
SA_AD0	K33	SA_AD50	U32	SA_PMEB	AJ33	SB_AD30	B17
SA_AD1	K32	SA_AD51	T33	SA_REQ0B	AH30	SB_AD31	C17
SA_AD2	J33	SA_AD52	T32	SA_REQ1B	AH31	SB_AD32	AC01
SA_AD3	J32	SA_AD53	T31	SA_REQ2B	AH32	SB_AD33	AC02
SA_AD4	J31	SA_AD54	R33	SA_REQ3B	AH33	SB_AD34	AB01
SA_AD5	H33	SA_AD55	R32	SA_REQ64B	L31	SB_AD35	AB02
SA_AD6	H32	SA_AD56	R31	SA_SERRB	B26	SB_AD36	AB03
SA_AD7	H31	SA_AD57	R30	SA_SIC	AM28	SB_AD37	AA01
SA_AD8	G32	SA_AD58	P33	SA_SID	AK27	SB_AD38	AA02
SA_AD9	G31	SA_AD59	P32	SA_SILB	AN28	SB_AD39	AA03
SA_AD10	E33	SA_AD60	P31	SA_SLOTM0	F30	SB_AD40	AA04
SA_AD11	A29	SA_AD61	N33	SA_SLOTM1	E31	SB_AD41	Y01
SA_AD12	A28	SA_AD62	N32	SA_SLOTM2	D32	SB_AD42	Y02
SA_AD13	C28	SA_AD63	N31	SA_SOC	AM27	SB_AD43	Y03
SA_AD14	A27	SA_CBE0B	G33	SA_SOD	AK26	SB_AD44	W01
SA_AD15	B27	SA_CBE1B	C27	SA_SOL	AJ25	SB_AD45	W02
SA_AD16	C23	SA_CBE2B	B23	SA_SORB	AN27	SB_AD46	W03
SA_AD17	D23	SA_CBE3B	A20	SA_STOPB	C25	SB_AD47	V01
SA_AD18	A22	SA_CBE4B	M32	SA_TRDYB	B24	SB_AD48	V02
SA_AD19	B22	SA_CBE5B	M31	SB_ACK64B	L03	SB_AD49	V03
SA_AD20	C22	SA_CBE6B	M30	SB_AD0	K01	SB_AD50	U01
SA_AD21	A21	SA_CBE7B	L33	SB_AD1	K02	SB_AD51	U02
SA_AD22	B21	SA_CLKM	A30	SB_AD2	K03	SB_AD52	U03

NAME	PKG	NAME	PKG	NAME	PKG	NAME	PKG
SB_AD53	T01	SB_REQ2B	AH03	VDD1.5	T06	VDD3.3	J06
SB_AD54	T02	SB_REQ3B	AH02	VDD1.5	U30	VDD3.3	K06
SB_AD55	T03	SB_REQ64B	L02	VDD1.5	W04	VDD3.3	K28
SB_AD56	R01	SB_SERRB	A08	VDD1.5	Y28	VDD3.3	L06
SB_AD57	R02	SB_SIC	AN04	VDD1.5	AA06	VDD3.3	L28
SB_AD58	R03	SB_SID	AM05	VDD1.5	AB28	VDD3.3	M28
SB_AD59	P01	SB_SILB	AK06	VDD1.5	AC04	VDD3.3	N06
SB_AD60	P02	SB_SLOTM0	E07	VDD1.5	AC30	VDD3.3	P28
SB_AD61	P03	SB_SLOTM1	C06	VDD1.5	AF06	VDD3.3	R06
SB_AD62	N01	SB_SLOTM2	B05	VDD1.5	AF28	VDD3.3	R28
SB_AD63	N02	SB_SOC	AJ07	VDD1.5	AG28	VDD3.3	U06
SB_CBE0B	G01	SB_SOD	AN05	VDD1.5	AH08	VDD3.3	U28
SB_CBE1B	C08	SB_SOL	AM06	VDD1.5	AH10	VDD3.3	V06
SB_CBE2B	B12	SB_SORB	AK07	VDD1.5	AH11	VDD3.3	V28
SB_CBE3B	A15	SB_STOPB	B10	VDD1.5	AH12	VDD3.3	W06
SB_CBE4B	M01	SB_TRDYB	A11	VDD1.5	AH13	VDD3.3	W28
SB_CBE5B	M02	SD_TESTEN	D06	VDD1.5	AH14	VDD3.3	Y06
SB_CBE6B	M03	SMB_ADD0	C01	VDD1.5	AH17	VDD3.3	AA28
SB_CBE7B	L01	SMB_ADD1	D02	VDD1.5	AH18	VDD3.3	AB06
SB_CLKM	A05	SMB_ADD2	E03	VDD1.5	AH19	VDD3.3	AC06
SB_DEVSELB	C10	SMB_ADD3	F03	VDD1.5	AH20	VDD3.3	AC28
SB_FRAMEB	A12	SMB_ADD4	F04	VDD1.5	AH21	VDD3.3	AD06
SB_GNT0B	AE01	SMB_ALERTB	AM26	VDD1.5	AH22	VDD3.3	AD28
SB_GNT1B	AD03	SMB_CLK	AJ24	VDD1.5	AH23	VDD3.3	AG05
SB_GNT2B	AD02	SMB_DAT	AK25	VDD1.5	AH25	VDD3.3	AG31
SB_GNT3B	AD01	TCK	AK08	VDD1.5	AK11	VDD3.3	AK33
SB_HPCM0	D28	TDI	AH09	VDD1.5	AK13	VDD3.3	AN02
SB_HPCM1	B29	TDO	AJ09	VDD1.5	AK15	VDD3.3	AN30
SB_INTAB	AJ06	TMC1	D33	VDD1.5	AK18	VSS	B01
SB_INTBB	AK05	TMC2	E32	VDD1.5	AK21	VSS	E08
SB_INTCB	AM04	TMS	AN07	VDD3.3	A04	VSS	E10
SB_INTDB	AN03	TRSTB	AK09	VDD3.3	A32	VSS	E11
SB_IRDYB	B11	VAUX_DET	AJ23	VDD3.3	B31	VSS	E12
SB_LOCKB	B09	VDD1.5	D09	VDD3.3	C05	VSS	E14
SB_M66EN	G03	VDD1.5	D11	VDD3.3	F09	VSS	E16
SB_M66EN_O	G04	VDD1.5	D15	VDD3.3	F10	VSS	E17
SB_PAR	B08	VDD1.5	D24	VDD3.3	F11	VSS	E18
SB_PAR64	N03	VDD1.5	F13	VDD3.3	F12	VSS	E19
SB_PCIXCAP_I	A09	VDD1.5	F18	VDD3.3	F14	VSS	E20
SB_PCIXCAP_P	A10	VDD1.5	F20	VDD3.3	F15	VSS	E21
SB_PCLK_I	AG03	VDD1.5	F22	VDD3.3	F16	VSS	E22
SB_PCLK0	AF02	VDD1.5	F26	VDD3.3	F17	VSS	E24
SB_PCLK1	AF01	VDD1.5	H04	VDD3.3	F19	VSS	E26
SB_PCLK2	AE03	VDD1.5	J28	VDD3.3	F21	VSS	G29
SB_PCLK3	AE02	VDD1.5	K04	VDD3.3	F23	VSS	H05
SB_PCLK4	AG01	VDD1.5	K30	VDD3.3	F24	VSS	H29
SB_PERRB	D08	VDD1.5	M06	VDD3.3	F25	VSS	K05
SB_PMEB	AK01	VDD1.5	N28	VDD3.3	F27	VSS	K29
SB_REQ0B	AJ02	VDD1.5	P06	VDD3.3	H06	VSS	L05
SB_REQ1B	AJ01	VDD1.5	P30	VDD3.3	H28	VSS	L29

NAME	PKG	NAME	PKG	NAME	PKG	NAME	PKG
VSS	M05						
VSS	M29						
VSS	N05						
VSS	P05						
VSS	P29						
VSS	R05						
VSS	T05						
VSS	T29						
VSS	U05						
VSS	U29						
VSS	V05						
VSS	V29						
VSS	W29						
VSS	Y05						
VSS	Y29						
VSS	AA29						
VSS	AB05						
VSS	AB29						
VSS	AC05						
VSS	AD05						
VSS	AD29						
VSS	AF05						
VSS	AG29						
VSS	AH07						
VSS	AH26						
VSS	AJ03						
VSS	AJ08						
VSS	AJ10						
VSS	AJ11						
VSS	AJ12						
VSS	AJ13						
VSS	AJ14						
VSS	AJ15						
VSS	AJ17						
VSS	AJ18						
VSS	AJ19						
VSS	AJ20						
VSS	AJ21						
VSS	AJ22						
VSS	AJ26						
VSS	AK12						
VSS	AK14						
VSS	AK16						
VSS	AK17						
VSS	AK19						
VSS	AK20						
VSS	AK22						
VSS	AL33						

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4. Pin Functions

Pin functions are described below. Pin direction types are classified as power, I (Input), O (Output), O 3State (3State Type Output), OD (Nch Open Drain Type Output), I/O (bi-directional), and I/OD (bi-directional/Nch Open Drain Type Output).

4.1. Power supply

Pin	I/O	Buffer Type	Active Level	Function
VDD3.3	Power			+3.3 V power supply
VDD1.5	Power			+1.5 V power supply
AVDD1	Power			+1.5 V power supply for PCI Express PLL circuit
AVDD2	Power			+1.5 V power supply for PCI/PCI-X Skew Control PLL circuit
VSS	Power			Ground
AVSS1	Power			Ground for PCI Express PLL circuit
AVSS2	Power			Ground for PCI/PCI-X Skew Control PLL circuit

4.2. PCI Express Interface

Pin	I/O	Buffer Type	Active Level	Function
PE_TX (0 : 7)P	O	PCI Express Driver		PCI Express Transmit Data (Positive polarity signal of differential pair)
PE_TX (0 : 7)N	O	PCI Express Driver		PCI Express Transmit Data (Negative polarity signal of differential pair)
PE_RX (0 : 7)P	I	PCI Express Receiver		PCI Express Receive Data (Positive polarity signal of differential pair)
PE_RX (0 : 7)N	I	PCI Express Receiver		PCI Express Receive Data (Negative polarity signal of differential pair)
PE_REF100P	I	PCI Express Reference Clock		PCI Express 100MHz Reference Clock (Positive polarity signal of differential pair)
PE_REF100N	I	PCI Express Reference Clock		PCI Express 100MHz Reference Clock (Negative polarity signal of differential pair)
PE_WAKEB	OD	Nch Open Drain Output	Low	PCI Express “WAKE#” signal

4.3. PCI/PCI-X Interface

(PCI/PCI-X Port A)

Pin	I/O	Buffer Type	Active Level	Function
SA_AD (63 : 0)	I/O	PCI-X I/O		PCI /PCI-X “AD [63 : 0]” signal
SA_CBE (7 : 0)B	I/O	PCI-X I/O		PCI/PCI-X “C/BE [7 : 0]” signal
SA_PAR	I/O	PCI-X I/O		PCI/PCI-X “PAR” signal
SA_PAR64	I/O	PCI-X I/O		PCI/PCI-X “PAR64” signal
SA_FRAMEB	I/O	PCI-X I/O	Low	PCI/PCI-X “FRAME#” signal

Pin	I/O	Buffer Type	Active Level	Function
SA_IRDYB	I/O	PCI-X I/O	Low	PCI/PCI-X “IRDY#” signal
SA_TRDYB	I/O	PCI-X I/O	Low	PCI/PCI-X “TRDY#” signal
SA_STOPB	I/O	PCI-X I/O	Low	PCI/PCI-X “STOP#” signal
SA_DEVSELB	I/O	PCI-X I/O	Low	PCI/PCI-X “DEVSEL#” signal
SA_REQ (3 : 0)B	I	Input	Low	PCI/PCI-X “REQ#” signal (Note) SA_REQ3B is used as Attention Button Depress Input in SHPC Parallel mode. 0b: Attention Button depressed 1b: Attention Button not depressed
SA_GNT (3 : 0)B	O 3State	3-State Output	Low	PCI/PCI-X “GNT#” signal (Note) SA_GNT3B is used as Power LED Control output in SHPC Parallel mode. 0b: Power LED off 1b: Power LED on
SA_PERRB	I/O	PCI-X I/O	Low	PCI/PCI-X “PERR#” signal
SA_SERRB	I	Input	Low	PCI/PCI-X “SERR#” signal
SA_LOCKB	I/O	PCI-X I/O	Low	PCI/PCI-X “LOCK#” signal
SA_REQ64B	I/O	PCI-X I/O	Low	PCI/PCI-X “REQ64#” signal
SA_ACK64B	I/O	PCI-X I/O	Low	PCI/PCI-X “ACK64#” signal
SA_INTAB	I	Input	Low	PCI/PCI-X “INTA#” signal
SA_INTBB	I	Input	Low	PCI/PCI-X “INTB#” signal
SA_INTCB	I	Input	Low	PCI/PCI-X “INTC#” signal
SA_INTDB	I	Input	Low	PCI/PCI-X “INTD#” signal
SA_PMEB	I	Input	Low	PCI/PCI-X “PME#” signal
SA_M66EN	I	Input		PCI/PCI-X “M66EN” signal
SA_M66EN_O	O 3State	3-State Output		PCI/PCI-X M66EN Low Clamp
SA_PCIXCAP_I	I	Input		PCI/PCI-X “PCIXCAP” signal
SA_PCIXCAP_P	O 3State	3-State Output		PCI/PCI-X PCIXCAP Low-impedance High Drive
SA_PCLK (4 : 0)	O	Output		PCI/PCI-X “CLK” signal SA_PCLK4 must be connected to SA_PCLK_I to make a feedback loop of PCI/PCI-X PLL.
SA_PCLK_I	I	Input		PCI/PCI-X Feedback Clock

(PCI/PCI-X Port B)

Pin	I/O	Buffer Type	Active Level	Function
SB_AD (63 : 0)	I/O	PCI-X I/O		PCI /PCI-X “AD [63 : 0]” signal
SB_CBE (7 : 0)B	I/O	PCI-X I/O		PCI/PCI-X “C/BE [7 : 0]” signal
SB_PAR	I/O	PCI-X I/O		PCI/PCI-X “PAR” signal
SB_PAR64	I/O	PCI-X I/O		PCI/PCI-X “PAR64” signal
SB_FRAMEB	I/O	PCI-X I/O	Low	PCI/PCI-X “FRAME#” signal

Pin	I/O	Buffer Type	Active Level	Function
SB_IRDYB	I/O	PCI-X I/O	Low	PCI/PCI-X “IRDY#” signal
SB_TRDYB	I/O	PCI-X I/O	Low	PCI/PCI-X “TRDY#” signal
SB_STOPB	I/O	PCI-X I/O	Low	PCI/PCI-X “STOP#” signal
SB_DEVSELB	I/O	PCI-X I/O	Low	PCI/PCI-X “DEVSEL#” signal
SB_REQ (3 : 0)B	I	Input	Low	PCI/PCI-X “REQ#” signal (Note) SB_REQ3B is used as Attention Button Depress Input in SHPC Parallel mode. 0b: Attention Button depressed 1b: Attention Button not depressed
SB_GNT (3 : 0)B	O 3State	3-State Output	Low	PCI/PCI-X “GNT#” signal (Note) SB_GNT3B is used as Power LED Control output in SHPC Parallel mode. 0b: Power LED off 1b: Power LED on
SB_PERRB	I/O	PCI-X I/O	Low	PCI/PCI-X “PERR#” signal
SB_SERRB	I	Input	Low	PCI/PCI-X “SERR#” signal
SB_LOCKB	I/O	PCI-X I/O	Low	PCI/PCI-X “LOCK#” signal
SB_REQ64B	I/O	PCI-X I/O	Low	PCI/PCI-X “REQ64#” signal
SB_ACK64B	I/O	PCI-X I/O	Low	PCI/PCI-X “ACK64#” signal
SB_INTAB	I	Input	Low	PCI/PCI-X “INTA#” signal
SB_INTBB	I	Input	Low	PCI/PCI-X “INTB#” signal
SB_INTCB	I	Input	Low	PCI/PCI-X “INTC#” signal
SB_INTDB	I	Input	Low	PCI/PCI-X “INTD#” signal
SB_PMEB	I	Input	Low	PCI/PCI-X “PME#” signal
SB_M66EN	I	Input		PCI/PCI-X “M66EN” signal
SB_M66EN_O	O 3State	3-State Output		PCI/PCI-X M66EN Low Clamp
SB_PCIXCAP_I	I	Input		PCI/PCI-X “PCIXCAP” signal
SB_PCIXCAP_P	O 3State	3-State Output		PCI/PCI-X PCIXCAP Low-impedance High Drive
SB_PCLK (4 : 0)	O	Output		PCI/PCI-X “CLK” signal SB_PCLK4 must be connected to SB_PCLK_I to make a feedback loop of PCI/PCI-X PLL.
SB_PCLK_I	I	Input		PCI/PCI-X Feedback Clock

4.4. System clock & Reset interface

Pin	I/O	Buffer Type	Active Level	Function
PX_REF133	I	Input with 50 kΩ Pull down R		133MHz PCI-X reference clock provided by system clock input or oscillator input
PWRGD	I	Schmitt Trigger Input	High	Power Good signal
RSM_PWRGD	I	Schmitt Trigger Input	High	Resume Well Power Good signal

4.5. Hot Plug Controller interface

(PCI/PCI-X Port A)

Pin	I/O	Buffer Type	Active Level	Function
SA_SIC	I/O	I/O		(SHPC Serial-mode) Shift-in Clock output signal (SHPC Parallel-mode) Power Fault Status input signal 0b: Power Fault happened 1b: Power Fault not happened (Non-SHPC mode) Not used
SA_SID	I	Input		(SHPC Serial-mode) Shift-in Data input signal (SHPC Parallel-mode) MRL Sensor Status input signal 0b: MRL closed 1b: MRL opened (Non-SHPC mode) Not used
SA_SILB	O	Output		(SHPC Serial-mode) Shift-in Load control output signal. Active Low. (SHPC Parallel-mode) PCI/PCI-X RST# output signal. Active Low. (Non-SHPC mode) PCI/PCI-X RST# output signal
SA_SOC	I/O	I/O		(SHPC Serial-mode) Shift-out Clock output signal (SHPC Parallel-mode or Non-SHPC mode) PCI/PCI-X PRSNT1# input signal
SA_SOD	O	Output		(SHPC Serial-mode) Shift-out Data output signal (SHPC Parallel-mode) Power Enable Control output signal 0b: Power off 1b: Power on (Non-SHPC mode) Not used

Pin	I/O	Buffer Type	Active Level	Function
SA_SOL	O	Output		(SHPC Serial-mode) Shift-out Load Control output signal. Active Low. (SHPC Parallel-mode) Attention LED Control output signal 0b: Attention LED off 1b: Attention LED on (Non-SHPC mode) Not used
SA_SORB	I/O	I/O		(SHPC Serial-mode) Shift-out Reset Control output signal 0b: Reset Shift-out Registers 1b: Not reset Shift-out Registers (SHPC Parallel-mode or Non-SHPC mode) PCI/PCI-X PRSNT2# input signal

(NOTE) SA_REQ3B is used as Attention Button Depress Input in SHPC Parallel mode.

SA_GNT3B is used as Power LED Control Output in SHPC Parallel mode.

(PCI/PCI-X Port B)

Pin	I/O	Buffer Type	Active Level	Function
SB_SIC	I/O	IO		(SHPC Serial-mode) Shift-in Clock output signal (SHPC Parallel-mode) 0b: Power Fault happened 1b: Power Fault not happened Power Fault Status input signal (Non-SHPC mode) Not used
SB_SID	I	Input		(SHPC Serial-mode) Shift-in Data input signal (SHPC Parallel-mode) MRL Sensor Status input signal 0b: MRL closed 1b: MRL opened (Non-SHPC mode) Not used

Pin	I/O	Buffer Type	Active Level	Function
SB_SILB	O	Output		(SHPC Serial-mode) Shift-in Load control output signal. Active Low. (SHPC Parallel-mode) PCI/PCI-X RST# output signal. Active Low. (Non-SHPC mode) PCI/PCI-X RST# output signal
SB_SOC	I/O	I/O		(SHPC Serial-mode) Shift-out Clock output signal (SHPC Parallel-mode or Non-SHPC mode) PCI/PCI-X PRSNT1# input signal
SB_SOD	O	Output		(SHPC Serial-mode) Shift-out Data output signal (SHPC Parallel-mode) Power Enable Control output signal 0b: Power off 1b: Power on (Non-SHPC mode) Not used
SB_SOL	O	Output		(SHPC Serial-mode) Shift-out Load Control output signal (SHPC Parallel-mode) Attention LED Control output signal 0b: Attention LED off 1b: Attention LED on (Non-SHPC mode) Not used
SB_SORB	I/O	I/O		(SHPC Serial-mode) Shift-out Reset Control output signal 0b: Reset Shift-out Registers 1b: Not reset Shift-out Registers (SHPC Parallel-mode or Non-SHPC mode) PCI/PCI-X PRSNT2# input signal

(NOTE) SB_REQ3B is used as Attention Button Depress Input in SHPC Parallel mode. 0b: Depressed, 1b: Not depressed

SB_GNT3B is used as Power LED Control Output in SHPC Parallel mode. 0b: LED off, 1b: LED on

4.6. System Interface

Pin	I/O	Buffer Type	Active Level	Function
VAUX_DET	I	Input	High	Vaux detect signal 0: Vaux not present 1: Vaux present
SMB_CLK	I	Schmitt Trigger Input with Failsafe		SMBus Clock signal
SMB_DAT	I/OD	I/O Nch Open Drain Output		SMBus Data signal
SMB_ALERTB	OD	Nch Open Drain Output		SMBus Alert# signal
EPR_CLK	O	Output		EEPROM Clock signal
EPR_DAT	I/OD	I/O Nch Open Drain Output		EEPROM Data signal

4.7. Strap-pin Signals

Pin	I/O	Buffer Type	Active Level	Function
SMB_ADD (4 : 0)	I	Input with 50 kΩ Pull down R		SMBus Slave Address (4:0)
SA_CLKM	I	Input with 50 kΩ Pull down R		PCI/PCI-X Port A Clock 100/133MHz mode 0: Maximum frequency is 133MHz 1: Maximum frequency is 100MHz
SA_SLOTM (2 : 0)	I	Input with 50 kΩ Pull down R		Port A Hot Plug Slot configuration 000: No Hot Plug Slot 001: One Hot Plug Slot 010: Two Hot Plug Slot 011: Three Hot Plug Slot 100: Four Hot Plug Slot Others: Reserved
SA_HPCM (1 : 0)	I	Input with 50 kΩ Pull down R		Port A SHPC Option support Bit0 0: MRL Sensor not support 1: MRL Sensor support Bit1 0: Attention button not support 1: Attention button support
SB_CLKM	I	Input with 50 kΩ Pull down R		PCI/PCI-X Port B Clock 100/133MHz mode 0: Maximum frequency is 133MHz 1: Maximum frequency is 100MHz
SB_SLOTM (2 : 0)	I	Input with 50 kΩ Pull down R		Port B Hot Plug Slot configuration 000: No Hot Plug Slot 001: One Hot Plug Slot 010: Two Hot Plug Slot 011: Three Hot Plug Slot 100: Four Hot Plug Slot Others: Reserved

Pin	I/O	Buffer Type	Active Level	Function
SB_HPCM (1 : 0)	I	Input with 50 kΩ Pull down R		Port B SHPC Option support Bit0 0: MRL Sensor not support 1: MRL Sensor support Bit1 0: Attention button not support 1: Attention button support
EPR_EN	I	Input with 50 kΩ Pull down R	High	EEPROM Enable mode 0: EEPROM data load disable 1: EEPROM data load enable

4.8. Test Signals

Pin	I/O	Buffer Type	Active Level	Function
TCK	I	Input with 50 kΩ Pull down R		JTAG Test Clock
TDI	I	Input with 50 kΩ Pull up R		JTAG Test Data Input
TDO	O	Output		JTAG Test Output
TMS	I	Input with 50 kΩ Pull up R		JTAG Test Mode Select
TRSTB	I	Input with 50 kΩ Pull up R	Low	JTAG Test Reset
CTRI	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
SD_TESTEN	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
DBT_MODE	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
DC_TEST_MODE	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
TMC1	I	Input with Pull down R	High	NEC Test. Should be left open on circuit board.
TMC2	I	Input with Pull down R	High	NEC Test. Should be left open on circuit board.
ROSC_EN	I	Input with Pull down R	High	NEC Test. Should be left open on circuit board.
ROSC_N5	O	Output		NEC Test. Should be left open on circuit board.
ROSC_N7	O	Output		NEC Test. Should be left open on circuit board.
ROSC_N8	O	Output		NEC Test. Should be left open on circuit board.
ROSC_N9	O	Output		NEC Test. Should be left open on circuit board.

4.9. No Connection

Pin	I/O	Buffer Type	Active Level	Function
N.C.				No Connection

5. Electrical characteristics

This section describes the electrical characteristics of μPD720400.

5.1. I/O Buffer List

Table 5-1 I/O Buffer List

Buffer Type	Signal Name
3.3V Input Buffer with 50KΩ Pull-Down	SMB_ADD (4:0), SA_CLKM, SA_SLOTM (2:0), SA_HPCM (1:0), SB_CLKM, SB_SLOTM (2:0), SB_HPCM (1:0), EPR_EN, TCK
3.3V Input Buffer with 50KΩ Pull-Up	TDI, TMS, TRSTB
3.3V Input Buffer	SA_SERRB, SA_M66EN, SA_PCIXCAP_I, SA_INTAB, SA_INTBB, SA_INTCB, SA_INTDB, SA_PMEB, SB_SERRB, SB_M66EN, SB_PCIXCAP_I, SB_INTAB, SB_INTBB, SB_INTCB, SB_INTDB, SB_PMEB, VAUX_DET, SA_SID, SB_SID
3.3V Schmitt Trigger Input Buffer	PWRGD, RSM_PWRGD
3.3V Schmitt Trigger Input Buffer with Fail Safe	SMB_CLK
3.3V 3mA Output Buffer	EPR_CLK
3.3V 6mA Output Buffer	SA_SOD, SA_SOL, SB_SOD, SB_SOL
3.3V 9mA Output Buffer	SA_SILB, SB_SILB, TDO
3.3V 24mA 3State Output Buffer	SA_M66EN_O, SA_PCIXCAP_P, SB_M66EN_O, SB_PCIXCAP_P
3.3V bi-directional Buffer 6mA Output	SA_SIC, SA_SOC, SA_SORB, SB_SIC, SB_SOC, SB_SORB
3.3V bi-directional Buffer 3mA Nch Open Drain Buffer	EPR_DAT
3.3V bi-directional Buffer 12mA Nch Open Drain Buffer	SMB_DAT
3.3V 3mA Nch Open Drain Buffer	PE_WAKEB, SMB_ALERTB
PCI/PCI-X 3.3V 24mA bi-directional Buffer	SA_AD (63:0), SA_CBE (7:0)B, SA_PAR, SA_PAR64, SA_FRAMEB, SA_IRDYB, SA_TRDYB, SA_STOPB, SA_DEVSELB, SA_PERRB, SA_LOCKB, SA_REQ64B, SA_ACK64B, SB_AD (63:0), SB_CBE (7:0)B, SB_PAR, SB_PAR64, SB_FRAMEB, SB_IRDYB, SB_TRDYB, SB_STOPB, SB_DEVSELB, SB_PERRB, SB_LOCKB, SB_REQ64B, SB_ACK64B
PCI/PCI-X 3.3V 24mA 3State Output Buffer	SA_GNT (3:0)B, SB_GNT (3:0)B
PCI/PCI-X 3.3V Input Buffer	SA_REQ (3:0)B, SB_REQ (3:0)B
PCI/PCI-X 3.3V 24mA Clock Output	SA_PCLK (4:0), SB_PCLK (4:0)
PCI/PCI-X 3.3V Feedback Clock Input	SA_PCLK_I, SB_PCLK_I
PCI-X 3.3V Reference Clock Input	PX_REF133
PCI Express Reference Clock Input	PE_REF100P, PE_REF100N
PCI Express Interface	PE_TX (0:7) P, PE_TX (0:7) N, PE_RX (0:7) P, PE_RX (0:7) N

5.2. Terminology

Table 5-2 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Table 5-3 Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage.

Table 5-4 Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

5.3. Absolute Maximum Ratings

Table 5-5 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	1.5V Power Supply	-0.5 to +2.0	V
		3.3V Power Supply	-0.5 to +4.6	
Input voltage, 1.5V buffer	V_I	$1.425\ V \le V_{DD} \le 1.575\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +2.0	V
Input voltage, 3.3V buffer	V_I	$3.135\ V \le V_{DD} \le 3.465\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +4.6	V
Output voltage, 1.5V buffer	V_O	$1.425\ V \le V_{DD} \le 1.575\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +2.0	V
Output voltage, 3.3V buffer	V_O	$3.135\ V \le V_{DD} \le 3.465\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +4.6	V
Storage temperature	T_{stg}		-65 to +150	°C

5.4. Recommended Operating Ranges

Table 5-6 Recommended Operating Ranges

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	V_{DD}	1.5V Power Supply	1.425	1.5	1.575	V
		3.3V Power Supply	3.135	3.3	3.465	
High-level input voltage	V_{IH}	3.3V input buffer	2.0		V_{DD}	V
Low-level input voltage	V_{IL}	3.3V input buffer	-0.5		0.8	V
Positive-Trigger input voltage	V_P	3.3V schmitt input	1.2		2.4	V
Negative-Trigger input voltage	V_N	3.3V schmitt input	0.6		1.8	V

5.5. DC Characteristics

Table 5-7 DC Characteristics (Pin Block other than PCI/PCI-X)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}		±10	μA
Output short circuit current	I_{OS} Note1			-250	mA
Low-level outpt voltage 3.3V Low-level outpt voltage	V_{OL}	I_{OL} = 0 mA		0.1	V
High-level outpt voltage 3.3V High-level outpt voltage	V_{OH}	I_{OH} = 0 mA	V_{DD}-0.1		V
Low-level outpt current 3.3V Low-level outpt current	I_{OL}				
3mA output buffer		V_{OL} = 0.4 V	3.0		mA
6mA output buffer		V_{OL} = 0.4 V	6.0		mA
9mA output buffer		V_{OL} = 0.4 V	9.0		mA
12mA output buffer		V_{OL} = 0.4 V	12.0		mA
24mA output buffer		V_{OL} = 0.4 V	24.0		mA
High-level outpt current 3.3V High-level outpt current	I_{OH}				
6mA output buffer		V_{OH} = 2.4 V	6.0		mA
9mA output buffer		V_{OH} = 2.4 V	9.0		mA
24mA output buffer		V_{OH} = 2.4 V	24.0		mA
Input leakage current 3.3V buffer	I_I	$V_I = V_{DD}$ or V_{SS}		±10	μA
3.3V buffer with 50k ohm PD		$V_I = V_{DD}$		175	μA
3.3V buffer with 50k ohm PU		$V_I = V_{SS}$		253	μA

Note 1: The output short circuit time is one second or less and is only for one pin on the LSI.

Table 5-8 DC Characteristics (PCI/PCI-X Interface Block)

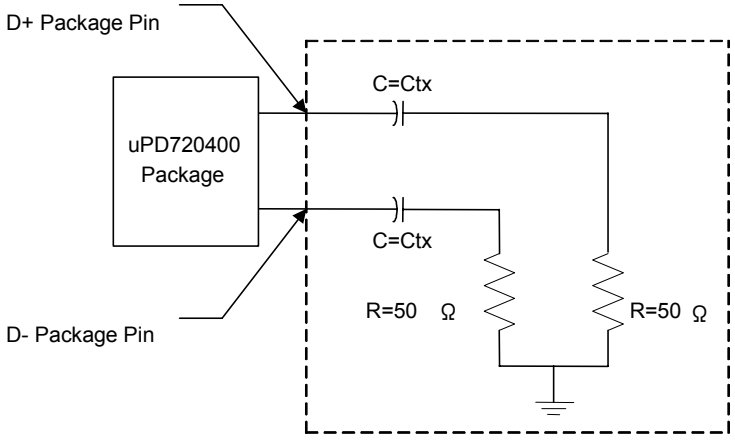
Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-level input voltage	V_{IH}		2.0	3.6	V
Low-level input voltage	V_{IL}		0	0.9	V
Low-level output voltage	V_{OL}	I_{OL} = 0 mA		0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0 mA	V_{DD} - 0.1		V
Low-level output current	I_{OL}	V_{OL} = 0.4 V	24.0		mA
High-level output current	I_{OH}	V_{OH} = 2.4 V	24.0		mA
Input low leakage current	I_{IL}	0 < Vin < 3.6 V		±10	μA

Table 5-9 DC Characteristics (PCI Express Interface Block)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Differential Transmitter (TX) Output					
Differential Peak to Peak Output Voltage	$V_{tx\text{-}diffpp}$		0.800	1.200	V

Parameter	Symbol	Condition	MIN.	MAX.	Unit
De-Emphasized Differential Output Voltage (Ratio)	$V_{tx\text{-}de\text{-}ratio}$		-3.0	-4.0	dB
Absolute Delta of DC Common Mode Voltage	$V_{tx\text{-}cm\text{-}dc\text{-}active\text{-}idle\text{-}delta}$	During L0 and Electrical Idle	0	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D-	$V_{tx\text{-}cm\text{-}dc\text{-}line\text{-}delta}$		0	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{tx\text{-}idle\text{-}diffp}$		0	20	mV
The amount of voltage change during Receiver Detection	$V_{tx\text{-}rcv\text{-}detect}$			600	mV
The TX DC Common Mode Voltage	$V_{tx\text{-}dc\text{-}cm}$		0	1.575	V
TX Short Circuit Current	$I_{tx\text{-}short}$			90	mA
DC Differential TX Impedance	$Z_{tx\text{-}diff\text{-}dc}$		80	120	Ω
Transmitter DC Impedance	$Z_{tx\text{-}dc}$		40		Ω
Differential Receiver (RX) Input					
Differential Input Peak to Peak Voltage	$V_{rx\text{-}diffpp}$		0.175	1.200	V
DC Differential Input Impedance	$Z_{rx\text{-}diff\text{-}dc}$		80	120	Ω
DC Input Impedance	$Z_{rx\text{-}dc}$		40	60	Ω
Powered Down DC Input Impedance	$Z_{rx\text{-}high\text{-}imp\text{-}dc}$		200K		Ω
Electrical Idle Detect Threshold	$V_{rx\text{-}idle\text{-}det\text{-}diffpp}$		65	175	mV

Figure 5-1 Transmitter Measurement Load



5.6. Pin Capacitance

Table 5-10 Pin Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	V_{DD} = 0 V, T_A = 25°C	3.82	6.14	pF
Output capacitance	C_O	f_c = 1 MHz	6.14	8.14	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	6.14	8.14	pF

5.7. Power Consumption and Thermal Spec

Table 5-11 Power Consumption and Thermal Spec

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VDD3.3 supply current	I_{DD} (3.3V)	PCIe x8 / PCI-X 2 ports		0.3	0.6	A
VDD1.5 supply current	I_{DD} (1.5V)			1.9	2.0	A
VDD3.3 supply current	I_{DD} (3.3V)	PCIe x4 / PCI-X 2 ports		0.3	0.6	A
VDD1.5 supply current	I_{DD} (1.5V)			1.5	1.6	A
VDD3.3 supply current	I_{DD} (3.3V)	PCIe x8 / PCI-X 1 port		0.2	0.3	A
VDD1.5 supply current	I_{DD} (1.5V)			1.7	1.8	A
VDD3.3 supply current	I_{DD} (3.3V)	PCIe x4 / PCI-X 1 port		0.2	0.3	A
VDD1.5 supply current	I_{DD} (1.5V)			1.3	1.5	A
Junction Temperature	T_j		0		115	°C
Thermal Resistance of case	θ_{jc}			2.50		°C/W
Thermal Resistance total	θ_{ja}	wv = 0 m/s *		19.96		°C/W
		wv = 0.2 m/s *		17.67		
		wv = 1.0 m/s *		14.50		
		wv = 2.0 m/s *		13.00		

(Note1) wv : wind velocity

(Note2) Recommended heat-sinks for uPD720400 are below.

ALPHA UB35-10B, UB35-25B (http://www.alphanovatech.com/c_ub35e.html)

(Note3) The formulas of the Tj calculation are below.

(1) Without heat-sink

$Tj = Power \times \theta_{ja} + Ta$

(2) With heat-sink

$Tj = Power \times (\theta_{jc} + \theta_{ch} + \theta_{ha}) + Ta$

Where

θ_{ch} is thermal resistance of adhesive. (like 0.5 °C /W)

θ_{ha} is thermal resistance of heat-sink.

5.8. System Clock Ratings

The characteristics for the PCI/PCI-X Reference Clock are described in Table 5-12. Regarding the characteristics for the PCI Express Reference Clock, μPD720400 is based on the PCI EXPRESS CARD ELECTROMECHANICAL SPECIFICATION. Please refer to the Section 2.1. of that specification.

Table 5-12 PCI/PCI-X Reference Clock

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CLK}		-500 ppm	133	+500 ppm	MHz
Clock Duty cycle	t_{DUTY}		45		55	%
Input rise time	T_r				2	ns
Input fall time	T_f				2	ns

5.9. AC Characteristics

Table 5-13 AC Characteristics (PCI/PCI-X Interface Block) 1/2

Parameter	Symbol	Conditions	MIN	MAX	Unit
PCI clock cycle time	t_{cyc}	PCI-X 133	7.5		ns
		PCI-X 66	15		
		Conventional PCI 66	15		
		Conventional PCI 33	30		
PCI clock pulse, high-level width	t_{high}	PCI-X 133	3		ns
		PCI-X 66	6		
		Conventional PCI 66	6		
		Conventional PCI 33	11		
PCI clock pulse, low-level width	t_{low}	PCI-X 133	3		ns
		PCI-X 66	6		
		Conventional PCI 66	6		
		Conventional PCI 33	11		
PCI clock, rise slew rate	S_{cr}	0.2 V_{DD} to 0.6 V_{DD}			V/ns
		PCI-X 133	1.5	4	
		PCI-X 66	1.5	4	
		Conventional PCI 66	1.5	4	
		Conventional PCI 33	1	4	
PCI clock, fall slew rate	S_{cf}	0.2 V_{DD} to 0.6 V_{DD}			V/ns
		PCI-X 133	1.5	4	
		PCI-X 66	1.5	4	
		Conventional PCI 66	1.5	4	
		Conventional PCI 33	1	4	
Delay from RSTB Low to CLK Frequency Change	T_{rlcx}		0		V/ns

Table 5-14 AC Characteristics (PCI/PCI-X Interface Block) 2/2

Parameter	Symbol	Conditions	MIN	MAX	Unit
PCI reset active time (vs. power supply stability)	t_{rst}		1		ms
PCI reset active time (vs. CLK Start)	$t_{rst-clk}$		100		μs
Output float delay time (vs. RSTB↓)	$t_{rst-off}$			40	ns
PCI reset rise slew rate	S_{rr}		50		mV/ns
PCI bus signal output time (vs. PCLK↑)	t_{val}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0.7	3.8	ns
PCI point-to-point signal output time (vs. PCLK↑)	t_{val} (ptp)	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0.7	3.8	ns
Output delay time (vs. PCLK↑)	t_{on}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	2		ns
Output float delay time (vs. PCLK↑)	t_{off}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33		7	ns
Input setup time (vs. PCLK↑)	t_{su}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	1.2		ns
Point-to-point input setup time (vs. PCLK↑)	t_{su} (ptp)	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	1.2		ns
Input hold time	t_h	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0		ns
REQ64B to RSTB Setup Time	t_{rrsu}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	10		Clock
RSTB to REQ64B Hold Time	t_{rrh}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0	50	ns
PCI-X Initialization Pattern to RSTB Setup Time	t_{prsu}		10		Clocks
RSTB to PCI Initialization Pattern Hold Time	t_{prh}		0	50	ns

Table 5-15 AC Characteristics (PCI Express Interface Block)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Differential Transmitter (TX) Output					
Unit Interval	UI		399.88	400.12	ps
Minimum TX Eye Width	T_{rx-eye}		0.70		UI
Maximum time between the jitter median and maximum deviation from the median	$T_{tx-eye-median-to-max-jitter}$			0.15	UI
D+/D- TX Output Rise/Fall Time	$T_{rx-rise}$, $T_{rx-fall}$		0.125		UI
AC Peak Common Mode Output Voltage	$V_{tx-cm-acp}$			20	mV
Minimum time spent in Electrical Idle	$T_{tx-idle-min}$		50		UI
Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle Ordered set	$T_{tx-idle-set-to-idle}$			20	UI
Lane-to-Lane Output Skew	$L_{tx-skew}$			500+2UI	ps
Differential Receiver (RX) Input					
Unit Interval	UI		399.88	400.12	ps
Minimum Receiver Eye Width	T_{rx-eye}		0.4		UI
Maximum time between the jitter median and maximum deviation from the median	$T_{rx-eye-median-to-max-jitter}$			0.3	UI
AC Peak Common Mode Input Voltage	$V_{rx-cm-acp}$			150	mV
Total Skew	$L_{rx-skew}$			20	ns

Figure 5-2 Minimum Transmitter Timing and Voltage

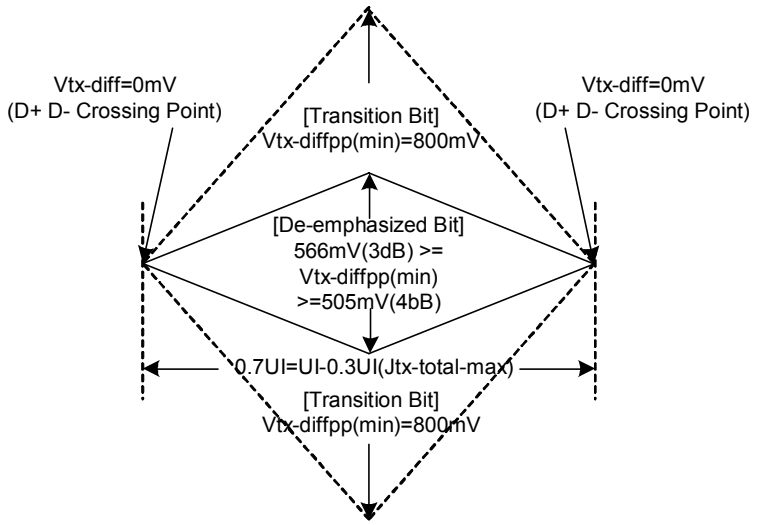


Figure 5-3 Transmitter Measurement Load

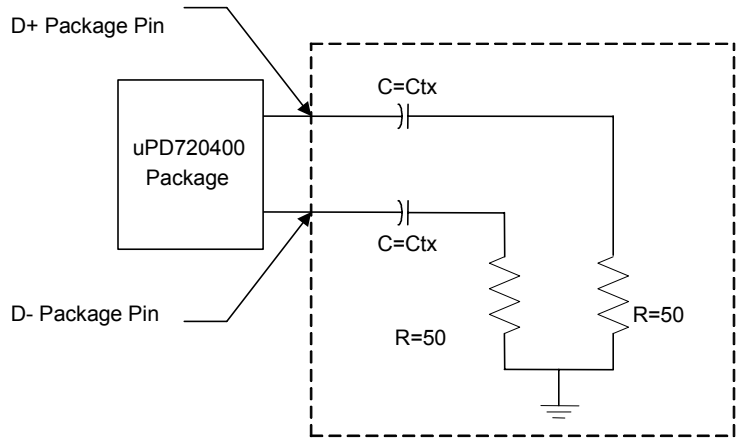


Figure 5-4 Minimum Receiver Timing and Voltage

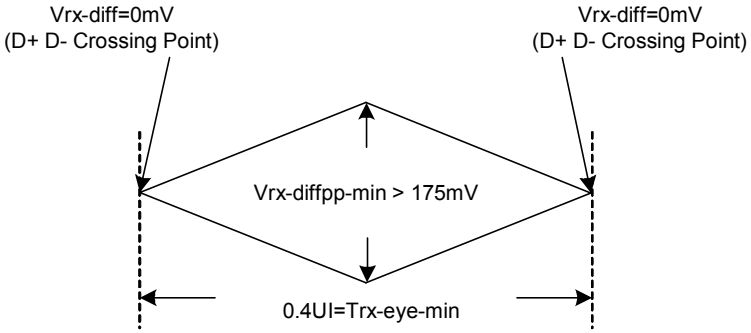


Table 5-16 AC Characteristics (SMBus Interface Block)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SMBus Operation Frequency	F_{smb}		10		400	KHz
Bus Free Time between STOP and START condition	T_{buf}		4.7			us
Hold Time after (Repeated) START condition.	$T_{hd:sta}$		4.0			us
Repeated START Condition setup time	$T_{su:sta}$		4.7			us
STOP condition setup time	$T_{su:sto}$		4.0			us
Data hold time	$T_{hd:dat}$		300			ns
Data setup time	$T_{su:dat}$		250			ns
Clock Low period	T_{low}		4.7			us
Clock High period	T_{high}		4.0		50	us
Clock/Data Fall time	T_f				300	ns
Clock/Data Rise time	T_r				1000	ns

Table 5-17 AC Characteristics (EEPROM Interface Block)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Frequency,EPR_CLK	F_{scl}				100	KHz
Clock Pulse Width Low	T_{low}		4.7			us
Clock Pulse Width High	T_{high}		4.7			us
Clock Low to Data Out Valid	T_{aa}		2.5		2.8	us
START Hold time	$T_{hd:sta}$		4.0			us
START Setup time	$T_{su:sta}$		4.7			us
Data In Hold time	$T_{hd:dat}$		0			us
Data In Setup time	$T_{su:dat}$		0			us
Inputs Rise time	T_r				1000	ns
Inputs Fall time	T_f				300	ns
Stop Setup time	$T_{su:sto}$		4.7			ns
Data Out Hold time	T_{dh}		2.5			ns

Table 5-18 AC Characteristics (Hot-Plug External Shift-IN Register)

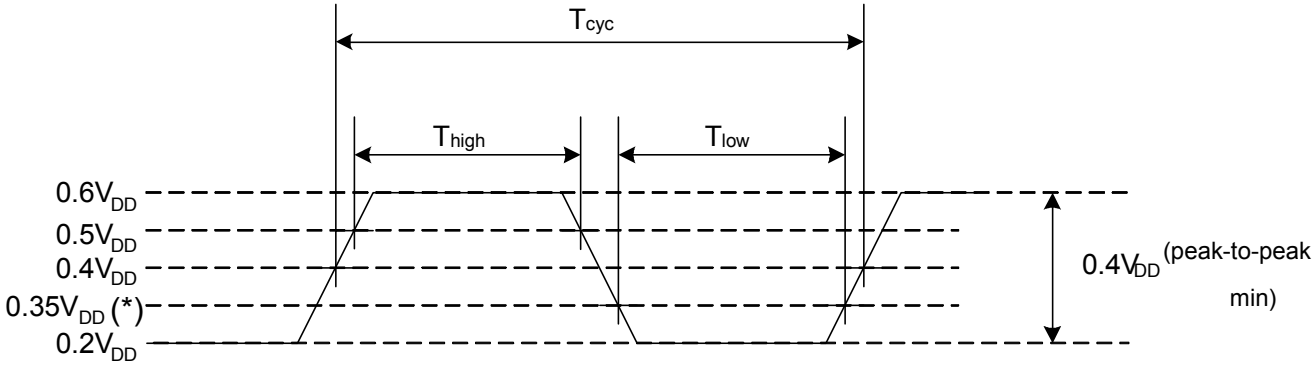
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Frequency, Sx_SIC	F_{sic}				12.5	MHz
Clock Pulse Width Low	T_{low}		40			ns
Clock Pulse Width High	T_{high}		40			ns
Load Pulse Width Low	$T_{low:load}$		40			ns
Load fall to Clock rise	T_{load}		80			ns
Rise Time	T_r				10	ns
Fall Time	T_f				10	ns
Input Data Setup time	T_{su}		10			ns
Input Data Hold time	T_{hd}		0			ns

Table 5-19 AC Characteristics (Hot-Plug External Shift-OUT Register)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Frequency, Sx_SOC	F_{soc}				12.5	MHz
Clock Pulse Width Low	T_{low}		40			ns
Clock Pulse Width High	T_{high}		40			ns
Reset Pulse Width Low	$T_{low:rst}$		40			ns
Load Pulse Width High	$T_{high:load}$		60			ns
Clock fall to Load reset	T_{load}		80			ns
Rise Time	T_r				10	ns
Fall Time	T_f				10	ns
Clock High to Data Output	T_{do}		40		50	ns

5.10. Timing Diagram

Figure 5-5 PCI/PCI-X Clock



(*) PCI-X. $0.3V_{DD}$ for Conventional PCI.

Figure 5-6 PCI/PCI-X Output Timing Measurement Timing

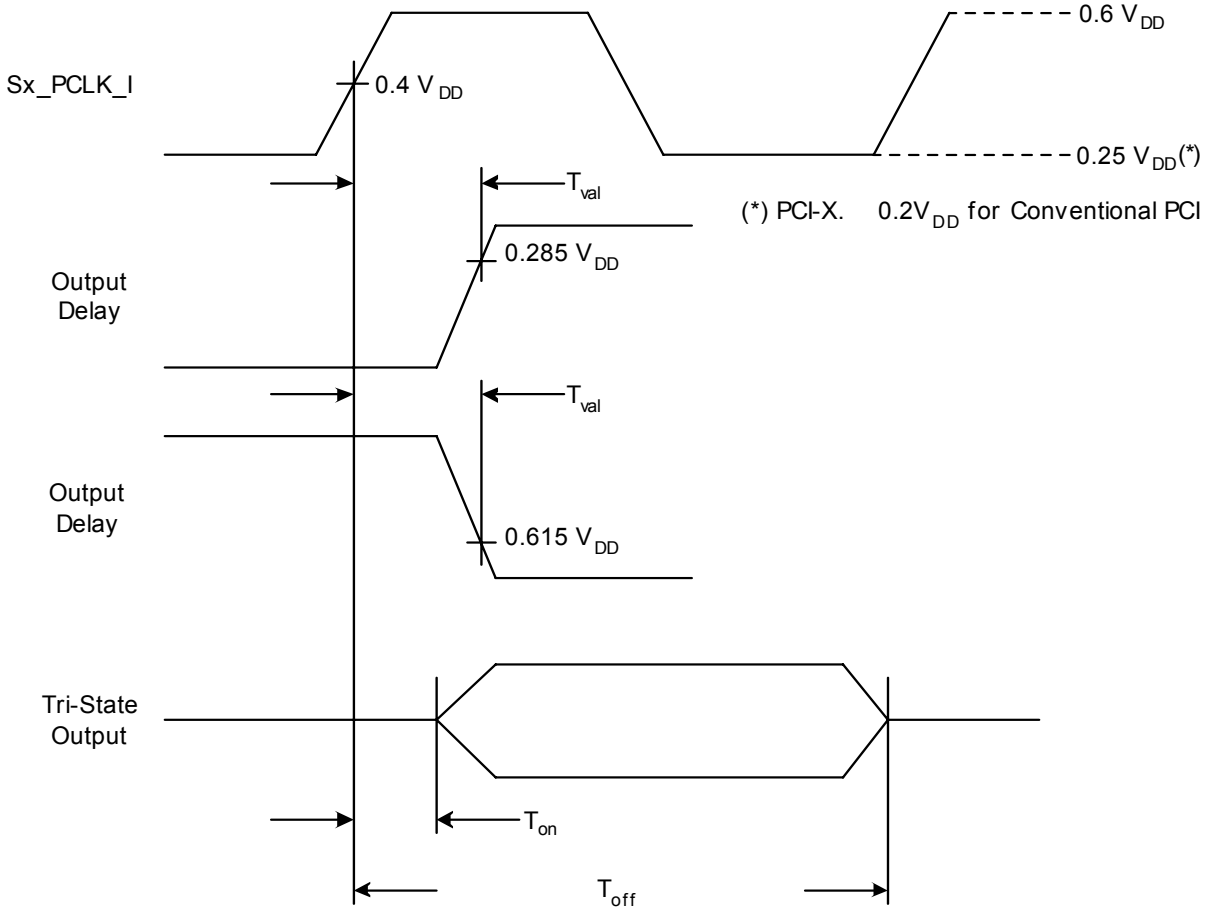
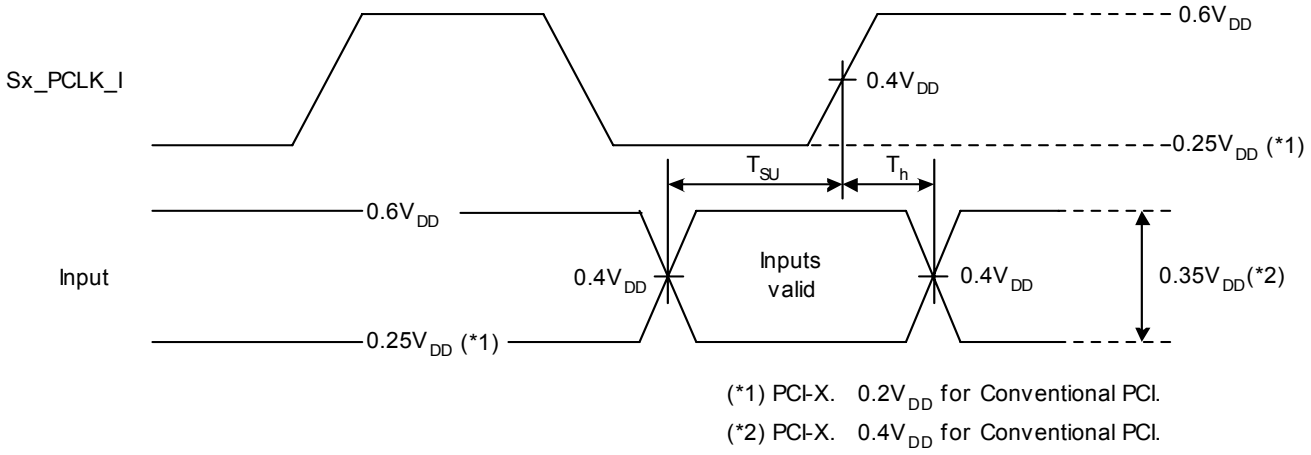


Figure 5-7 PCI/PCI-X Input Timing Measurement condition



(*1) PCI-X. $0.2V_{DD}$ for Conventional PCI.
(*2) PCI-X. $0.4V_{DD}$ for Conventional PCI.

Figure 5-8 SMBus Timing

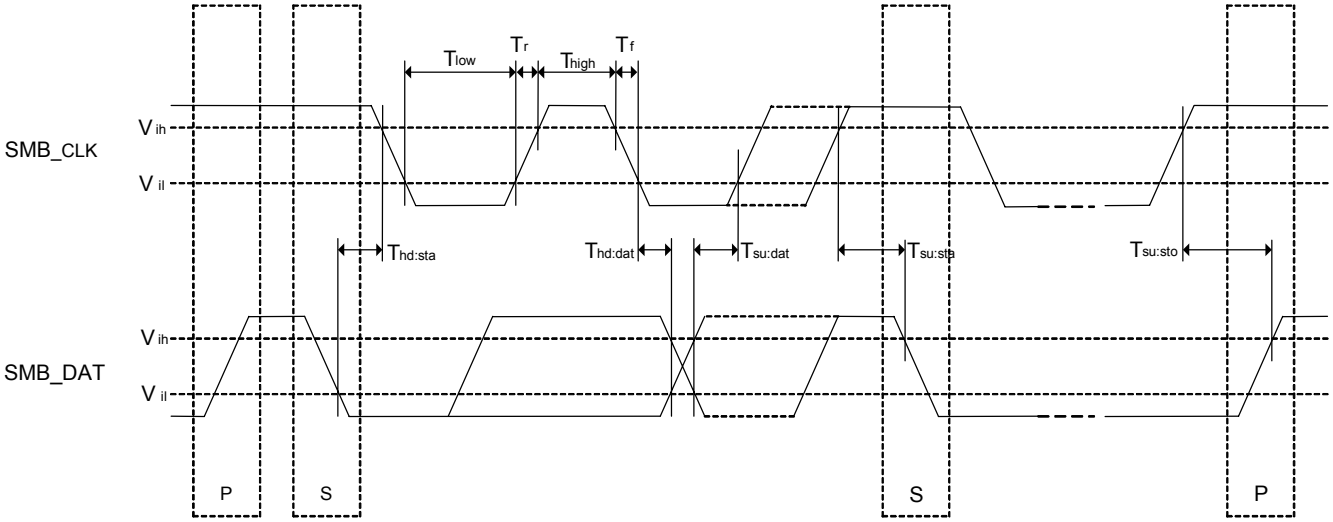


Figure 5-9 EEPROM Timing

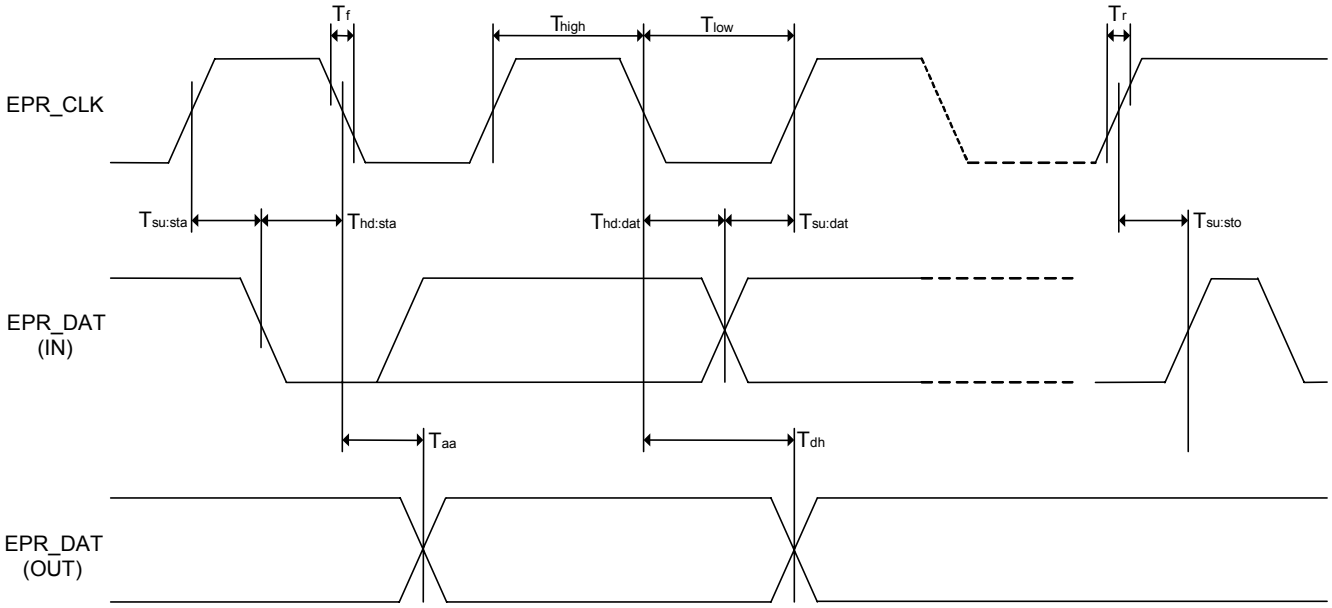


Figure 5-10 Hot-Plug SHIFT-IN Timing

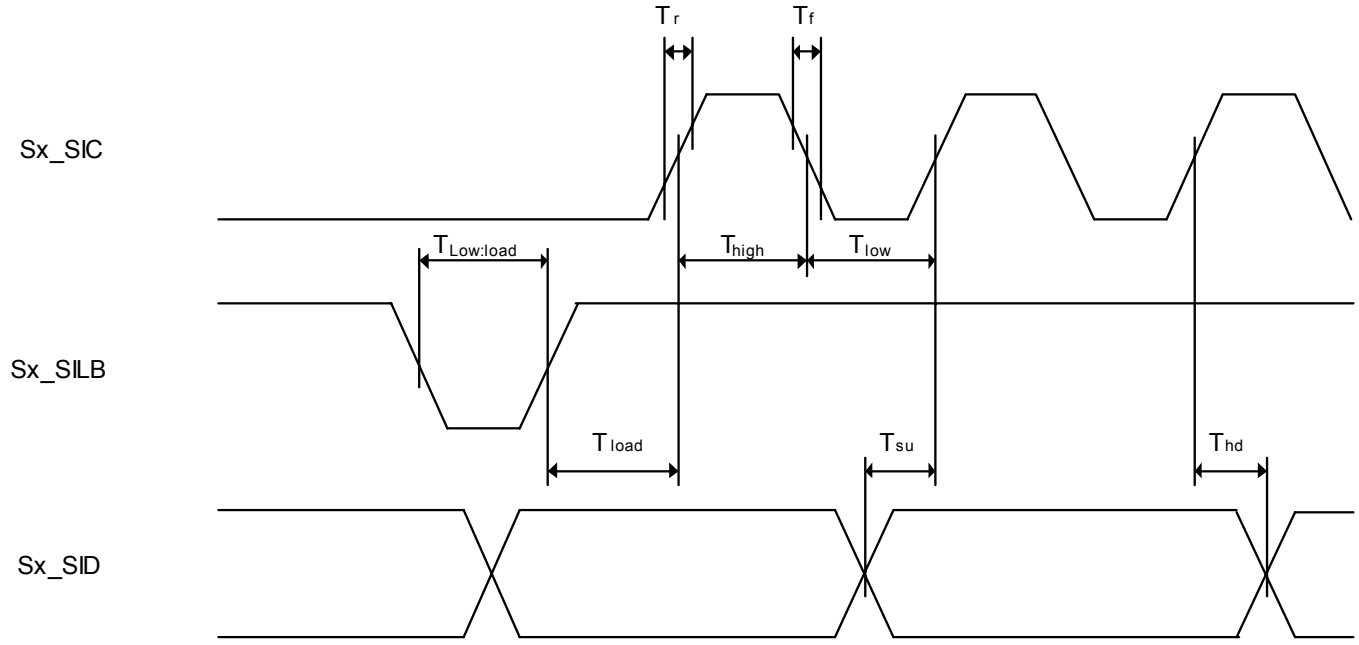


Figure 5-11 Hot-Plug SHIFT-OUT Timing