NEC

NEC Electronics Inc.

μPD72064
Floppy-Disk Controller

Preliminary Information

September 1990

Description

The μPD72064 FDC is NEC's highly integrated solution for PC/AT-type floppy-disk controller designs. Like its predecessor, the μPD72068, the μPD72064 maintains complete microcode compatibility with the industry standard μPD765 and contains the latest enhancements required for multitasking applications. Additionally, the μPD72064 provides the complete host-interface register set for PC/AT support.

The μPD72064 incorporates a high-performance digital PLL that is impervious to harmonic lock-on, a characteristic of analog counterparts. Being digital, the PLL requires no adjustments and supports all standard data rates.

The μPD72064 has on-chip clock generation, selectable write precompensation, and all the circuitry necessary for interfacing directly to four floppy-disk drives.

Features

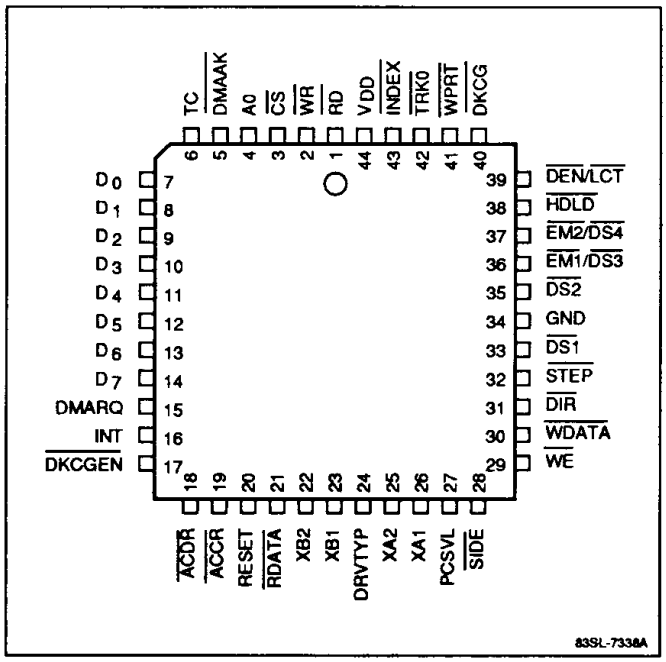
- Software compatible with μPD765A/B and μPD72065/65B
- Pinout compatible with WD37C65; uses 32-MHz and 19.2-MHz crystals
- IBM PC/AT compatible recording format
- On-chip peripheral circuits
  - —High-performance DPLL data separator
  - —Dual-circuit system clock generator
  - Host interface register for IBM PC/AT
  - —Write precompensator (programmable preshift)
- FDD interface
  - —High-current drivers (48-mA sink)
  - —Schmitt receivers
- Data transfer rates
  - —MFM: 500, 300, 250 kb/s
  - —FM: 250, 150, 125 kb/s
- Power saving standby mode (I_{DDI} = 100 μA maximum)
- One crystal for standard data rates: MFM 250, 500 kb/s
- Switches maximum step pulses (77/255) when recalibrating
- Controls up to four FDDs
- Dual-speed spindle motor control
- DMA or non-DMA data transfer from main system
- Multisector and multitrack transfer
- Programmable step rate and head load/unload time
- CMOS
- Single + 5-volt power supply

Ordering Information

Part Number	Package
μPD72064LM	44-pin PLCC
μPD72064GC-3B6	52-pin plastic QFP

Pin Configurations

44-Pin PLCC



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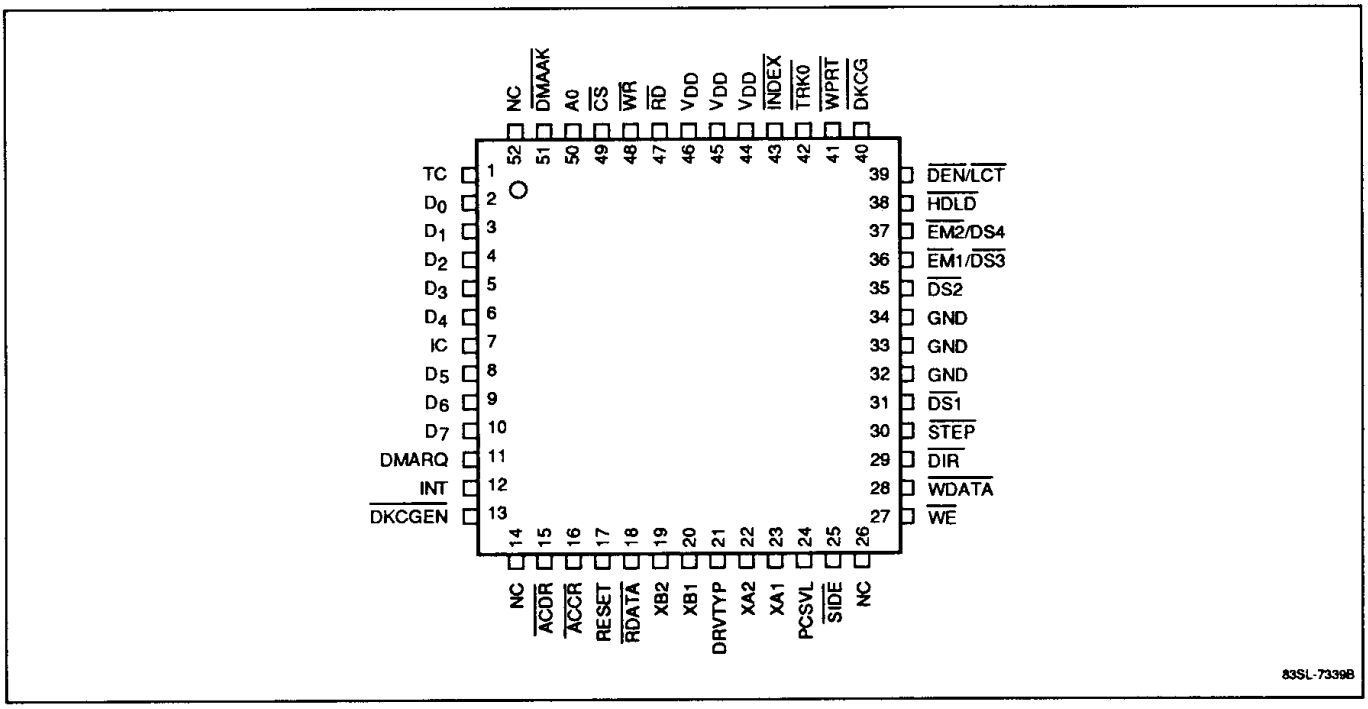
52-Pin Plastic QFP



Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects μPD72064 registers. A0 Registers 0 Status, auxiliary command 1 Data
$\overline{ACCR}$	In	Selects control register and digital input register when $\overline{ACCR}$ = 0.
$\overline{ACDR}$	In	Selects digital out register when $\overline{ACDR}$ = 0.
$\overline{CS}$	In	Chip Select. Allows $\overline{RD}$ and $\overline{WR}$ signals to be enabled.
D_0-D_7	I/O	Data Bus. Bidirectional, three-state data bus.
$\overline{DEN/LCT}$ (3)	Out	Density/Low Current. Base or special mode: Indicates the read/write heads are positioned on cylinder 43 or later. Please refer to table 8 for operation in PC/AT mode.
$\overline{DIR}$ (3)	Out	Specifies the seek direction. $\overline{DIR}$ Seek Direction 0 Centripetal 1 Centrifugal
$\overline{DKCG}$ (3)	In	Indicates drive status. $\overline{DKCG}$ = 0 means the drive latch is left unlocked (a medium may be exchanged or inserted).
$\overline{DKCGEN}$ (1)	In	Enables disk change signal ($\overline{DKCG}$).
$\overline{DMAAK}$	In	DMA Acknowledge. Enables DMA cycle.
DMARQ	Out	DMA Request. Requests data transfer in DMA mode.
DRVTYP	In	Allows a two-speed spindle motor to be used when DRVTYP = 1. Set this pin to 0 if the XB clock is not used.
$\overline{DS1}$, $\overline{DS2}$ (3)	Out	Selects a drive.
$\overline{EM1/DS3}$, $\overline{EM2/DS4}$ (3)	Out	PC/AT mode: Becomes $\overline{EM1}$, $\overline{EM2}$ to control the spindle motor. Base or special mode: Becomes $\overline{DS3}$, $\overline{DS4}$ to select a drive.
$\overline{HDLD}$ (3)	Out	Head Load. Places the read/write heads in the load state.
$\overline{INDEX}$ (2)	In	Indicates a read/write head is positioned at the physical start point of track on the medium.
INT	Out	Interrupt Request. Requests main system to process transferred data or execution results.
PCSVL	In	Sets the pre-shift value used when the transfer rate of 500/250 kb/s (MFM) is applied. PCSVL Pre-Shift Value 0 187 ns for cylinder 43 or later; 0 ns for cylinder 42 or earlier 1 125 ns

Pin Identification (cont)

Symbol	I/O	Signal Function
$\overline{RD}$	In	Read. Signal causes the main system to read data from the μPD72064 to the data bus.
$\overline{RDATA}$ (2)	In	Read data (consists of clock and data bits) from FDD.
RESET	In	Places the μPD72064 in the idle state. All pins on the drive side are in the high-impedance state. On the main system side, INT and DMARQ pins are in the floating state, and D_0-D_7 pins are in the input state.
$\overline{SIDE}$ (3)	Out	Selects read/write head 0 or 1 of the double-sided drive. SIDE Read/Write 0 Head 1 1 Head 0
$\overline{STEP}$ (3)	Out	Generates step pulses for the seek movement
TC	In	Terminal Count. Indicates data transfer is ended.
$\overline{TRK0}$ (2)	In	Indicates read/write heads are positioned at cylinder 0.
$\overline{WDATA}$ (3)	Out	Write data (clock and data bits) to FDD.
$\overline{WE}$ (3)	Out	Indicates write to the drive.
$\overline{WPRT}$ (2)	In	Indicates medium is write-protected.
$\overline{WR}$	In	Write. Control signal that allows the main system to write data bus data into the μPD72064.
XA1, XA2	In	Crystal A. For internal oscillator frequency control, a crystal resonator is connected to XA1 and XA2. For external clock input at XA1, XA2 is open. Frequency = 32 MHz
XB1, XB2	In	Crystal B. For internal oscillator frequency control, a crystal resonator is connected to XB1 and XB2. For external clock input at XB1, XB2 is open. Frequency = 19.2 MHz
IC		Internal Connection
NC	—	No Connection
GND	—	Ground
V_{DD}	In	+5-volt power supply

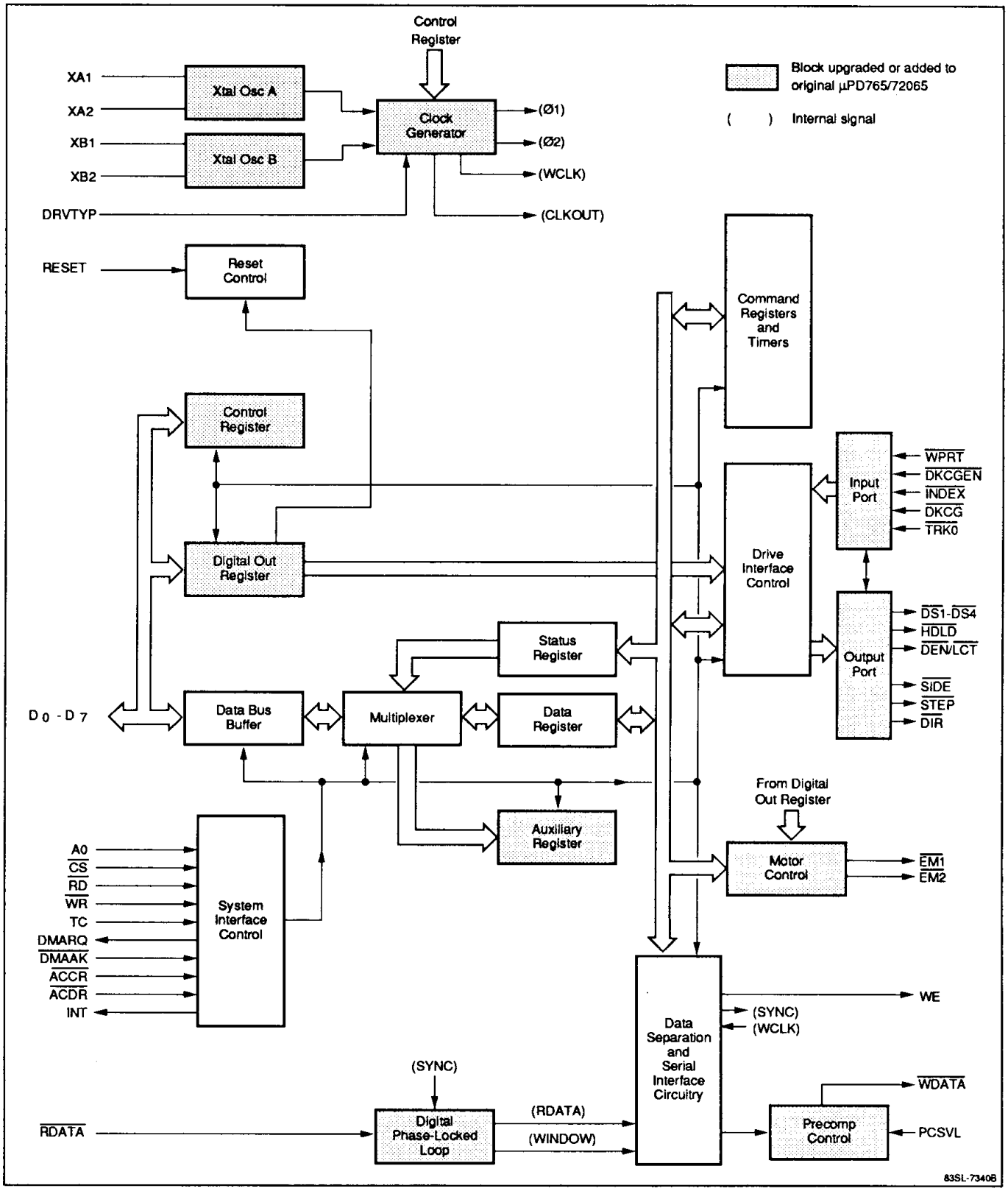
Notes:

(1) Internal pullup.

(2) Schmitt trigger input.

(3) High-current driver (48-mA sink current).

μPD72064 Block Diagram



REGISTERS

Table 1 describes the six 8-bit registers in the 72064 Floppy-Disk Controller (FDC) that interface with the main system.

Table 1. Registers

Name	Description
Data register	Temporarily stores information to be transferred between the FDC and the main system; for example, a command code, a parameter, data, or a result status.
Status register	Indicates FDC status; register can be read by the main system at any time.
Auxiliary command register	Temporarily stores a command for the FDC.
Digital out register	Selects mode (PC/AT or special), drive, motor control, software reset, and INT/DMARQ control.
Control register	Sets data transfer rate.
Digital input register	Indicates drive status ($\overline{DKCG}$).

Register Selection

As shown in table 2, the logic state of input pins A0, $\overline{CS}$, $\overline{ACDR}$, and $\overline{ACCR}$ selects a particular register. The state of input pins $\overline{WR}$ and $\overline{RD}$ selects register write or register read.

If the DMA acknowledge input ($\overline{DMAAK}$) is active, the data register will be selected regardless of the $\overline{CS}$ and A0 input states.

(1) $\overline{ACCR}$ or $\overline{ACDR}$ input will be held inactive.

(2) If both $\overline{CS}$ and A0 inputs are 0, the write of any code other than an auxiliary command code ($\overline{WR}$ = 0) will be inhibited.

Table 2. Register Selection

Operation	$\overline{WR}$	$\overline{RD}$	A0	$\overline{CS}$	$\overline{ACDR}$	$\overline{ACCR}$
Status register read	1	0	0	0	1	1
Auxiliary command register write	0	1	0			
Data register read	1	0	1			
Data register write	0	1	1			
Nonselection	x	x	x	1	1	1
Digital out register write	0	1	x	1	0	1
Control register write	0	1	x	1	1	0
Digital input register read	1	0	x	1	1	0

x = Don't care

Main Status Register

The main status register contains the status information of the FDC and may be accessed any time. Only the status register may be read and used to facilitate the transfer of data between the processor and the FDC.

The main status register bits are defined in table 3. Bits DIP and RQM indicate when data is ready and in which direction data will be transferred on the data bus. See figure 1.

Data Register

The data register stores data, commands, parameters, and FDD status information. Data bytes are read out of or written into the data register in order to program or obtain the results after a particular command.

Status registers ST0-ST3 (table 4) are stored in a stack with only one register at a time presented through the data register during the Result phase of a command.

Auxiliary Command Register

This register temporarily stores a command for the FDC. Auxiliary commands include Set Standby, Reset Standby, Software Reset, Start Clock, and Select Track Number.

Table 3. Main Status Register

Bit	Name	Function
D_0	D_0B (FDD 0 Busy)	FDD 0 is in the seek mode. If any of the D_nB bits is set, FDC will not accept a read or write command.
D_1	D_1B (FDD 1 Busy)	FDD 1 is in the seek mode. If any of the D_nB bits is set, FDC will not accept a read or write command.
D_2	D_2B (FDD 2 Busy)	FDD 2 is in the seek mode. If any of the D_nB bits is set, FDC will not accept a read or write command.
D_3	D_3B (FDD 3 Busy)	FDD 3 is in the seek mode. If any of the D_nB bits is set, FDC will not accept a read or write command.
D_4	CB (FDC Busy)	A read or write command is in procces. FDC will not accept any other command.
D_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
D_6	DIO (Data Input/Output)	Indicates direction of data transfer between FDC and data register. If DIO = 1, transfer is from data register to processor. If DIO = 0, transfer is from processor to data register.
D_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

Table 4. Status Registers ST0-ST3

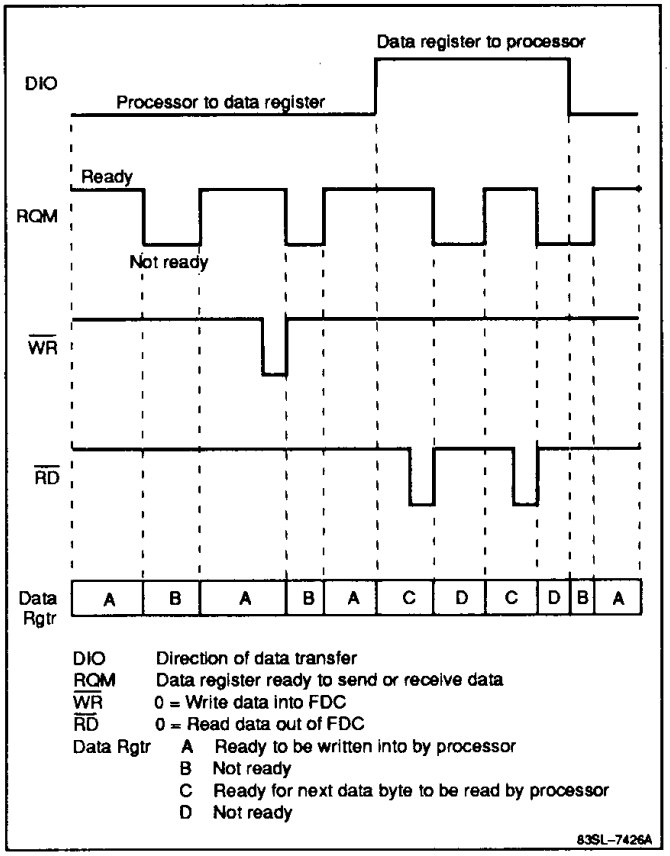
Bit	Name	Function
Status Register ST0		
D_7, D_6	IC (interrupt Code)	D_7 = 0 and D_6 = 0. Normal termination of command (INT). Command was completed and properly executed. D_7 = 0 and D_6 = 1. Abnormal termination of command (AT). Execution of command was started but was not successfully completed. D_7 = 1 and D_6 = 0. Invalid command issue (IC). Command that was issued was never started. D_7 = 1 and D_6 = 1. Abnormal termination because during command execution the ready signal from the FDD changed state.
D_5	SE (Seek End)	When the FDC completes the Seek command, this flag is set to 1.
D_4	EC (Equipment Check)	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate command), then this flag is set.
D_3	NR (Not Ready)	When the FDD is in the not-ready state and Read or Write command is issued, this flag is set. If a Read or Write command is issued to sed 1 of a single-sided drive, then this flag is set.
D_2	HD (Head Address)	This flag indicates the state of the head at interrupts.
D_1	US_1 (Unit Select1)	This flag indicates a drive unit number at interrupt.
D_0	US_0 (Unit Select 0)	This flag indicates a drive unit number at interrupt.

CRC Cyclic Redundancy Check
IDR Internal Data Register
C Current/selected cylinder (track) 0 through 76 of the medium.

Table 4. Status Registers ST0-ST3 (cont)

Bit	Name	Function
Status Register ST1		
D_7	EN (End of Cylinder)	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6		Not used. This bit is always 0.
D_5	DE (Data Error)	When the FDC detects CRC(1) error in either the ID field or the data field, this flag is set.
D_4	OR (Overrun)	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3		Not used. This bit is always 0.
D_2	ND (No Data)	During execution of Read Data, Read Deleted Data, Write Data, Write Deleted Data, or Scan command, if the FDC cannot find the sector specified in the IDR(2) register, this flag is set. During execution of the Read ID command, if the FDC cannot read the ID field without an error, this flag is set. During execution of the Read Diagnostic command, if the starting sector cannot be found, this flag is set.
D_1	NW (Not Writable)	During execution of Write Data, Write Deleted Data , or Write ID command, if the FDC detects a write protect signal from the FDD, this flag is set.
D_0	MA (Missing Address Mark)	This bit is set if the FDC does not detect the IDAM before two index pulses. It is also set if the FDC cannot find the DAM or DDAM after the IDAM is found. The MD bit of ST2 is also set at this time
Status Register ST2		
D_7		Not used. This bit is always 0.
D_6	CM (Control Mark)	During execution of the Read Data or Scan command, if the FDC encounters a sector containing a deleted data address mark, this flag is set. It is also set if DAM is found during Read Deleted Data.
D_5	DD (Data Error in Data Field)	If the FDC detects a CRC error in the data field, this flag is set.
D_4	WC (Wrong Cylinder)	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	SH (Scan Equal Hit)	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	SN (Scan Not Satisfied)	During execution of the Scan command, if the FDC cannot find a sector on the cylinder that meets the condition, this flag is set.
D_1	BC (Bad Cylinder)	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, this flag is set.
D_0	MD (Missing Address Mark in Data Field)	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, this flag is set.
Status Register ST3		
D_7	FT (Fault)	Indicates status of fault signal from the FDD.
D_6	WP (Write Protected)	Indicates status of write protected signal from the FDD.
D_5	RY (Ready)	Indicates status of ready signal from the FDD.
D_4	T0 (Track 0)	Indicates status of track 0 signal from the FDD.
D_3	TS (Two-Side)	Indicate status of two-side signal from the FDD.
D_2	HD (Head Address)	Indicates status of side select signal from the FDD.
D_1	US_1 (Unit Select 1)	Indicates status of unit select 1 signal to the FDD.
D_0	US_0 (Unit Select 0)	Indicates status of unit select 0 signal to the FDD.

Figure 1. Main Status Register; Bits DIO and RQM



Digital Out Register

This register (table 5) provides PC/AT or special mode selection, drive selection, motor control, software reset, and INT/DMARQ.

Control Register

The control register (table 6) sets the data transfer rate.

Digital Input Register

The function of the Digital Input register (table 7) is to provide the Disk Change ($\overline{DKCG}$) status to the FDC.

Table 5. Digital Out Register

Bit	Name	Function
D7	MDSEL	Mode select: 1 Special mode 0 PC/AT mode
D6		Not used
D5	ENABLE MOTOR2	Motor control signal for drive 2. Setting D5 to 1 in PC/AT mode activates the $\overline{EM2}$ pin.
D4	ENABLE MOTOR1	Motor control signal for drive 1. Setting D4 to 1 in PC/AT mode activates the $\overline{EM1}$ pin.
D3	ENABLE INT/DMARQ	Enables the INT/DMARQ signal from the FDC. When D3 is 0, the INT and DMARQ pins will be in the high-impedance state, and the $\overline{DMAAK}$ and TC signals will be disregarded.
D2	RESET FDC	Reset signal for the FDC: 0 Set the reset state. 1 Clear the reset state.
D1		Not used.
D0	SELECT	Selects drive signal in the PC/AT mode: 0 $\overline{DS1}$ is active if $\overline{EM1}$ is active. 1 $\overline{DS2}$ is active if $\overline{EM2}$ is active.

Table 6. Control Register

Bit	Name	Function
CR7-CR2		Not used. (Set these bits to 0.)
CR1, CR0	DATA RATE	Sets the data transfer rate. (See table 8.)

Table 7. Digital Input Register

Bit	Name	Function
D7	$\overline{DKCG}$	Indicates the drive status. 0 The latch of the drive is left open or a medium may be changed.
D6-D0		Not used. (High-impedance state when read.)

OUTPUTS

Data Transfer Rate

Regardless of mode, the data transfer rate is set by bits CR1 and CR0 of the control register and by the logic state of the DRVTYP input pin. See table 8.

Write Precompensation

Regardless of mode, the pre-shift value for MFM-type modulation is set by the logic state of the PCSVL pin according to the data transfer rate. See table 9.

Drive Select

In the base or special mode of the μPD72064, drive select is set by bits US0 and US1. In the PC/AT mode, it is set by bits D0, D4, and D5 of the digital out register; see table 10.

Table 8. Setting Data Transfer Rate

Data Transfer Rate, kb/s MFM (FM)	Control Register CR1	Control Register CR0	DRVTYP Pin Input	$\overline{DEN}$ Pin Output
500 (250)	0	0	0	1
250 (125)	*0	1	0	0
	1	1	0	0
	1	0	0	0
300 (150)	*0	1	1	0

* State at the time the FDC is reset.

Table 9. Setting Pre-Shift Value

Data Transfer Rate, MFM (kb/s)	PCSVL Pin Input	Pre-Shift Value (ns)	Number of Tracks
500, 250	1	125	N/A
	0	187	≥ 43
		0	≤ 42
300	N/A	208	N/A

N/A = Not applicable

Table 10. Setting Drive Select in PC/AT Mode

	Digital Out Register		Drive Select Output	
D0 (SELECT)	D4 (ENABLE MOTOR1)	D5 (ENABLE MOTOR2)	$\overline{DS1}$	$\overline{DS2}$
0	1	x	0	1
1	x	1	1	0

SYSTEM CLOCK

Table 11 lists the connections from an external crystal resonator or clock to the XA and XB pins of the μPD72064. Note that a 32-MHz XA input is always required. For certain data transfer rates, a 19.2-MHz XB input is also required.

Table 11. System Clock Arrangement According to Data Transfer Rate

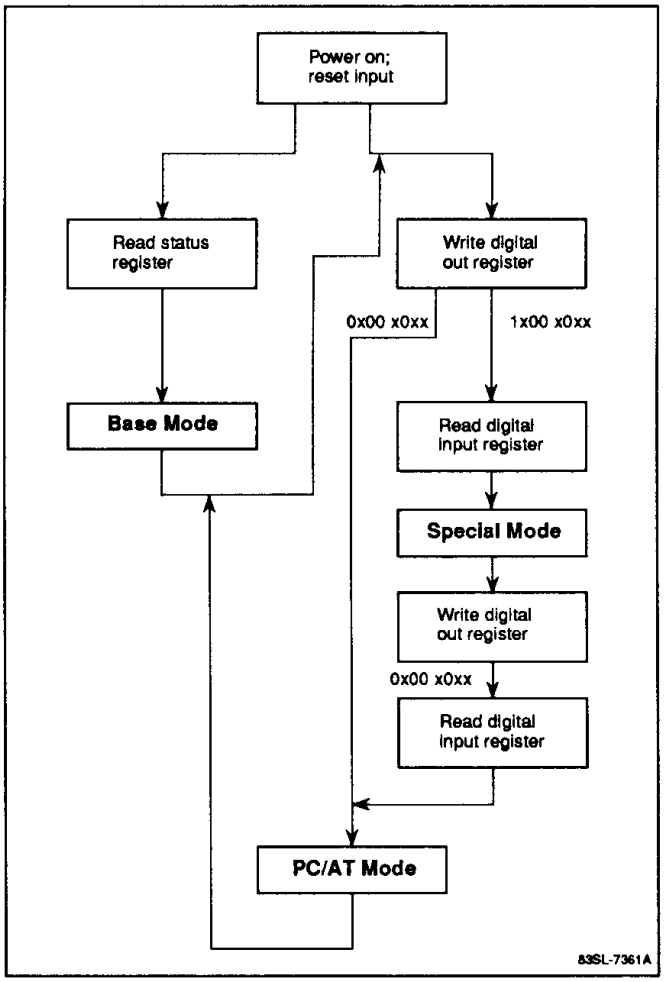
	Data Transfer Rate, kb/s		
Connections to Pins	500, 250	500, 300	300, 250
Crystal Resonator			
XA1, XA2	32 MHz	32 MHz	32 MHz
XB1, XB2	GND, Open	19.2 MHz	19.2 MHz
External Clock			
XA1 (*)	32 MHz	32 MHz	32 MHz
XB1 (*)	GND	19.2 MHz	19.2 MHz

* Leave pins XA2 and XB2 open

OPERATING MODES

Figure 2 shows the steps in setting the operating modes (base, special, and PC/AT) of the μPD72064.

Figure 2. Operating Modes Flowchart



COMMANDS

The μPD72064 FDC is capable of performing the 22 different commands listed in table 12. Each command is initiated by a multibyte transfer from the processor; after command execution, the result may be a multibyte transfer back to the processor. Because of this information interchange, it is convenient to consider each command as having three phases as follows.

Command — FDC receives all information from the processor it needs to perform a particular operation.

Execution — FDC performs the operation.

Result — Status and other housekeeping information are made available to the processor

Most commands require nine command bytes and return seven bytes during the result phase. Table 13 is the FDC instruction set. Symbols in table 13 are explained in table 14.

Table 12. List of Commands

Command Name	Function
Read Commands	
READ DATA	Specifies a sector and transfers its data to the host.
READ DELETED DATA	
READ DIAGNOSTIC	Checks the track format.
READ ID	Reads a sector ID.
SCAN EQUAL	Compares each sector data with host data and detects a sector that satisfies the set condition.
SCAN LOW OR EQUAL	
SCAN HIGH OR EQUAL	
Write Commands	
WRITE DATA	Specifies a sector and transfers its data from the host.
WRITE DELETED DATA	
WRITE ID	Writes the format of a track.
Seek Commands	
RECALIBRATE	Moves the read/write head to the outermost track (track 0).
SEEK	Moves the read/write head to the specified cylinder.
Sense Commands	
SENSE INTERRUPT STATUS	Reads the interrupt factor (seek end/state change) in the μPD72064.
SENSE DEVICE STATUS	Reads the FDD status.
Initialize Command	
SPECIFY	Defines a μPD72064 operation mode.
Other Commands	
INVALID	Reports the issuance of an unnecessary command to the μPD72064.
VERSION	Identifies a B-type product.
Auxiliary Commands	
SET STANDBY	Drives the μPD72064 in the standby status.
RESET STANDBY	Releases the μPD72064 from the standby status.
SOFTWARE RESET	Initializes the μPD72064.
START CLOCK	Starts the clock generator operation.
SELECT TRACK NUMBER	Specifies the maximum number of recalibratable tracks (77/255)

Table 13. Instruction Set

Phase	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data									
Command (Write)	MT	MF	SK	0	0	1	1	0	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
					H				
					R				
					N				
					EOT				
					GPL				
					DTL				
Execution									Data transfer between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				
Read Deleted Data									
Command (Write)	MT	MF	SK	0	1	1	0	0	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
					H				
					R				
					N				
					EOT				
					GPL				
					DTL				
Execution									Data transfer between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				

Notes:

(1) A_0 should equal 1 for all operations.

(2) x = Don't care; usually set to 0.

Table 13. Instruction Set (cont)

Phase	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Diagnostic									
Command (Write)	0	MF	SK	0	0	0	1	0	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution.
					H				
					R				
					N				
					EOT				
					GPL				
					DTL				
Execution									Data transfer between FDD and main system. FDC reads all data fields from index hole to EOT.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				
Read ID									
Command (Write)	0	MF	0	0	1	0	1	0	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
Execution									The first correct ID information on the cylinder is stored in the data register.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information read during execution phase from floppy disk.
					H				
					R				
					N				

Table 13. Instruction Set (cont)

Phase	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Equal									
Command (Write)	MT	MF	SK	1	0	0	0	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution.
					H				
					R				
					N				
					EOT				
					GPL				
					STP				
Execution									Data transfer between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				
Scan Low or Equal									
Command (Write)	MT	MF	SK	1	1	0	0	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution.
					H				
					R				
					N				
					EOT				
					GPL				
					STP				
Execution									Data compared between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				

Table 13. Instruction Set (cont)

Phase	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan High or Equal									
Command (Write)	MT	MF	SK	1	1	1	0	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution.
					H				
					R				
					N				
					EOT				
					GPL				
					STP				
Execution									Data compared between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				
Write Data									
Command (Write)	MT	MF	0	0	0	1	0	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
					H				
					R				
					N				
					EOT				
					GPL				
					DTL				
Execution									Data transfer between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				

Table 13. Instruction Set (cont)

Phase	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Deleted Data									
Command (Write)	MT	MF	0	0	1	0	0	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					C				Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
					H				
					R				
					N				
					EOT				
					GPL				
					DTL				
Execution									Data transfer between FDD and main system.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				Sector ID information after command execution.
					H				
					R				
					N				
Write ID (Format Write)									
Command (Write)	0	MF	0	0	1	1	0	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					N				Bytes/sector
					SC				Sectors/track
					GPL				Gap 3
					D				Filler byte
Execution									FDC formats an entire track.
Result (Read)					ST0				Status information after command execution.
					ST1				
					ST2				
					C				In this case, the ID information has no meaning
					H				
					R				
					N				
Recalibrate									
Command (Write)	0	0	0	0	0	1	1	1	Command codes.
	X	X	X	X	X	0	US_1	US_0	
Execution									Head retracted to track 0.

Table 13. Instruction Set (cont)

Phase	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Seek									
Command (Write)	0	0	0	0	1	1	1	1	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
					NCN				
Execution									Head is positioned over proper cylinder on diskette.
Sense Interrupt Status									
Command (Write)	0	0	0	0	1	0	0	0	Command code.
Result (Read)					ST0				Status information about FDC at the end of seek operation.
					PCN				
Sense Device Status									
Command (Write)	0	0	0	0	0	1	0	0	Command codes.
	X	X	X	X	X	HD	US_1	US_0	
Result (Read)					ST3				Status information about FDD.
Specify									
Command (Write)	0	0	0	0	0	0	1	1	Command codes.
	SRT (D_7-D_4)					HUT (D_3-D_0)			
				HLT (D_7-D_1)				ND	
Invalid									
Command (Write)					Invalid Codes				Invalid command codes.
Result (Read)					ST0				ST0 = 80H
Version									
Command (Write)	X	X	X	1	0	0	0	0	Command code.
Result (Read)	1	0	0	*1	0	0	0	0	*Indicates B-type product.
Set Standby									
Command (Write)	0	0	1	1	0	1	0	1	
Reset Standby									
Command (Write)	0	0	1	1	0	1	0	0	
Result (Read)	1	0	0	0	0	0	0	0	Invalid command.
Software Reset									
Command (Write)	0	0	1	1	0	1	1	0	
Start Clock									
Command (Write)	0	1	0	0	0	1	1	1	
Select Track Number									
Command (Write)	0	1	0	TR	1	1	1	1	
Result (Read)	1	0	0	0	0	0	0	0	Invalid command.

Table 14. Command Symbols

Symbol	Name	Description
A_0	Address Line 0	Controls selection of main status register (A_0 = 0) or data register (A_0 = 1).
C	Cylinder Number	Current/selected cylinder (track) 0 through 76 of the medium.
D	Data	Data pattern that is going to be written into a sector during WRITE ID operation.
D_7-D_0	Data Bus	8-bit data bus, where D_7 stands for the most significant bit, and D_0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length that users are going to read out or write into the sector.
EOT	End of Track	Final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	Length of gap 3. During Read/Write commands, this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During format command, it determines the size of gap 3.
H	Head Address	Logical head number 0 or 1, as specified in ID field.
HD	Head	Physical head number 0 or 1. Controls the polarity of the $\overline{SIDE}$ pin. (H = HD in all command words.)
HLT	Head Load Time	Head load time in the FDD (2 to 254 ms in 2-ms increments).
HUT	Head Unload Time	Head unload time after a Read or Write operation has occurred (16 to 240 ms in 16-ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected; if it is high, MFM mode is selected.
MT	Multitrack	If MT is high, a multitrack operation is performed. If MT = 1 after finishing read/write operation on side 0, the FDC will automatically start searching for sector 1 on side 1.
N	Number	Number of data bytes written in a sector.
NCN	New Cylinder Number	New cylinder number that is going to be reached as a result of the seek operation; desired position of head.
ND	Non-DMA Mode	Operation in the non-DMA mode.
PCN	Present Cylinder Number	Cylinder number at the completion of Sense Interrupt Status command (head position at present time).
R	Record	Sector number that will be read or written.
R/W	Read/Write	Read (R) or Write (W) signal.
SC	Sector	Number of sectors per cylinder.
SK	Skip	Skip deleted data address mark.
SRT	Step Rate Time	Stepping rate for the FDD (1 to 16 ms in 1-ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.).
ST0-ST3	Status 0-3	ST0-ST3 stands for one of four registers that store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST0-ST3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US_0, US_1	Unit Select	Selected drive number 0 or -3.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Voltage on any pin (except V_{DD})	−0.5 to V_{DD} + 0.5
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		20	pF	
Output capacitance	C_{OUT}		20	pF	

Oscillator Specifications

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; see figures 3, 4 and 5.

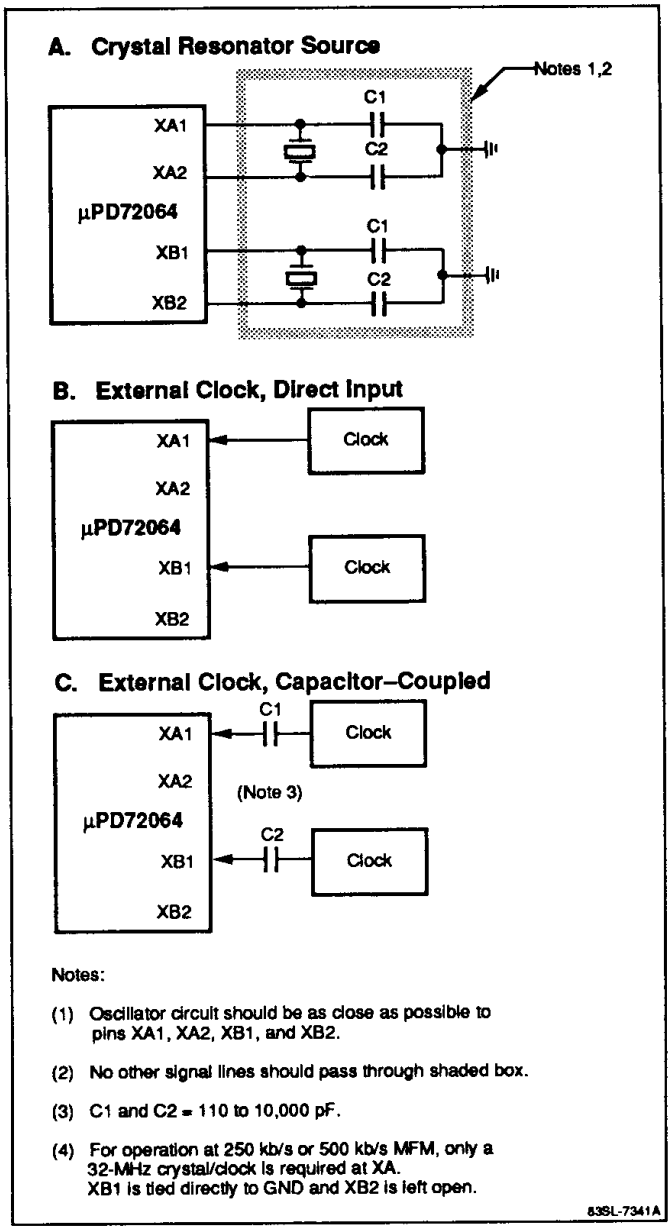
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal Resonator Source						
Oscillator stabilization time (Note 1)	t_{KS}			10	ms	
External Clock, Direct Input						
Low-level input voltage	V_{IL}	−0.5		0.2 V_{DD}	V	Pins XA1, XB1
High-level input voltage	V_{IH}	0.8 V_{DD}		V_{DD} + 0.5	V	
Clock cycle	t_{CYA}		31.25		ns	Pin XA1
	t_{CYB}		52.08		ns	Pin XB1
Permissible clock cycle error from typical value (Note 2)				±0.5	%	Pins XA1, XB1
Clock high-level width	t_{KKH}	7.0			ns	Pin XA1
		15.0			ns	Pin XB1
Clock low-level width	t_{KKL}	7.0			ns	Pin XA1
		15.0			ns	Pin XB1
Clock rise time	t_{KR}			5.0	ns	
Clock fall time	t_{KF}			5.0	ns	
External Clock, Capacitor-Coupled Input						
Clock input amplitude	V_{KP-P}	2.0		V_{DD}	V	Pins XA1, XB1
Clock cycle	t_{CYA}		31.25		ns	Pin XA1
	t_{CYB}		52.08		ns	Pin XB1
Permissible clock cycle error from typical value (Note 2)				±0.5	%	Pins XA1, XB1
Duty cycle, high-level		40		60	%	

Notes:

(1) Oscillator stabilization time should also be taken as the wait time between the issuance of START CLOCK and RESET STANDBY commands.

(2) Clock cycle error affects DPLL performance.

Figure 3. Recommended External Clock Circuits



Notes:

(1) Oscillator circuit should be as close as possible to pins XA1, XA2, XB1, and XB2.

(2) No other signal lines should pass through shaded box.

(3) C1 and C2 = 110 to 10,000 pF.

(4) For operation at 250 kb/s or 500 kb/s MFM, only a 32-MHz crystal/clock is required at XA. XB1 is tied directly to GND and XB2 is left open.

Figure 4. External Clock Waveform

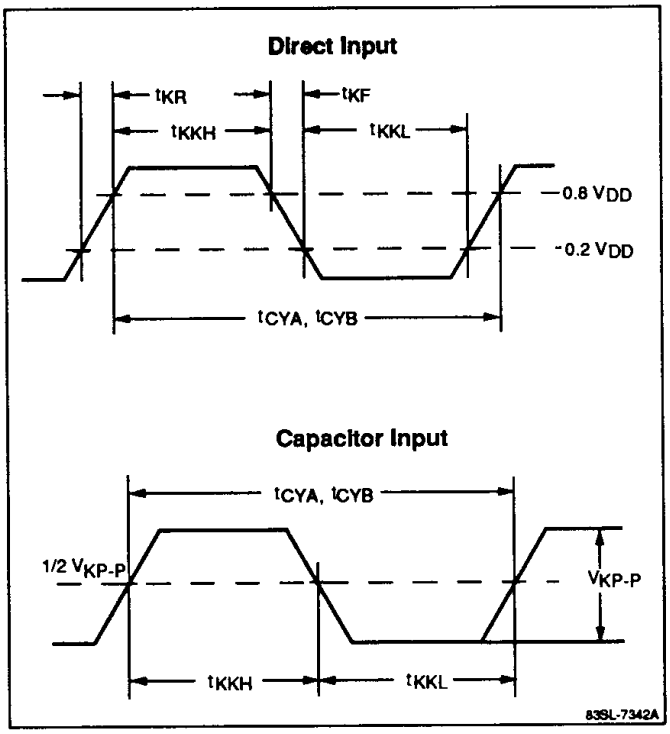
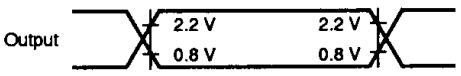


Figure 5. Voltage Thresholds for Timing Measurements



Output load = 1 TTL + 100 pF

Input Voltage During Measurement

Input	High Level	Low Level
Schmitt trigger	0.8 V_{DD}	0.45 V
XA1, XB1	0.9 V_{DD}	0.1 V_{DD}
Other input pins	2.4 V	0.45 V

83SL-7362A

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Pin Groups	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	2	−0.5	0.8	V	
	V_{IL1}	1	−0.5	0.2 V_{DD}	V	
High-level input voltage	V_{IH}	2	2.2	V_{DD} + 0.5	V	
	V_{IH1}	1	0.8 V_{DD}	V_{DD} + 0.5	V	
Low-level output voltage	V_{OL}	4		0.45	V	I_{OL} = 12 mA
	V_{OL1}	3		0.45	V	I_{OL} = 48 mA
High-level output voltage	V_{OH}	4	0.7 V_{DD}	V_{DD}	V	I_{OH} = −200 μA
Low-level input leakage current	I_{LIL}	1, 2		−10	μA	V_{IN} = 0 V
High-level input leakage current	I_{LIH}	1, 2		+10	μA	V_{IN} = V_{DD}
Low-level output leakage current	I_{LOL}	4		−10	μA	V_{OUT} = +0.45 V
	I_{LOL1}	3		−100	μA	
High-level output leakage current	I_{LOH}	4		+10	μA	V_{OUT} = V_{DD}
	I_{LOH1}	3		+100	μA	
V_{DD} supply current	I_{DD}			60	mA	
Standby current	I_{DD1}			100	μA	

Pin Groups:

(1) Schmitt-trigger inputs: $\overline{\text{DKCG}}$, $\overline{\text{INDEX}}$, $\overline{\text{RDATA}}$, $\overline{\text{TRK0}}$, $\overline{\text{WPRT}}$.

(2) Other inputs: A0, $\overline{\text{ACCR}}$, $\overline{\text{ACDR}}$, $\overline{\text{CS}}$, D_0-D_7, $\overline{\text{DKCGEN}}$, $\overline{\text{DMAAK}}$, DRVTYP, PCSVL, $\overline{\text{RD}}$, RESET, TC, $\overline{\text{WR}}$; excludes XA1, XA2, XB1, XB2.

(3) Open-drain outputs: $\overline{\text{DIR}}$, $\overline{\text{DS1}}$, $\overline{\text{DS2}}$, $\overline{\text{SIDE}}$, $\overline{\text{STEP}}$, $\overline{\text{WDATA}}$, $\overline{\text{WE}}$. Disk drive outputs: $\overline{\text{DEN/LCT}}$, EMI/DS3, EM2/DS4, HDLD.

(4) Other outputs: D_0-D_7, DMARQ, INT.

AC Characteristics 1; 500 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{ACCR}$, $\overline{CS}$, $\overline{DMAAK}$ setup time to $\overline{RD}$	6	t_{AR}	0			ns	
A0, $\overline{ACCR}$, $\overline{CS}$, $\overline{DMAAK}$ hold time from $\overline{RD}$	6	t_{RA}	0			ns	
$\overline{RD}$ pulse width	6	t_{RR}	90			ns	
Data access time from $\overline{RD}$ ↓	6	t_{RD}			90	ns	
Data float delay time from $\overline{RD}$ ↑	6	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	6	t_{RI}			200	ns	When data is transferred in non-DMA mode.
A0, $\overline{ACCR}$, $\overline{ACDR}$, $\overline{CS}$, $\overline{DMAAK}$ setup time to $\overline{WR}$	7	t_{AW}	0			ns	
A0, $\overline{ACCR}$, $\overline{ACDR}$, $\overline{CS}$, $\overline{DMAAK}$ hold time from $\overline{WR}$	7	t_{WA}	0			ns	
$\overline{WR}$ pulse width	7	t_{WW}	60			ns	
Data setup time to $\overline{WR}$	7	t_{DW}	80			ns	
Data hold time from $\overline{WR}$	7	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	7	t_{WI}			200	ns	When data is transferred in non-DMA mode.
DMARQ cycle time	8	t_{MCY}	13			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	8	t_{MA}	0			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	8	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	8	t_{AA}	90			ns	
$\overline{RD}$ ↓ response time from DMARQ ↑	8	t_{MR}	0			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	8	t_{MW}	0			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	8	t_{MRW}			12	μs	
TC pulse width	8	t_{TC}	60			ns	
Clock hold time on standby	9	t_{WC}	4			μs	
Clock setup time after standby release	9	t_{CW}	2			μs	
START CLOCK command write setup time to RESET STANDBY command write	9	t_{WS}	2			μs	
INT response time from DMARQ ↓	10	t_{MI}	7.5		9.6	μs	
$\overline{DMAAK}$ signal invalid from INT ↑	10	t_{IA}			125	ns	
RESET pulse width	11	t_{RST}	250			μs	

AC Characteristics 1; 500 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ low-level width	12	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ low-level width	12	t_{WDD}		250		ns	
$\overline{\text{DS1}}$-$\overline{\text{DS4}}$ setup time to $\overline{\text{DIR}}$ (Note 3)	13	t_{DSD}	12			μs	Note 1
$\overline{\text{DIR}}$ setup time to $\overline{\text{STEP}}$	13	t_{DST}	1			μs	
$\overline{\text{DS1}}$-$\overline{\text{DS4}}$ hold time from $\overline{\text{STEP}}$ (Note 3)	13	t_{STU}	5			μs	
$\overline{\text{STEP}}$ low-level width	13	t_{STP}	6	7	8	μs	
$\overline{\text{DS1}}$-$\overline{\text{DS4}}$ hold time from $\overline{\text{DIR}}$ (Notes 2, 3)	13	t_{DDS}	15			μs	
$\overline{\text{DIR}}$ hold time from $\overline{\text{STEP}}$	13	t_{STD}	24			μs	
$\overline{\text{STEP}}$ cycle time	13	t_{SC}	33			μs	
$\overline{\text{INDEX}}$ low-level width	14	t_{IDX}	500			ns	

Notes:

(1) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(2) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(3) Except in PC/AT mode.

(4) See figure 5 for timing measurement voltage thresholds.

AC Characteristics 2; 250 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 250 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{ACCR}$, $\overline{CS}$, $\overline{DMAAK}$ setup time to $\overline{RD}$	6	t_{AR}	0			ns	
A0, $\overline{ACCR}$, $\overline{CS}$, $\overline{DMAAK}$ hold time from $\overline{RD}$	6	t_{RA}	0			ns	
$\overline{RD}$ pulse width	6	t_{RR}	90			ns	
Data access time from $\overline{RD}$ ↓	6	t_{RD}			90	ns	
Data float delay time from $\overline{RD}$ ↑	6	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	6	t_{RI}			200	ns	When data is transferred in non-DMA mode.
A0, $\overline{ACCR}$, $\overline{ACDR}$, $\overline{CS}$, $\overline{DMAAK}$ setup time to $\overline{WR}$	7	t_{AW}	0			ns	
A0, $\overline{ACCR}$, $\overline{ACDR}$, $\overline{CS}$, $\overline{DMAAK}$ hold time from $\overline{WR}$	7	t_{WA}	0			ns	
$\overline{WR}$ pulse width	7	t_{WW}	60			ns	
Data setup time to $\overline{WR}$	7	t_{DW}	80			ns	
Data hold time from $\overline{WR}$	7	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	7	t_{WI}			200	ns	When data is transferred in non-DMA mode.
DMARQ cycle time	8	t_{MCY}	26			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	8	t_{MA}	0			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	8	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	8	t_{AA}	90			ns	
$\overline{RD}$ ↓ response time from DMARQ ↑	8	t_{MR}	0			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	8	t_{MW}	0			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	8	t_{MRW}			24	μs	
TC pulse width	8	t_{TC}	60			ns	
Clock hold time on standby	9	t_{WC}	8			μs	
Clock setup time after standby release	9	t_{CW}	4			μs	
START CLOCK command write setup time to RESET STANDBY command write	9	t_{WS}	4			μs	
INT response time from DMARQ ↓	10	t_{MI}	15		19.2	μs	
$\overline{DMAAK}$ signal invalid from INT ↑	10	t_{IA}			250	ns	
RESET pulse width	11	t_{RST}	250			μs	

AC Characteristics 2; 250 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ low-level width	12	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ low-level width	12	t_{WDD}		500		ns	
$\overline{\text{DS1}}$-$\overline{\text{DS4}}$ setup time to $\overline{\text{DIR}}$ (Note 3)	13	t_{DSD}	24			μs	Note 1
$\overline{\text{DIR}}$ setup time to $\overline{\text{STEP}}$	13	t_{DST}	2			μs	
$\overline{\text{DS1}}$-$\overline{\text{DS4}}$ hold time from $\overline{\text{STEP}}$ (Note 3)	13	t_{STU}	10			μs	
$\overline{\text{STEP}}$ low-level width	13	t_{STP}	12	14	16	μs	
$\overline{\text{DS1}}$-$\overline{\text{DS4}}$ hold time from $\overline{\text{DIR}}$ (Notes 2, 3)	13	t_{DDS}	30			μs	
$\overline{\text{DIR}}$ hold time from $\overline{\text{STEP}}$	13	t_{STD}	48			μs	
$\overline{\text{STEP}}$ cycle time	13	t_{SC}	66			μs	
$\overline{\text{INDEX}}$ low-level width	14	t_{IDX}	1000			ns	

Notes:

(1) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(2) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(3) Except in PC/AT mode.

(4) See figure 5 for timing measurement voltage thresholds.

AC Characteristics 3; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{ACCR}$, $\overline{CS}$, $\overline{DMAAK}$ setup time to $\overline{RD}$	6	t_{AR}	0			ns	
A0, $\overline{ACCR}$, $\overline{CS}$, $\overline{DMAAK}$ hold time from $\overline{RD}$	6	t_{RA}	0			ns	
$\overline{RD}$ pulse width	6	t_{RR}	90			ns	
Data access time from $\overline{RD}$ ↓	6	t_{RD}			90	ns	
Data float delay time from $\overline{RD}$ ↑	6	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	6	t_{RI}			200	ns	When data is transferred in non-DMA mode.
A0, $\overline{ACCR}$, $\overline{ACDR}$, $\overline{CS}$, $\overline{DMAAK}$ setup time to $\overline{WR}$	7	t_{AW}	0			ns	
A0, $\overline{ACCR}$, $\overline{ACDR}$, $\overline{CS}$, $\overline{DMAAK}$ hold time from $\overline{WR}$	7	t_{WA}	0			ns	
$\overline{WR}$ pulse width	7	t_{WW}	60			ns	
Data setup time to $\overline{WR}$	7	t_{DW}	80			ns	
Data hold time from $\overline{WR}$	7	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	7	t_{WI}			200	ns	When data is transferred in non-DMA mode.
DMARQ cycle time	8	t_{MCY}	21.7			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	8	t_{MA}	0			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	8	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	8	t_{AA}	90			ns	
$\overline{RD}$ ↓ response time from DMARQ ↑	8	t_{MR}	0			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	8	t_{MW}	0			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	8	t_{MRW}			20	μs	
TC pulse width	8	t_{TC}	60			ns	
Clock hold time on standby	9	t_{WC}	6.7			μs	
Clock setup time after standby release	9	t_{CW}	3.3			μs	
START CLOCK command write setup time to RESET STANDBY command write	9	t_{WS}	3.3			μs	
INT response time from DMARQ ↓	10	t_{MI}	12.5		16.0	μs	
$\overline{DMAAK}$ signal invalid from INT ↑	10	t_{IA}			208.3	ns	
RESET pulse width	11	t_{RST}	250			μs	

AC Characteristics 3; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{RDATA}$ low-level width	12	t_{RDD}	40			ns	
$\overline{WDATA}$ low-level width	12	t_{WDD}		416.7		ns	
$\overline{DS1}$-$\overline{DS4}$ setup time to $\overline{DIR}$ (Note 3)	13	t_{DSD}	20			μs	Note 1
$\overline{DIR}$ setup time to $\overline{STEP}$	13	t_{DST}	1.7			μs	
$\overline{DS1}$-$\overline{DS4}$ hold time from $\overline{STEP}$ (Note 3)	13	t_{STU}	8.3			μs	
$\overline{STEP}$ low-level width	13	t_{STP}	10	11.7	13.3	μs	
$\overline{DS1}$-$\overline{DS4}$ hold time from $\overline{DIR}$ (Notes 2, 3)	13	t_{DDS}	25			μs	
$\overline{DIR}$ hold time from $\overline{STEP}$	13	t_{STD}	40			μs	
$\overline{STEP}$ cycle time	13	t_{SC}	55			μs	
$\overline{INDEX}$ low-level width	14	t_{IDX}	833.3			ns	

Notes:

(1) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(2) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(3) Except in PC/AT mode.

(4) See figure 5 for timing measurement voltage thresholds.

Figure 6. Read Operation

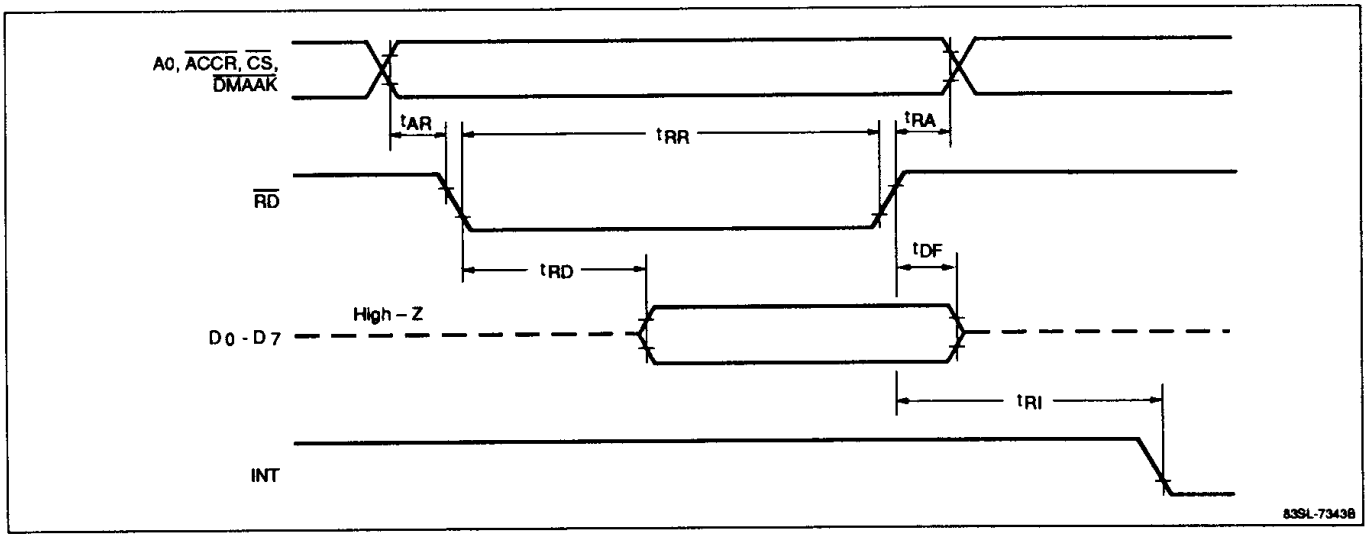


Figure 7. Write Operation

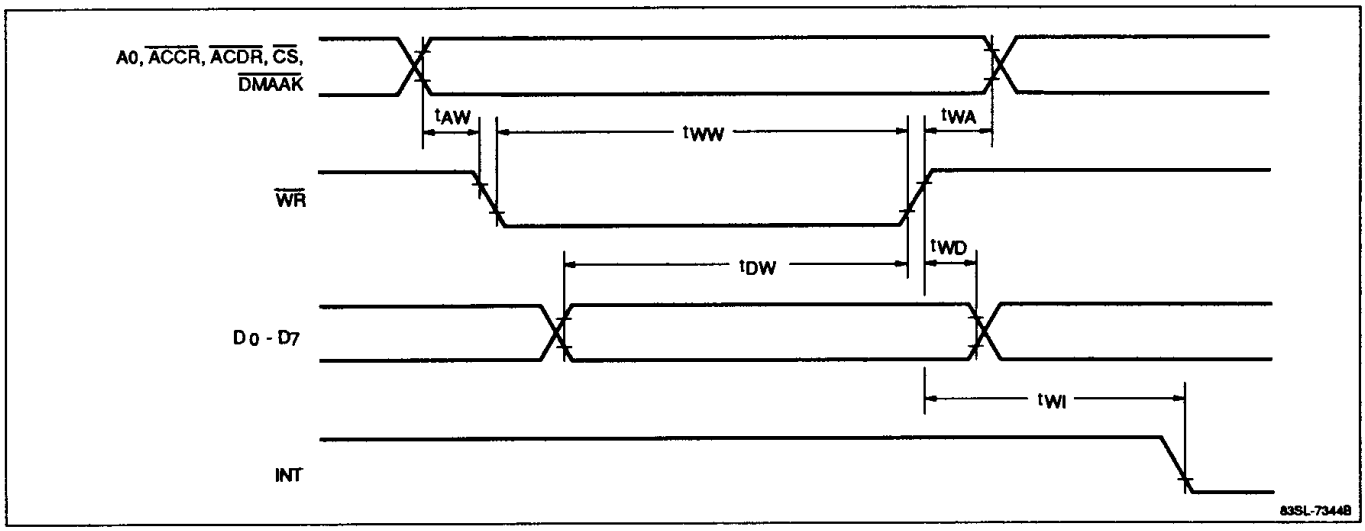


Figure 8. DMA Operation

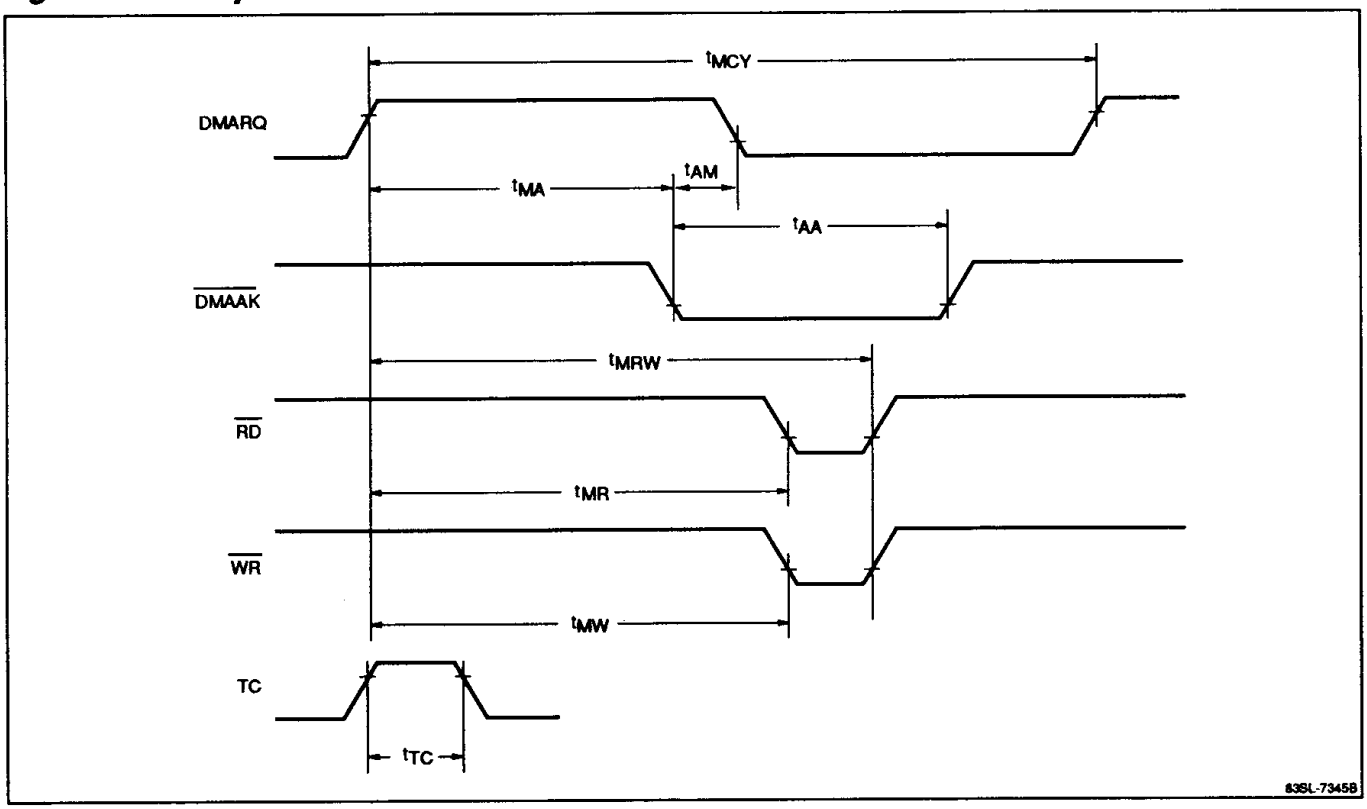
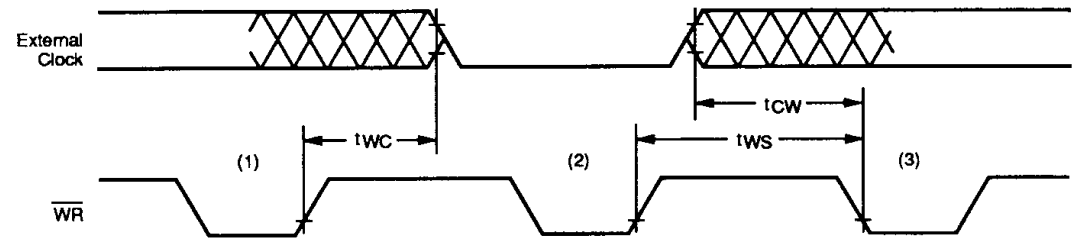


Figure 9. Standby Operation



Notes:

(1) SET STANDBY command write.

(2) START CLOCK command write.

(3) RESET STANDBY command write.

(4) When in standby mode the external clock should be fixed low. The standby current specifications cannot be met unless this is done.

83SL-5755B

Figure 10. Operation in Case of Overrun

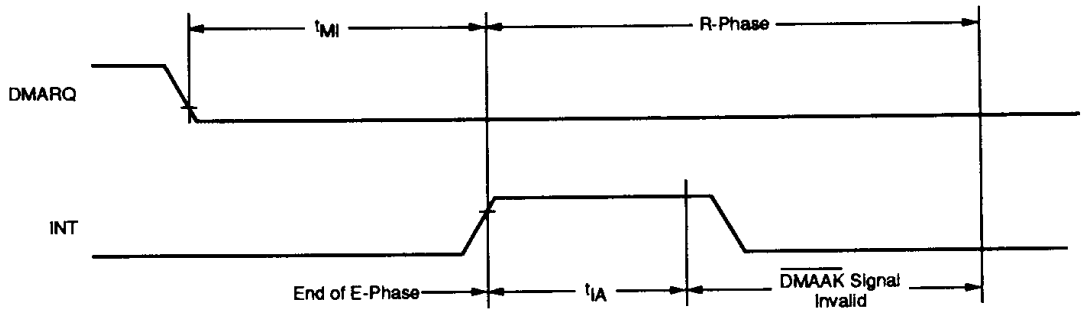


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Figure 11. RESET Waveform

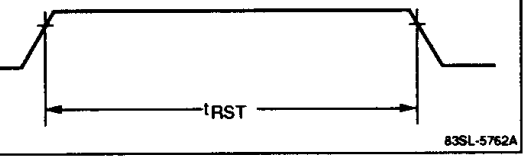

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Figure 12. $\overline{\text{RDATA}}$ and $\overline{\text{WDATA}}$ Waveforms

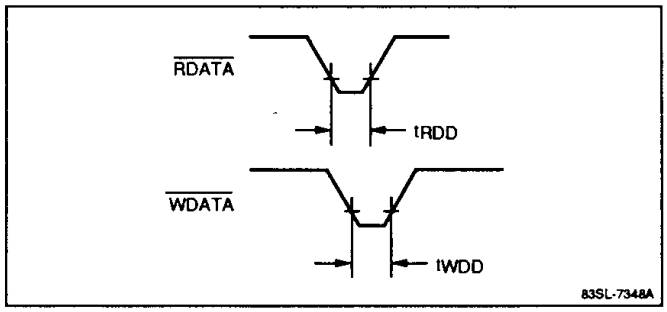


Figure 13. Seek Operation

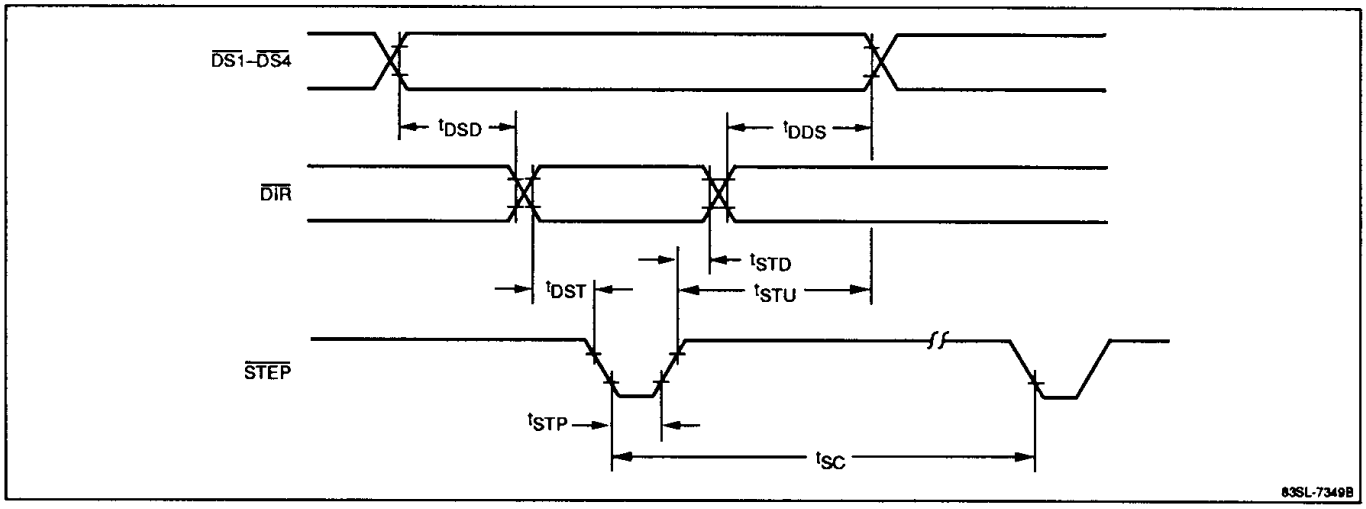
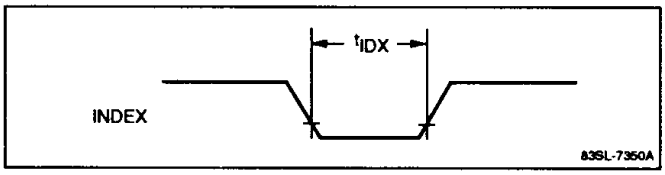


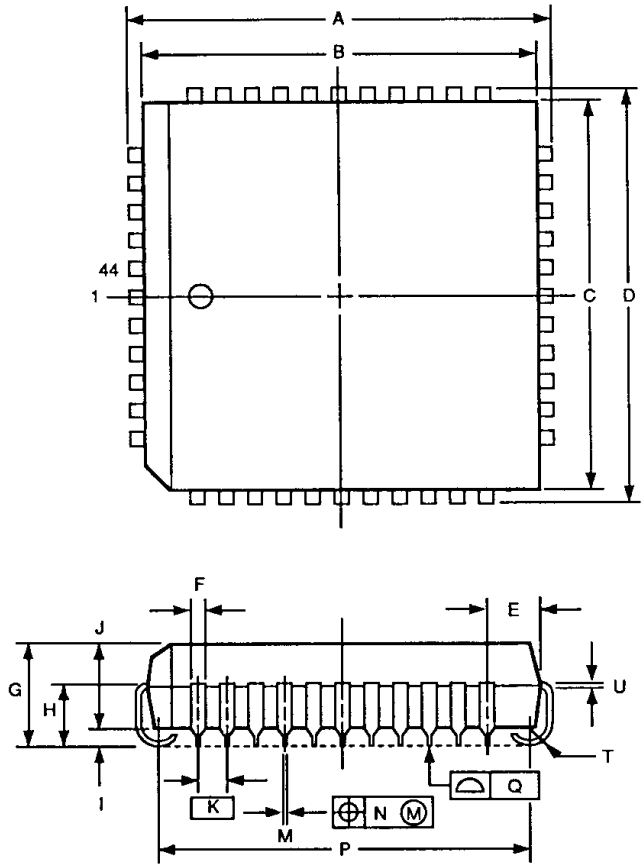
Figure 14. INDEX Waveform



PACKAGE DRAWINGS

44-Pin PLCC

Item	Millimeters	Inches
A	17.5 ±0.2	.689 ±.008
B	16.58	.653
C	16.58	.653
D	17.5 ±0.2	.689 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	15.50 ±0.20	.610 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

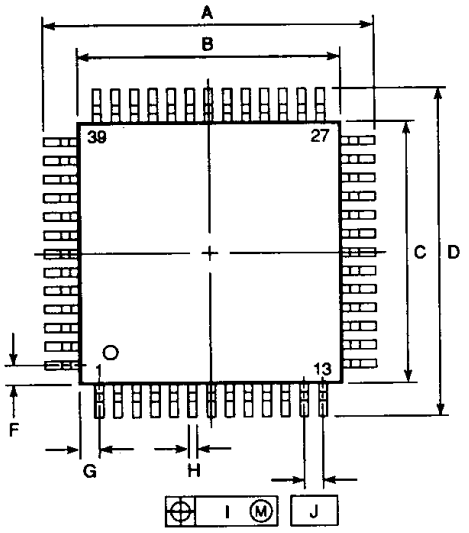


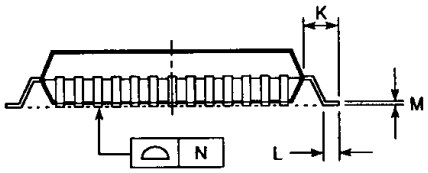
P44L-50A1-1

3/90 83YL-5804B

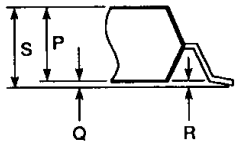
52-Pin Plastic QFP

Item	Millimeters	Inches
A	17.6 ±0.4	.693 ±.016
B	14.0 ±0.2	.551 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	17.6 ±0.4	.693 ±.016
F	1.0	.039
G	1.0	.039
H	0.40 ±0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ±0.2	.071 $^{+.008}_{-.009}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.119 max





Enlarged detail of lead end



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49NR-493B (5/89)

NEC

NEC Electronics Inc.

CORPORATE HEADQUARTERS

401 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000
TLX 3715792

For literature, call toll-free 8 a.m. to 4 p.m. Pacific time:
1-800-632-3531