μPD7502/03
4-Bit, Single-Chip CMOS Microcomputers With LCD Controller/Driver

T-49-19-40

Description

The μPD7502 and μPD7503 4-bit, single-chip CMOS microcomputers have advanced fourth-generation architecture with the functional blocks necessary for a single-chip controller, including an 8-bit timer/event counter, an 8-bit serial I/O, and an LCD controller/driver.

The instruction set includes the following types of instructions: addressing, table look-up, bit manipulation, vectored jump, auto increment or decrement data pointer, and conditional skip. These instructions maximize use of fixed program memory space.

Both devices are manufactured with the CMOS process and have a maximum power consumption of 900 μA at 5 V and 300 μA at 3 V. Halt and stop modes further reduce power consumption.

These devices are ideal for a wide range of solar- and battery-powered applications.

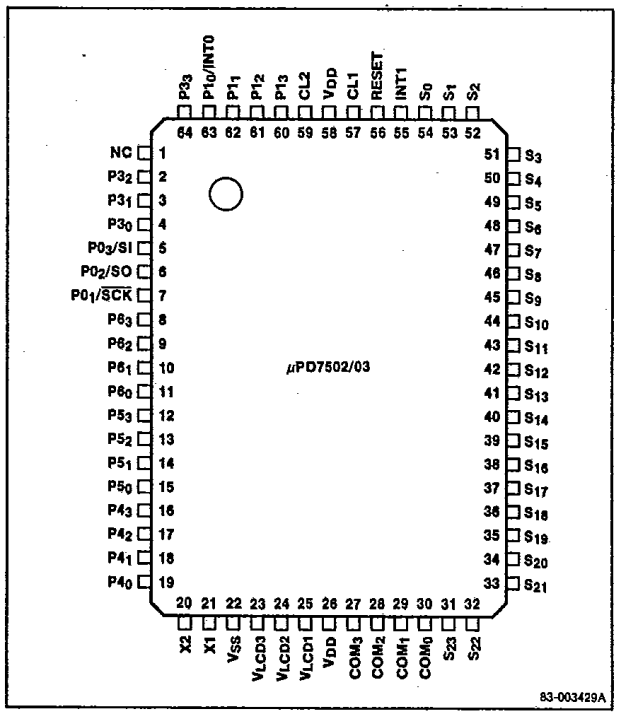
Features

- ☐ 92 powerful instructions
- ☐ Program ROM
  - — μPD7502: 2048 x 8-bit
  - — μPD7503: 4096 x 8-bit
- ☐ Data RAM
  - — μPD7502: 128 x 4-bit
  - — μPD5703: 224 x 4-bit
- ☐ Interrupts
  - — External: INT0, INT1
  - — Internal: INTT (timer/event counter)
    INTS (serial interface)
- ☐ 8-bit timer/event counter
  - — Based on crystal oscillation
  - — External event counter (prescale option by 64)
- ☐ Serial interface
- ☐ LCD controller/driver
  - — Programmable multiplexing mode: triplex, quadruplex, or pseudo-static
  - — 4 common lines (COM_0-COM_3)
  - — 24 segment lines (S_0-S_{23})
- ☐ Standby modes: stop, halt
- ☐ Data retention mode
- ☐ I/O ports
  - — 3-bit input port
  - — 4-bit input port
  - — 4-bit output port
  - — Two 4-bit I/O ports with 8-bit capability
  - — 4-bit I/O port with each bit configurable as an input or output
- ☐ RC oscillation clock
- ☐ Crystal oscillation clock
- ☐ 2.5 to 6.0 V operating voltage
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7502GF-12	64-pin plastic QFP	410 kHz
μPD7503GF-12	64-pin plastic QFP	410 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2-4, 64	$P3_3$-$P3_0$	4-bit output port 3
5-7	$P0_3$/SI $P0_2$/$\overline{SO}$ $P0_1$/$\overline{SCK}$	3-bit input port 0, or serial I/O interface
8-11	$P6_3$-$P6_0$	4-bit I/O port 6
12-15	$P5_3$-$P5_0$	4-bit I/O port 5
16-19	$P4_3$-$P4_0$	4-bit I/O port 4
20, 21	X2, X1	Crystal clock/external event input port X
22	V_{SS}	Ground
23-25	V_{LCD3}-V_{LCD1}	LCD bias supply inputs
26, 58	V_{DD}	Positive power supply
27-30	COM_3-COM_0	LCD backplane driver outputs
31-54	S_{23}-S_0	LCD segment driver outputs
55	INT1	External interrupt
56	RESET	RESET input
57, 59	CL1, CL2	System clock input
60-63	$P1_3$-$P1_1$, $P1_0$/INT0	4-bit input port 1, or external interrupt INT0

Status of Unused Pins

Name	Pin Connection
CL2	Open
X1	V_{SS}
X2	Open
$P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI	V_{SS} or V_{DD}
$P1_0$/INT0	V_{SS}
$P1_1$-$P1_3$	V_{SS} or V_{DD}
$P3_0$-$P3_3$	Open
$P4_0$-$P4_3$ $P5_0$-$P5_3$ $P6_0$-$P6_3$	Input mode: V_{SS} or V_{DD} Output mode: Open
INT1	V_{SS}
S_0-S_{23} COM_0-COM_3 V_{LCD1}-V_{LCD3}	Open

Pin Functions

$P0_3$/SI, $P0_2$/SO, $P0_1$/$\overline{SCK}$ [Port 0 or Serial Interface]

This port can be configured as a 4-bit parallel input port 0 or as the 8-bit serial I/O interface under control of the serial mode select register. The serial interface consists of the serial input (SI), the serial output (SO), and the serial clock ($\overline{SCK}$), which synchronizes data transfer.

$P1_3$-$P1_1$, $P1_0$/INT0 [Port 1 or Interrupt]

4-bit input port 1. Line $P1_0$ is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

$P3_3$-$P3_0$ [Port 3]

4-bit, latched three-state output port 3.

$P4_3$-$P4_0$ [Port 4]

4-bit input or latched three-state output port 4. Can perform 8-bit I/O in conjunction with port 5.

$P5_3$-$P5_0$ [Port 5]

4-bit input or latched three-state output port 5. Can perform 8-bit I/O in conjunction with port 4.

$P6_3$-$P6_0$ [Port 6]

4-bit input or latched three-state output port 6. The port 6 mode select register configures individual lines as inputs or outputs.

COM_3-COM_0 [LCD Backplane Driver Outputs]

LCD backplane driver outputs.

S_{23}-S_0 [LCD Segment Driver Outputs]

LCD segment driver outputs.

INT1 [Interrupt]

This external interrupt is a rising edge-triggered interrupt latched by CL.

RESET

A high-level input to this pin initializes the μPD7502/7503.

X2, X1 [Crystal Clock/External Event Input Port X]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input external event pulses to X1 and leave X2 open.

CL1, CL2 [System Clock Input]

Connect an 82-kΩ resistor across CL1 and CL2, and a 33-pF capacitor from CL1 to V_{SS}. Or, connect an external clock source to CL1 and leave CL2 open.

V_{LCD3}-V_{LCD1} [LCD Bias Voltage Inputs]

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.

V_{DD}

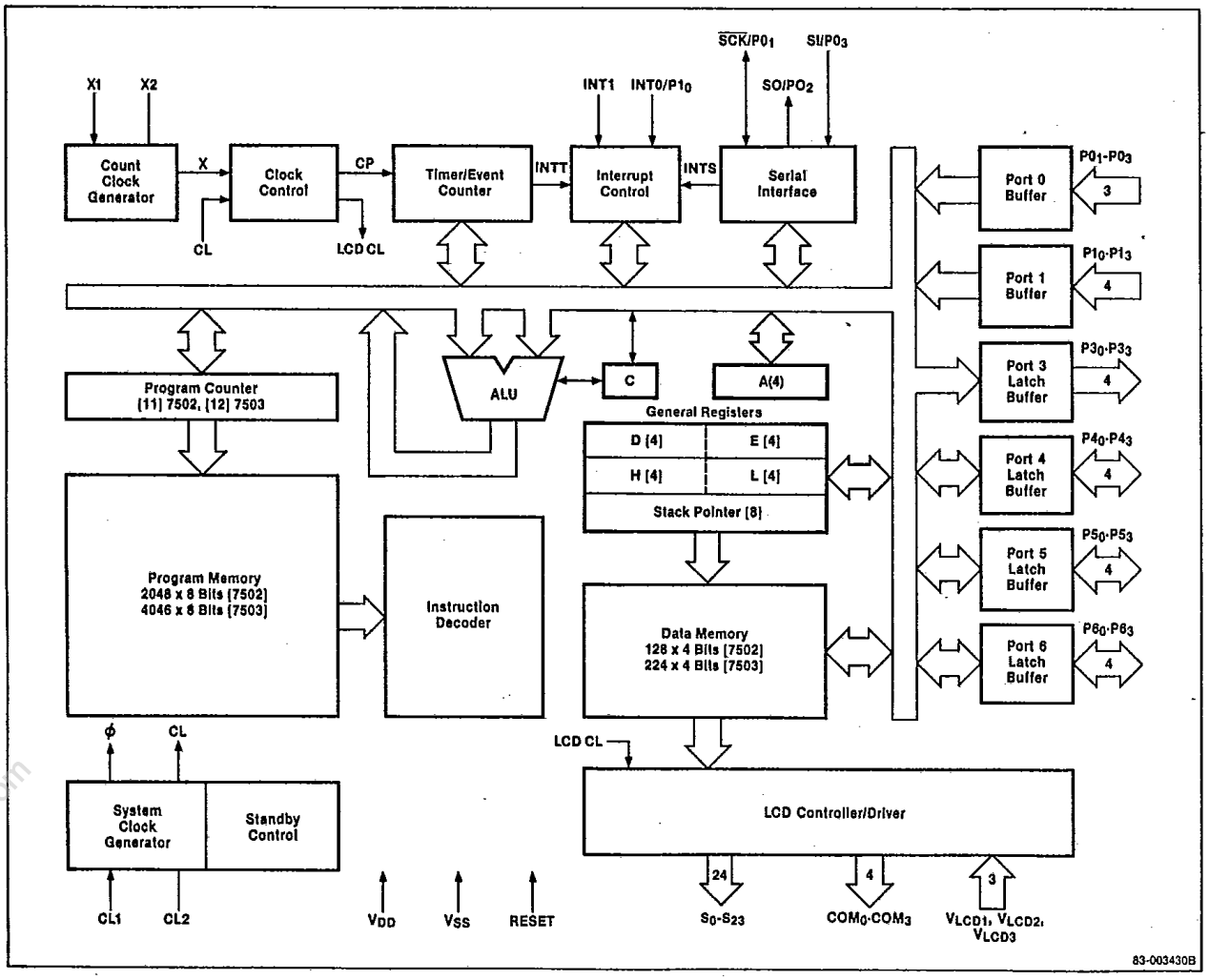
Positive power supply. For proper operation, apply a single voltage from 2.5 to 6.0 V.

V_{SS}

Ground.

T-49-19-40

Block Diagram



See figures 1 through 8 for additional block diagram details.

Figure	Title
1	Data Memory Map
2	Program Memory Map
3	Interface at Input/Output Ports
4	Clock Control
5	Timer/Event Counter
6	Interrupt Control
7	Serial Interface
8	LCD Controller/Driver

T-49-19-40

Figure 1. Data Memory Map

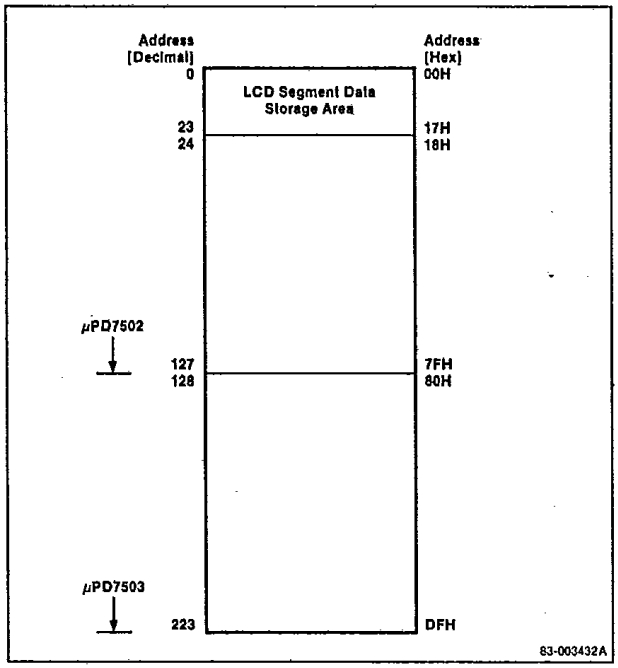
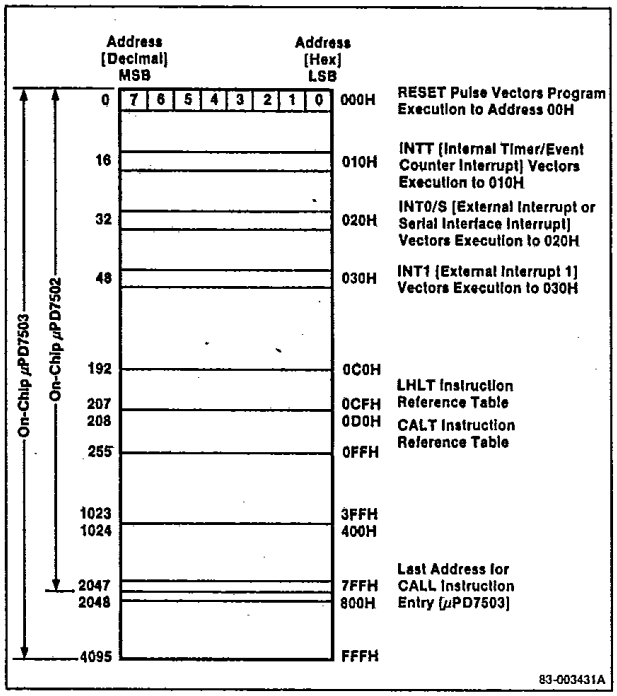


Figure 2. Program Memory Map



3

Figure 3. Interface at Input/Output Ports

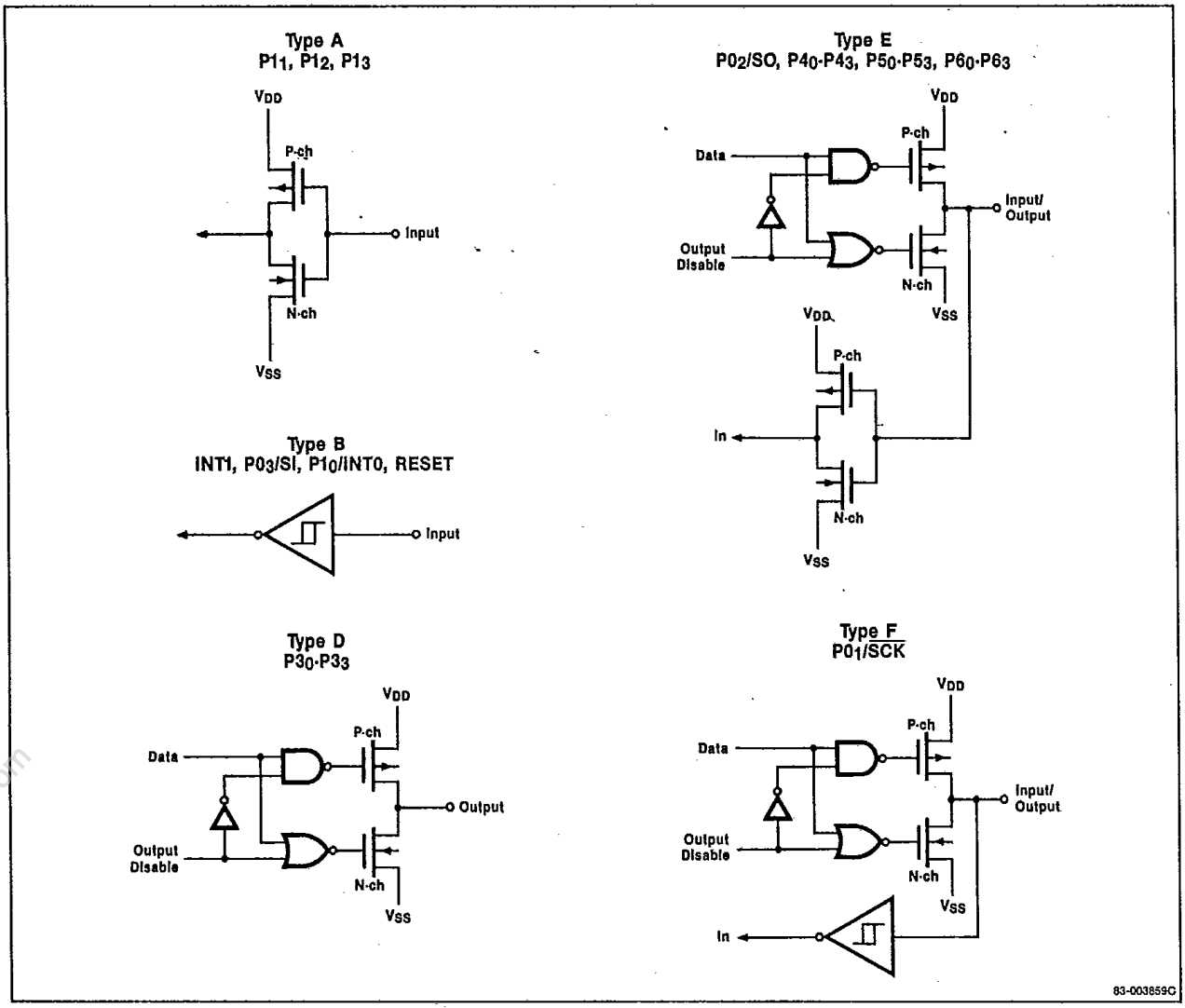
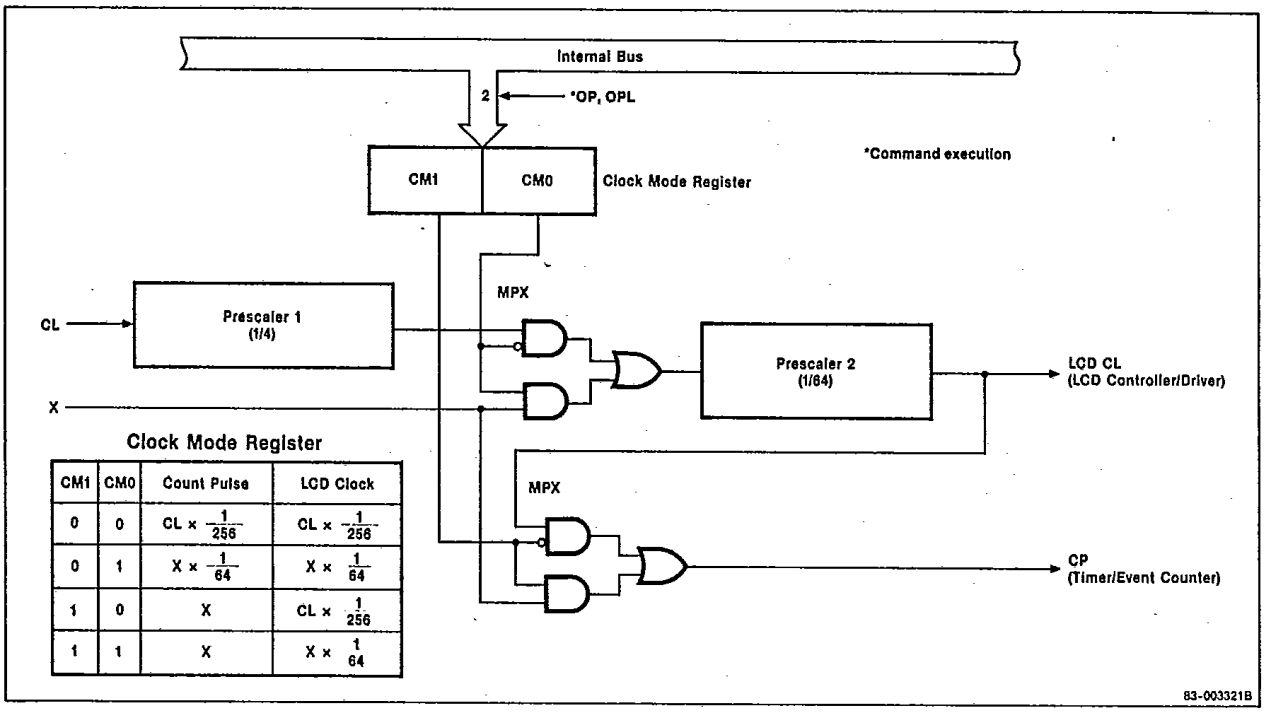


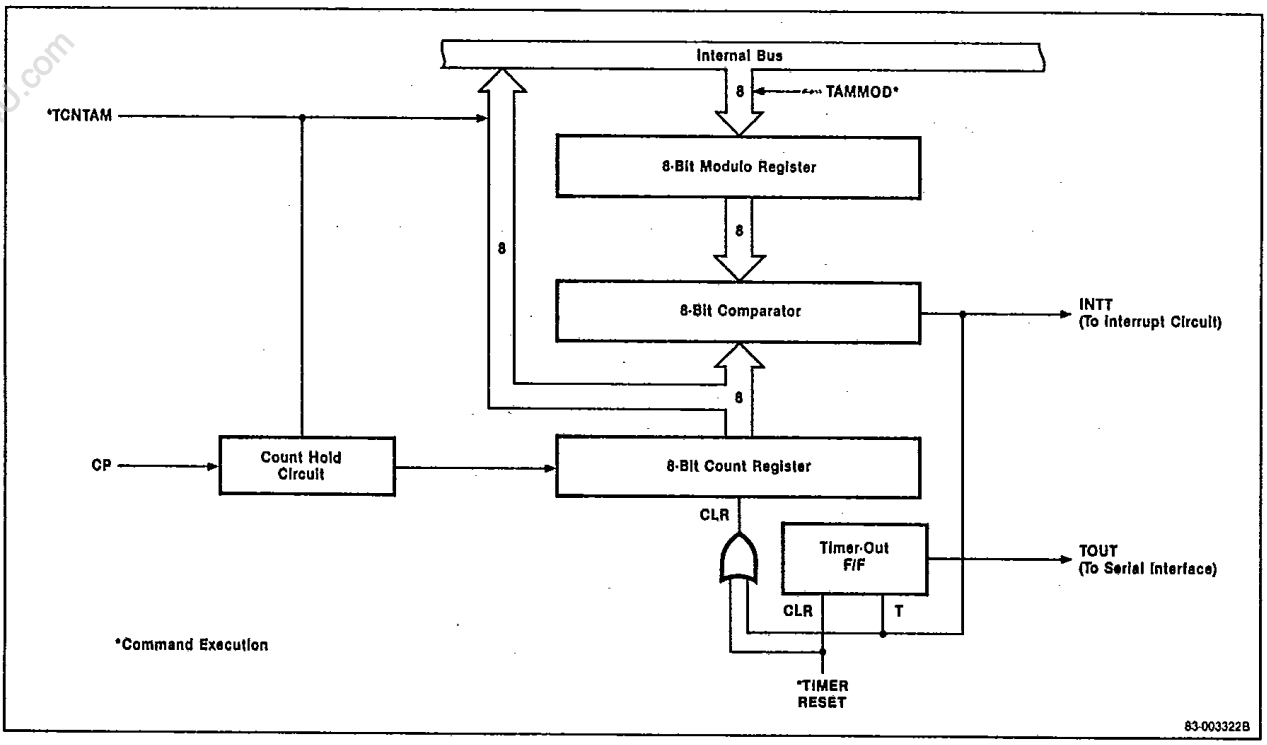
Figure 4. Clock Control



Clock Mode Register

CM1	CM0	Count Pulse	LCD Clock
0	0	CL × $\frac{1}{256}$	CL × $\frac{1}{256}$
0	1	X × $\frac{1}{64}$	X × $\frac{1}{64}$
1	0	X	CL × $\frac{1}{256}$
1	1	X	X × $\frac{1}{64}$

Figure 5. Timer/Event Counter



NEC

T-49-19-40

Figure 6. Interrupt Control

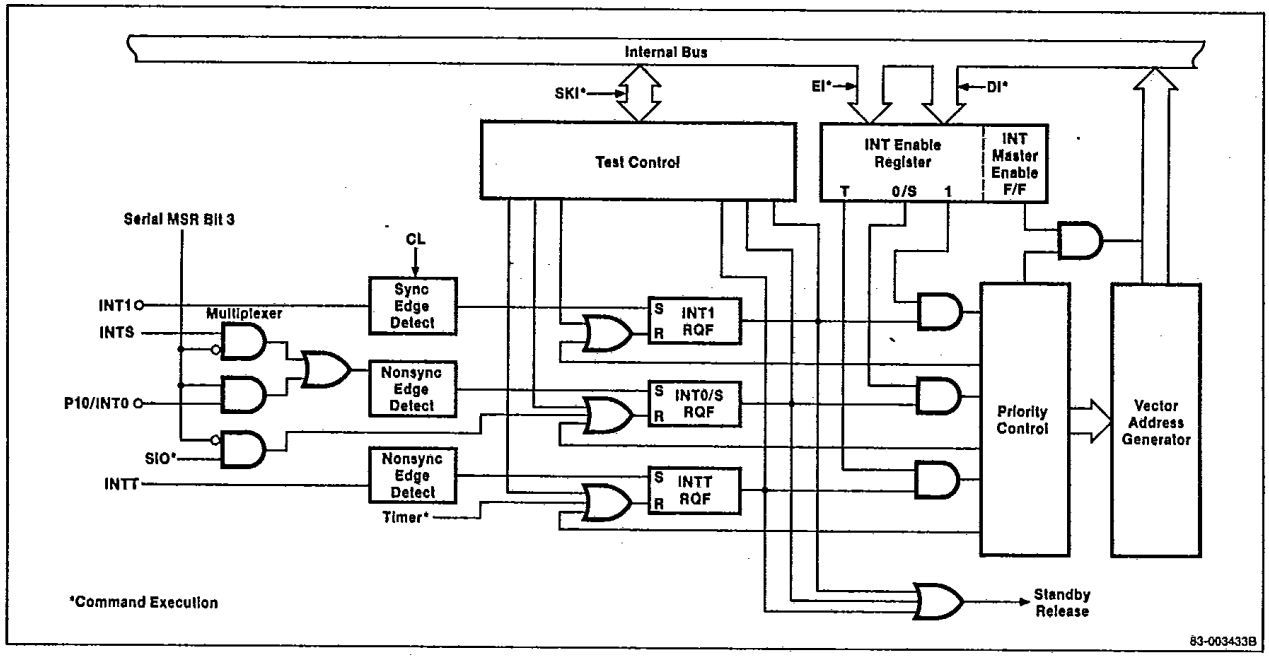
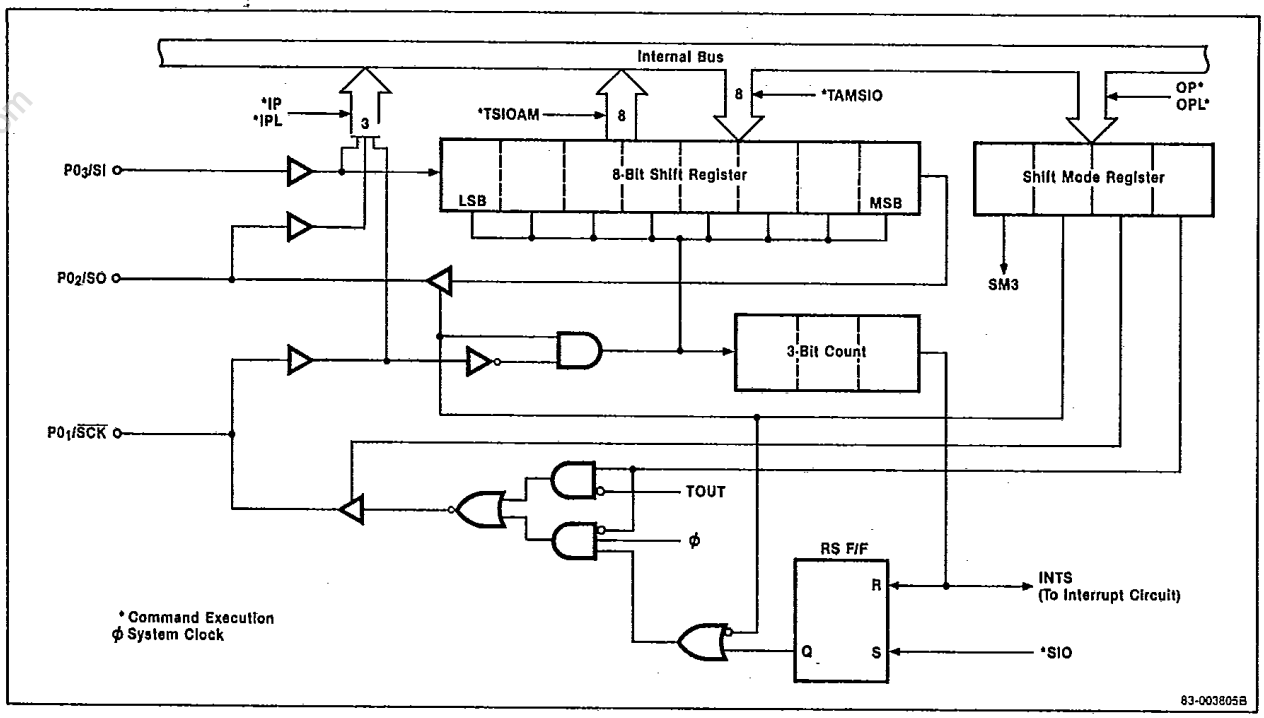
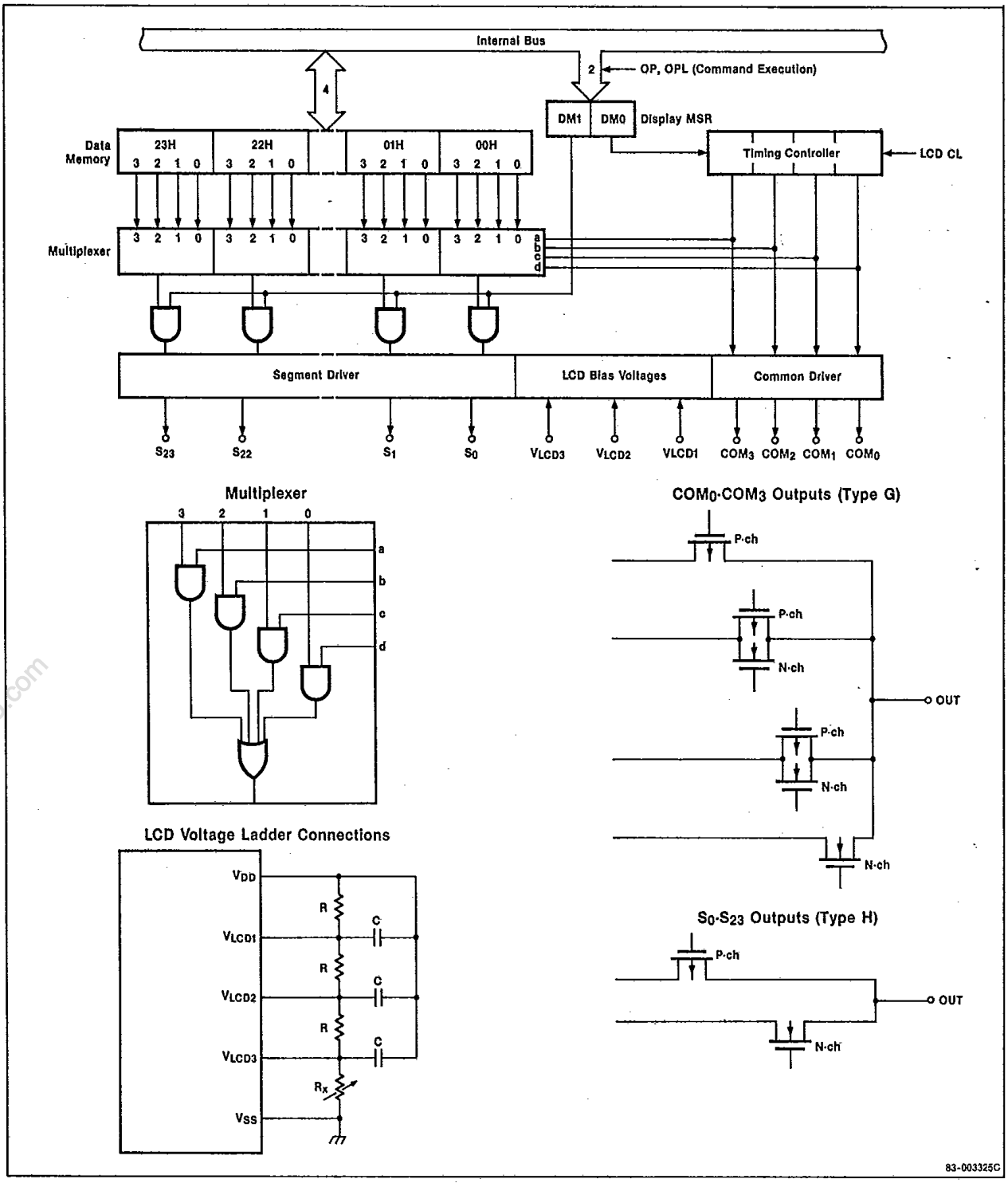


Figure 7. Serial Interface



T-49-19-40

Figure 8. LCD Controller/Driver



NEC

T-49-19-40

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 V to V_{DD} + 0.3 V
Output current high, I_{OH}	
Per pin	−17 mA
Total, output ports	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, output ports	55 mA
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	$f_C = 1$ MHz Unmeasured pins returned to V_{SS}
Output capacitance	C_O			15	pF	
I/O capacitance	C_{IO}			15	pF	

DC Characteristics 1

For V_{DD} = 2.5 to 3.3 Volts

$T_A = -10$ to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	$I_{OH} = -80\ \mu A$
Output voltage, low	V_{OL}			0.5	V	$I_{OL} = 350\ \mu A$
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_{IN} = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_{IN} = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; $V_{IN} = 0$ V
	I_{LIL2}			−10	μA	CL1, X1; $V_{IN} = 0$ V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	250	μA	Normal operation, $V_{DD} = 3$ V ± 10%; R = 240 kΩ ±2%, C = 33 pF ±5%
			35	230	μA	Normal operation, $V_{DD} = 2.5$ V; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 3$ V ±10%
			0.2	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 2.5$ V
	I_{DDDR}		0.2	10	μA	Data retention mode, $V_{DDDR} = 2.0$ V

T-49-19-40

DC Characteristics 2

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2		RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA, V_{DD} = 4.5 to 6.0 V
		V_{DD} − 0.5			V	I_{OL} = −100 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA, V_{DD} = 4.5 to 6.0 V
				0.5	V	I_{OL} = 400 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Output impedance (1)	R_{COM}		3	5	kΩ	COM_0-COM_3; V_{DD} = 4.5 to 6.0 V
			5	15	kΩ	COM_0-COM_3
	R_S		15	20	kΩ	S_0-S_{23}; V_{DD} = 4.5 to 6.0 V
			20	60	kΩ	S_0-S_{23}
Supply voltage	V_{DDDR}	2.0		6.0	V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ± 10%; R = 82 kΩ ± 2%, C = 33 pF ± 5%
			70	300	μA	Normal operation, V_{DD} = 3 V ± 10%; R = 160 kΩ ± 2%, C = 33 pF ± 5%
	I_{DD2}		1.0	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ± 10%
			0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ± 10%
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

Note:

(1) V_{LCD} = 2.7 V to V_{DD}
$V_{LCD1} = V_{DD} - (1/3)\ V_{LCD}$
$V_{LCD2} = V_{DD} - (2/3)\ V_{LCD}$
$V_{LCD3} = V_{DD} - V_{LCD}$

AC Characteristics 1

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 160 kΩ ±2% (Note 1)
		75		135	kHz	R = 160 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as input
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		16.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	$\overline{SCK}$ as input
		2.2			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	(Note 2)			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Notes:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leqq 60$ ppm.

(2) $2 \times 10^3 \div f_{CC}$ or f_C in kHz.

T-49-19-40

AC Characteristics 2

For V_{DD} = 2.5 to 3.3 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	R = 240 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.25			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	(Note 2)			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	

Notes:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, |ΔC/°C| ≦ 60 ppm.

(2) $2 \times 10^3 \div f_{CC}$ or f_C in kHz.

Recommended R and C Values for System Clock Oscillation Circuit

T_A = −10 to +70°C

Supply Voltage Range	Recommended Values (Note 1)	Frequency Range
4.5 to 6.0 V	R = 82 kΩ ±2%	150 to 250 kHz, 200 kHz typical
2.7 to 3.3 V	R = 160 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R = 160 kΩ± 2%	75 to 135 kHz
2.5 to 3.3 V	R = 240 kΩ ±2%	50 to 80 kHz
2.5 to 6.0 V	R = 240 kΩ ±2 %	50 to 85 kHz

Note:

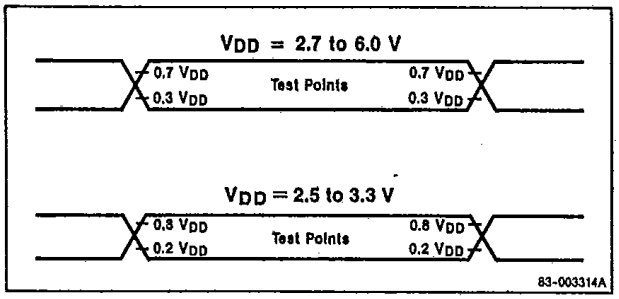
(1) C = 33 pF ±5%, |ΔC/°C| ≦ 60 ppm.

NEC

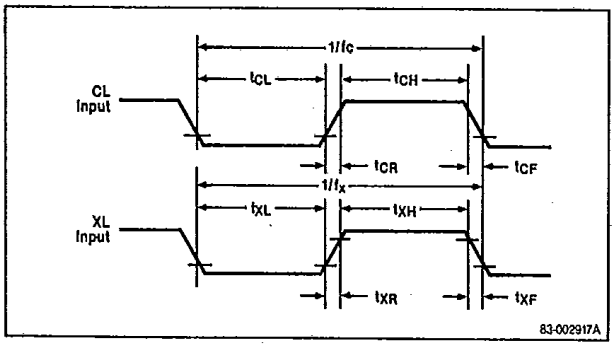
T-49-19-40

Timing Waveforms

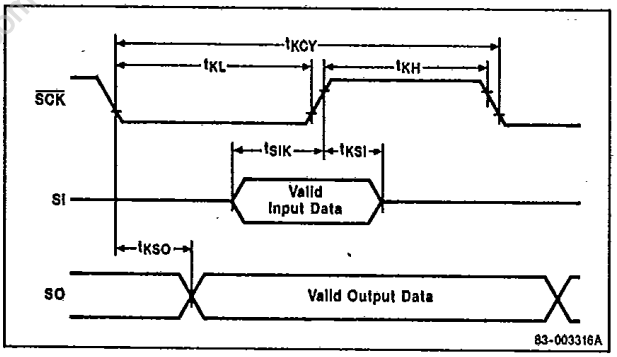
Timing Measurement Points



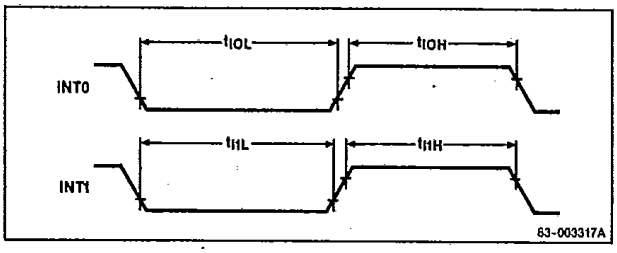
Clock Timing



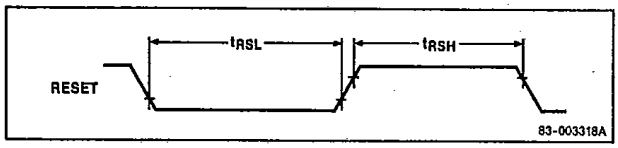
Serial Interface



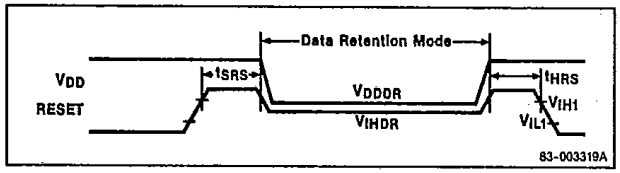
External Interrupts



Reset



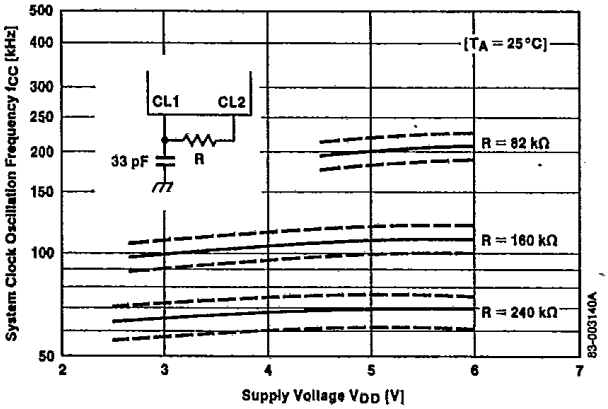
Data Retention Mode



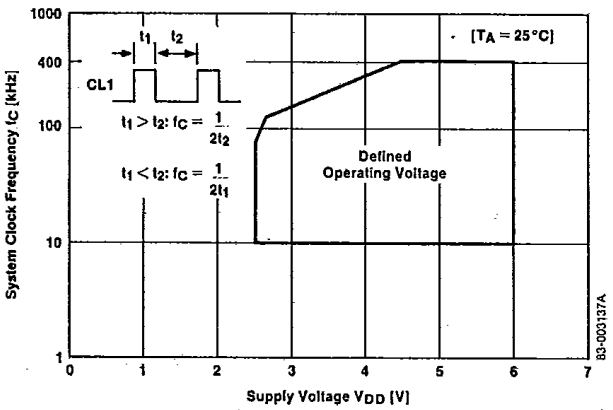
Operating Characteristics

$T_A = 25°C$

f_{CC} vs V_{DD}

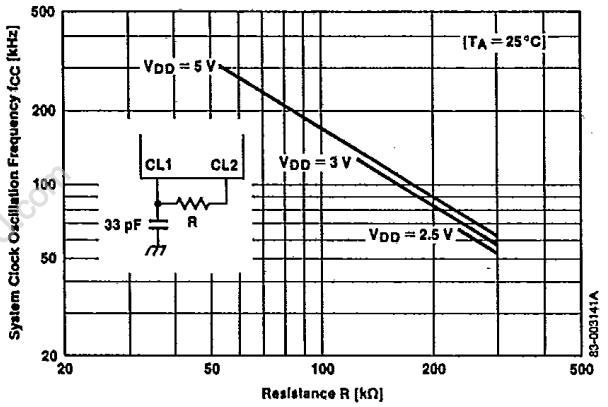


f_C vs V_{DD} [External Clock]

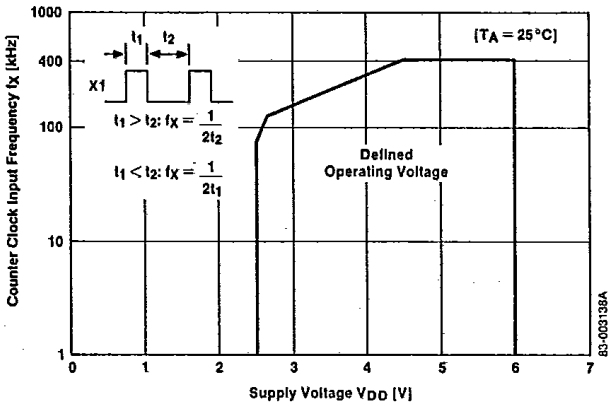


3

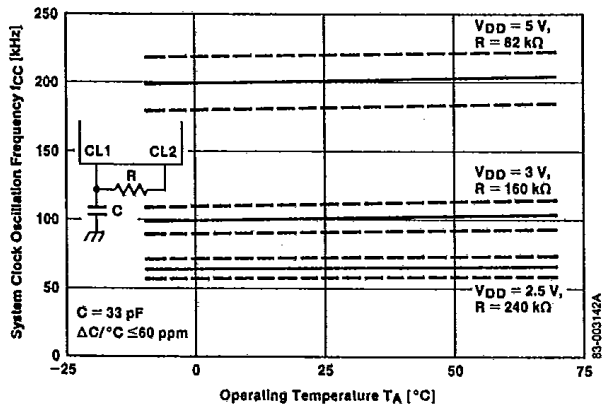
f_{CC} vs R



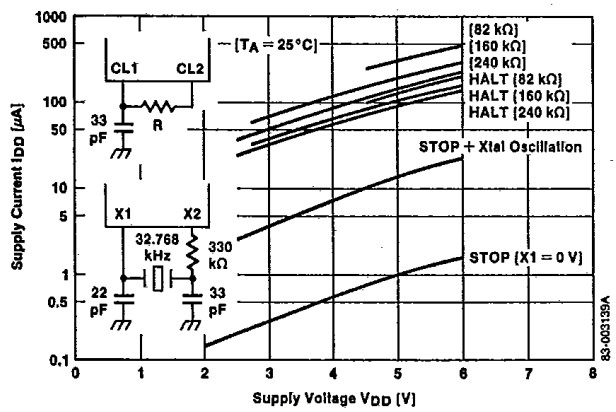
f_X vs V_{DD} [External Clock]



f_{CC} vs T_A



I_{DD} vs V_{DD}

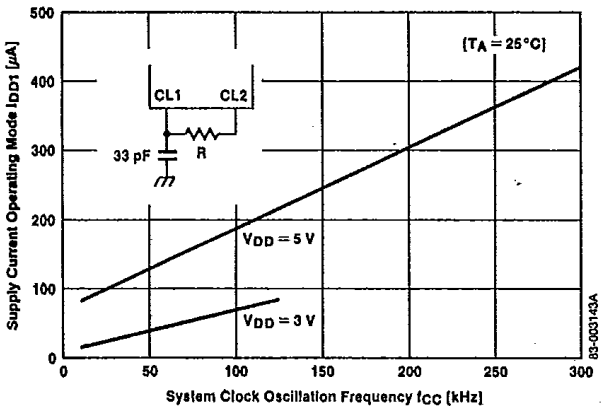


NEC

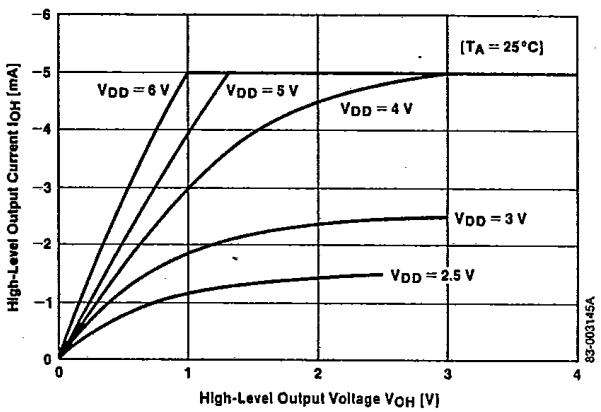
T-49-19-40

Operating Characteristics (cont)

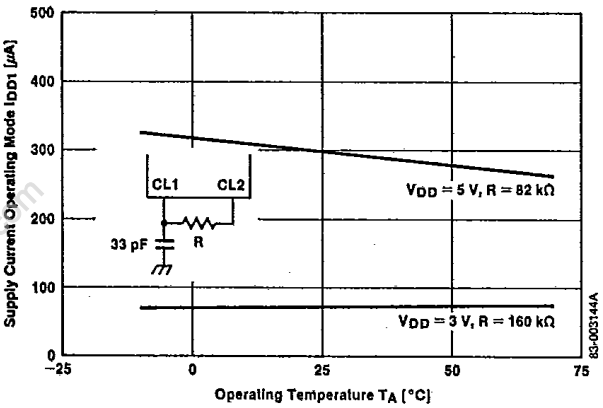
I_{DD1} vs f_{CC}



I_{OH} vs V_{OH}



I_{DD1} vs T_A



I_{OL} vs V_{OL}