4-BIT SINGLE CHIP MICROCOMPUTER

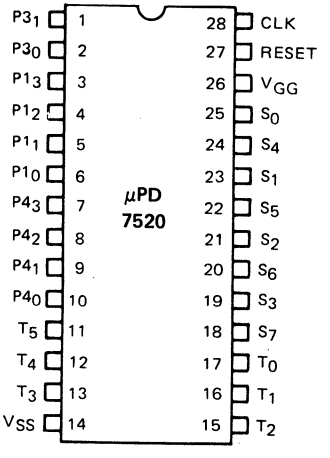
DESCRIPTION

The μPD7520 is a μCOM-75 4-bit single chip microcomputer with a Programmable Display Controller capable of directly driving a multiplexed 8-segment, 8-digit LED Display. It has a 768 x 8 ROM, a 48 x 4 RAM, and 24 I/O lines for communication with and control of external circuitry. The μPD7520 is manufactured with a low-power consumption PMOS process, allowing use of a single power supply between −6V and −10V. The μPD7520 executes 47 instructions of the μCOM-75 instruction set, and is available in a low-cost 28-pin plastic dual-in-line package.

FEATURES

- 768 x 8 Bit ROM
- 48 x 4 Bit RAM
- 20 μs Instruction Cycle Time, Typical
- 47 Powerful Instructions
  - Table Look-Up Capability with LAMT Instruction
- 2-Level Subroutine Stack
- One 4-Bit Input Port
- One 4-Bit I/O Port
- One 2-Bit Output Port (Capable of Driving Piezo Element)
- Programmable Display Controller
  - 6 LED Direct Digit Drive Outputs (8 Possible Using $P4_{0-1}$)
  - 8 LED Direct Segment Drive Outputs
  - Selection of a 4, 5, 6, or 8-Digit Display Strobe Cycle
  - Can Directly Drive 8-Segment, Multiplexed Displays, or up to an 8 x 8 Dot Matrix
  - Automatic Synchronization of Segment and Digit Signals, Transparent to Program Execution
  - Segment Outputs also Function as Latched, 8-Bit Parallel Output Port
- Built-In Clock Signal Generation Circuitry
- Built-In Reset Circuitry
- Single Power Supply, Variable from −6V to −10V
- Low Power Consumption: 45 mW, Typical
- P-Channel MOS Technology
- 28-Pin Plastic Dip

PIN CONFIGURATION



PIN NAMES

$S_0 - S_7$	Segment Drive Output Port S
$T_0 - T_5$	Digit Drive Output Port T
$P1_0 - P1_3$	Input Port 1
$P3_0 - P3_1$	Output Port 3
$P4_0 - P4_3$	Input/Output Port 4
CLK	Clock Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Ground

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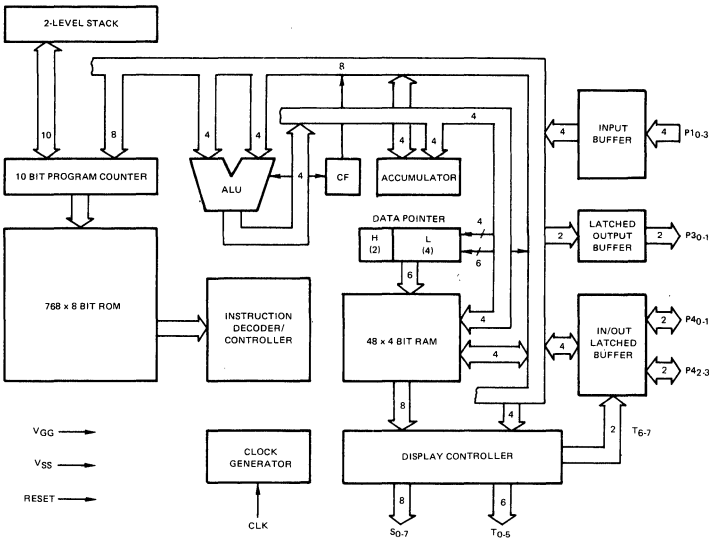
DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −6V to −10V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS	
Input Voltage High	V_{IH}			−2	V	Ports 1, 4, RESET	V_{GG} = −9V ± 1V
				−1.8			V_{GG} = −6V to −10V
Input Voltage Low	V_{IL}	V_{GG}+1.5			V	Ports 1, 4, RESET	V_{GG} = −9V ± 1V
		V_{GG}+0.8					V_{GG} = −6V to −10V
Clock Voltage High	$V_{\phi H}$			−0.8	V	CLK, External Clock	
Clock Voltage Low	$V_{\phi L}$	−5.0			V	CLK, External Clock	
Input Current High	I_{IH}	45		200	μA	Port 1, RESET	V_I = 0V, V_{GG} = −9V ± 1V
		40		200			V_I = 0V, V_{GG} = −6V to −10V
Input Leakage Current High	I_{LIH}			+5	μA	Port 4, V_I = 0V	
Input Leakage Current Low	I_{LIL_1}			−5	μA	Port 1, RESET, V_I = −10V, V_{GG} = −10V	
	I_{LIL_2}			−5	μA	Port 4, V_I = −10V	
Clock Current High	$I_{\phi H}$			0.5	mA	CLK, External Clock, $V_{\phi H}$ = 0V, V_{GG} = −9V ± 1V	
Clock Current Low	$I_{\phi L}$			−2.1	mA	CLK, External Clock, $V_{\phi L}$ = −5V, V_{GG} = −9V ± 1V	
Output Voltage Low	V_{OL}	V_{GG}+0.5			V	Port 3, No Load	
Output Current High	I_{OH_1}	−1.0			mA	Port 3,	V_O = −1.0V, V_{GG} = −9V ± 1V
		−0.6					V_O = −1.0V, V_{GG} = −6V
	I_{OH_2}	−2.0			mA	Port 4,	V_O = −1.0V, V_{GG} = −9V ± 1V
		−1.2					V_O = −1.0V, V_{GG} = −6V
	I_{OH_3}	−5	−10		mA	Port S,	V_O = −2.0V, V_{GG} = −9V ± 1V
		−3	−6				V_O = −2.0V, V_{GG} = −6V
		−1	−3				V_O = −1.0V, V_{GG} = −6V to −10V
	I_{OH_4}	−24	−48		mA	Port T,	V_O = −2.0V, V_{GG} = −9V ± 1V
		−13	−27				V_O = −1.0V, V_{GG} = −9V ± 1V ①
		−9	−18				V_O = −1.0V, V_{GG} = −6V
Output Current Low	I_{OL_1}	1	2		mA	Port 3,	V_O = V_{GG} + 1.5V, V_{GG} = −9V ± 1V ①
		0.1	0.2				V_O = V_{GG} + 3.5V, V_{GG} = −9V ± 1V
		0.3	0.6				V_O = −4.5V, V_{GG} = −6V ①
		0.1	0.2				V_O = −2.5V, V_{GG} = −6V
	I_{OL_2}	4.5	9		mA	Port S,	V_O = V_{GG} + 5.0V, V_{GG} = −9V ± 1V
		1	2				V_O = V_{GG} + 3.5V, V_{GG} = −6V to −10V
Output Leakage Current High	I_{LOH}			+5	μA	Ports 4, T, V_O = 0V	
Output Leakage Current Low	I_{LOL}			−5	μA	Ports 4, T, V_O = −10V	
Supply Current	I_{GG}		−5	−9.8	mA	T_a = 25°C, V_{GG} = −9V, No Load	

Note: ① Current within 2.5 ms after turning to the low level (T_a = 25°C).

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Internal Registers

The ALU, the Accumulator, and the Carry Flag together comprise the central portion of the μPD7520 architecture. The ALU performs the arithmetic and logical operations, and checks for various results. The Accumulator stores the results generated by the ALU, and acts as the major interface point between the RAM, the I/O ports, and the H and L registers. The Carry Flag can be addressed directly, and can be set during an addition.

Data Pointer Registers

The 2-bit H register and 4-bit L register are two registers which reside externally to the 48 x 4 bit RAM. They function as the Data Pointer, addressing the rows and columns of the RAM, respectively. They are individually accessible, and the L register can be automatically incremented or decremented.

RAM

The μPD7520 has a static 48 x 4 bit RAM organized into 3 rows by 16 columns. The RAM is used for general purpose data storage or data transfers, and is also used to store Display Data for access by the segment latch of the Display Controller.

ROM

The ROM is the mask-programmable portion of the μPD7520 which stores the application program. It is organized into a single 768 x 8 bit field. Execution of the program resident in the ROM is independent of field or page boundary limitations.

Program Counter and Stack Register

The Program Counter is a 10-bit register which contains the address of a particular instruction being executed. It is incremented during normal operation, but can be modified by various JUMP and CALL instructions. The Stack Register is a LIFO push-down stack register used to save the value of the Program Counter when a subroutine is called. It is organized as 2 words x 10 bits to accommodate 2 levels of subroutine calls.

CAPACITANCE

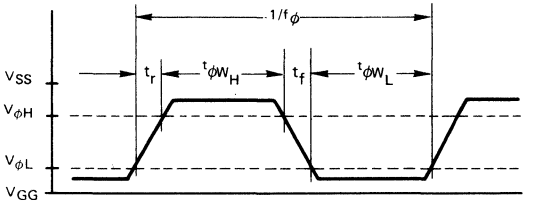
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS	
Input Capacitance	C_I			15	pF	Port 1, RESET	f = 1 MHz
Output Capacitance	C_O			20	pF	Ports 3, S, T,	
Input/Output Capacitance	C_{IO}			20	pF	Port 4	
Clock Capacitance	C_ϕ			30	pF	CLK	

AC CHARACTERISTICS

T_a = -10°C to +70°C, V_{GG} = -6V to -10V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Frequency	f_{osc}	225	300	375	kHz	R_f = 1MΩ, V_{GG} = -9V ± 1V, T_a = 25°C
		180	300	450	kHz	R_f = 1MΩ, V_{GG} = -9V ± 1V
	f_ϕ	100		330	kHz	CLK, External Clock
Clock Rise and Fall Times	t_r, t_f			2	μs	
Clock Pulse Width High	$t_{\phi W_H}$	1.5		3	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	1.5		3	μs	

CLOCK WAVEFORM



DEVELOPMENT TOOLS

The NEC Microcomputers' NDS Development System is available for the development of software source code, editing, and assembly into object code. In addition, the ASM-75 Cross Assembler is available for systems supporting the ISIS-II (TM Intel Corp.) Operating System, and the CASM-75 Cross Assembler is available for systems supporting the CP/M (® Digital Research Corp.) Operating System.

The EVAKIT-7520 Evaluation Board is available for production device evaluation and prototype system debugging.

Clock and Reset Circuitry

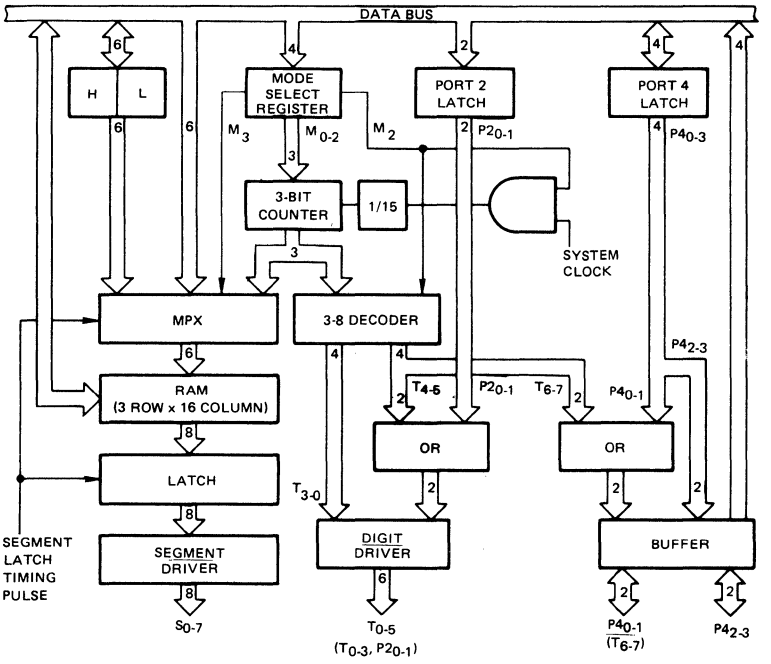
The Clock Circuitry for the μPD7520 can be implemented by connecting a resistor from the CLK input to V_{GG}. The Power-On-Reset Circuitry for the μPD7520 can be implemented by connecting a capacitor from the RESET input to V_{SS}.

I/O Capability

The μPD7520 has 24 I/O lines for communication with and control of external circuitry. The Port configuration is selectable under software control via the Mode Select Register as follows:

Port 1	$P1_{0-3}$	4-Bit Schmidt Input
Port 2	$P2_{0-1}$	2-Bit Latched Output Option, Accessible through Port T (T_{4-5})
Port 3	$P3_{0-1}$	2-Bit Latched Output
Port 4	$P4_{0-3}$	4-Bit Input/Latched Output
Port S	S_{0-7}	Latched 8-Bit Parallel/Segment Drive Output
Port T	T_{0-5}	6-Bit High-Current/Digit Drive Output
	T_{6-7}	Additional 2-Bit Digit Drive Output Option, Accessible through Port 4 ($P4_{0-1}$)

DISPLAY CONTROLLER BLOCK DIAGRAM



DISPLAY CONTROLLER

The Display Controller is the major feature of the μPD7520. It automatically performs scan or display strobe operations which would otherwise require considerable software.

The Display Controller interfaces to a common-anode LED display without external components. Connections from the Display Controller to the display are made from Port S to the cathodes (segments), and from Port T to the anodes (digit enables). Up to 6 digits can be driven directly by the μPD7520 in this manner. A total of 8 digit drives are available by using the two digit drives accessible through Port 4_{0-1}, and adding only two small driver transistors and four resistors externally. When Port T_{4-5} is not used to drive a display, it may be used as a high current driver, accessible through Port 2_{0-1}.

During operation, a 3-to-8 decoder selects which digit of a Display Buffer in the RAM will be multiplexed onto the display. The contents of the pair of RAM locations, corresponding to the digit chosen from the Display Buffer, are transferred to the 8 latched outputs of Port S, and the corresponding Port T digit drive is enabled. After 13 machine cycles have been completed, the digit drive is disabled, the decoder is updated to select the next digit of the Display Buffer to be multiplexed onto the display, and this cycle is repeated. Thus, the μPD7520 program needs only to load the properly decoded display data into the Display Buffer and it immediately appears on the display. Operation in this manner is completely transparent to the μPD7520, and requires no intervention once the proper display mode has been selected.

The use of a Mode Select Register enhances the utility of the Display Controller by allowing a choice of a 4, 5, 6, or 8 digit display strobe cycle output, or a direct latched output. A choice can also be made between one of the two possible Display Buffers, resident in either Row 0 or Row 2 of the RAM.

MODE SELECT REGISTER

The Mode Select Register (MSR) is a separate 4-bit register of the Display Controller which determines the function that the Display Controller will perform. The value of the MSR can range from 0_{16} to F_{16}, and it can be modified by data in the Accumulator. This is accomplished by execution of the OPL (output-to-port) instruction, where L (the lower 4-bits of the data pointer) is set to the value B_{16} in order to address the MSR. Execution of this instruction transfers the contents of the Accumulator into the MSR, and the Display Controller begins operating according to the following table:

M_3	M_2	M_1	M_0	DISPLAY CONTROLLER OPERATION
0	0	0	0	Reset (S_{0-7}: High level); (T_{0-5}: OFF)
0	0	0	1	8-bit parallel output: $S_{0-3} \leftarrow$ (0EH); $S_{4-7} \leftarrow$ (0FH); (T_{0-3}: OFF)
0	0	1	0	Not used
0	0	1	1	Not used
0	1	0	0	4-digit display (T_{0-3}); Segment data: 00H-07H
0	1	0	1	5-digit display (T_{0-4}); Segment data: 00H-09H
0	1	1	0	6-digit display (T_{0-5}); Segment data: 00H-0BH
0	1	1	1	8-digit display (T_{0-7}); Segment data: 00H-0FH
1	0	0	0	Not used
1	0	0	1	8-bit parallel output: $S_{0-3} \leftarrow$ (2EH); $S_{4-7} \leftarrow$ (2FH); (T_{0-3}: OFF)
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	4-digit display (T_{0-3}); Segment data: 20H-27H
1	1	0	1	5-digit display (T_{0-4}); Segment data: 20H-29H
1	1	1	0	6-digit display (T_{0-5}); Segment data: 20H-2BH
1	1	1	1	8-digit display (T_{0-7}); Segment data: 20H-2FH

The MSB, M_3, of the Mode Select Register defines the Row of RAM (0 or 2) to be used for the Display Buffer and M_2 distinguishes between a digit strobe cycle output, or a direct latched output.

INSTRUCTION SET SYMBOL DEFINITIONS

The following abbreviations are used in the description of the μPD7520 instruction set:

SYMBOL	EXPLANATION AND USE
A	Accumulator
address	Immediate address
C	Carry Flag
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
H	Register H
HL	Register pair HL
L	Register L
P( )	Parallel Input/Output Port addressed by the value within the brackets
PC_n	Bit "n" of Program Counter
S	Number of bytes in next instruction when Skip Condition occurs
STACK	Stack Register
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
–	Complement
∀	LOGICAL Exclusive-OR

INSTRUCTION SET

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
LOAD													
LAI data	$A \leftarrow D_{3\text{-}0}$	Load A with 4 bits of immediate data; execute succeeding LAI instructions as NOP instructions	0	0	0	1	D_3	D_2	D_1	D_0	1	1	String
LHI data	$H \leftarrow D_{1\text{-}0}$	Load H with 2 bits of immediate data	0	0	1	0	1	0	D_1	D_0	1	1	
LHLI data	$HL \leftarrow D_{4\text{-}0}$	Load HL with 5 bits of immediate data; execute succeeding LHLI instructions as NOP instructions	1	1	0	D_4	D_3	D_2	D_1	D_0	1	1	String
LAMT	$A \leftarrow [PC_{9\text{-}6}, 0, C, A]_H$	Load the upper 4 bits of ROM Table Data at address $PC_{9\text{-}6}$, 0, C, A to A	0	1	0	1	1	1	1	0	1	2	
	$(HL) \leftarrow [PC_{9\text{-}6}, 0, C, A]_L$	Load the lower 4 bits of ROM Table Data at address $PC_{9\text{-}6}$, 0, C, A to the RAM location addressed by HL											
L	$A \leftarrow (HL)$	Load A with the contents of RAM addressed by HL	0	1	0	1	0	0	1	0	1	1	
LIS	$A \leftarrow (HL)$ $L = L + 1$ Skip if L = 0H	Load A with the contents of RAM addressed by HL; increment L; skip if L = 0H	0	1	0	1	0	0	0	1	1	1 + S	L = 0H
LDS	$A \leftarrow (HL)$ $L = L - 1$ Skip if L = FH	Load A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	0	0	0	1	1 + S	L = FH
LADR address	$A \leftarrow (D_{5\text{-}0})$	Load A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	2	2	
STORE													
ST	$(HL) \leftarrow A$	Store A into the RAM location addressed by HL	0	1	0	1	0	1	1	1	1	1	
STII data	$(HL) \leftarrow D_{3\text{-}0}$ $L \leftarrow L + 1$	Store 4 bits of immediate data into the RAM location addressed by HL; increment L	0	1	0	0	D_3	D_2	D_1	D_0	1	1	

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
EXCHANGE													
XAH	$A_{1-0} \leftrightarrow H_{1-0}$ $A_{3-2} \leftarrow 00H$	Exchange A with H	0	1	1	1	1	0	1	0	1	1	
XAL	$A \leftrightarrow L$	Exchange A with L	0	1	1	1	1	0	1	1	1	1	
X	$A \leftrightarrow (HL)$	Exchange A with the contents of RAM addressed by HL	0	1	0	1	0	1	1	0	1	1	
XIS	$A \leftrightarrow (HL)$ $L \leftarrow L + 1$ Skip if L = 0H	Exchange A with the contents of RAM addressed by HL; increment L; skip if L = 0H	0	1	0	1	0	1	0	1	1	1 + S	L = 0H
XDS	$A \leftrightarrow (HL)$ $L \leftarrow L - 1$ Skip if L = FH	Exchange A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	1	0	0	1	1 + S	L = FH
XADR address	$A \leftrightarrow (D_{5-0})$	Exchange A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	2	2	
ARITHMETIC AND LOGICAL													
AISC data	$A \leftarrow A + D_{3-0}$ Skip if overflow	Add 4 bits of immediate data to A; Skip if overflow is generated	0	0	0	0	D_3	D_2	D_1	D_0	1	1 + S	Overflow
ASC	$A \leftarrow A + (HL)$ Skip if overflow	Add the contents of RAM addressed by HL to A; skip if overflow is generated	0	1	1	1	1	1	0	1	1	1 + S	Overflow
ACSC	$A, C \leftarrow A + (HL) + C$ Skip if C = 1	Add the contents of RAM addressed by HL and the carry flag to A; skip if carry is generated	0	1	1	1	1	1	0	0	1	1 + S	C = 1
EXL	$A \leftarrow A \veebar (HL)$	Perform a LOGICAL Exclusive–OR operation between the contents of RAM addressed by HL and A; store the result in A	0	1	1	1	1	1	1	0	1	1	
ACCUMULATOR AND CARRY FLAG													
CMA	$A \leftarrow \overline{A}$	Complement A	0	1	1	1	1	1	1	1	1	1	
RC	$C \leftarrow 0$	Reset Carry Flag	0	1	1	1	1	0	0	0	1	1	
SC	$C \leftarrow 1$	Set Carry Flag	0	1	1	1	1	0	0	1	1	1	
INCREMENT AND DECREMENT													
ILS	$L \leftarrow L + 1$ Skip if L = 0H	Increment L; Skip if L = 0H	0	1	0	1	1	0	0	1	1	1 + S	L = 0H
IDRS address	$(D_{5-0}) \leftarrow (D_{5-0}) + 1$ Skip if (D_{5-0}) = 0H	Increment the contents of RAM addressed by 6 bits of immediate data; Skip if the contents = 0H	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	2	2 + S	(D_{5-0}) = 0H
DLS	$L \leftarrow L - 1$ Skip if L = FH	Decrement L; Skip if L = FH	0	1	0	1	1	0	0	0	1	1 + S	L = FH
DDRS address	$(D_{5-0}) \leftarrow (D_{5-0}) - 1$ Skip if (D_{5-0}) = FH	Decrement the contents of RAM addressed by 6 bits of immediate data, skip if the contents = FH	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	2	2 + S	(D_{5-0}) = FH
BIT MANIPULATION													
RMB data	$(HL)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of the RAM location addressed by HL to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(HL)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of the RAM location addressed by HL to one	0	1	1	0	1	1	D_1	D_0	1	1	
JUMP, CALL, AND RETURN													
JMP address	$PC_{9-0} \leftarrow D_{9-0}$	Jump to the address specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	0 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
JAM data	$PC_{9-8} \leftarrow D_{1-0}$ $PC_{7-4} \leftarrow A$ $PC_{3-0} \leftarrow (HL)$	Jump to the address specified by 2 bits of immediate data, A, and the RAM contents addressed by HL	0 0	0 0	1 0	1 1	1 0	1 0	1 D_1	1 D_0	2	2	
JCP address	$PC_{5-0} \leftarrow D_{5-0}$	Jump to the address specified by the higher-order bits PC_{9-6} of the PC, and 6 bits of immediate data	1	0	D_5	D_4	D_3	D_2	D_1	D_0	1	1	

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
CALL address	STACK ← PC + 2 $PC_{9-0} \leftarrow D_{9-0}$	Store a return address (PC + 2) in the stack; call the subroutine program at the location specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
CAL address	STACK ← PC + 1 $PC_{9-0} \leftarrow 01D_4D_3$ $000D_2D_1D_0$	Store a return address (PC + 1) in the stack; call the subroutine program at one of the 32 special locations specified by 5 bits of immediate data	1	1	1	D_4	D_3	D_2	D_1	D_0	1	1	
RT	PC ← STACK	Return from Subroutine	0	1	0	1	0	0	1	1	1	1	
RTS	PC ← STACK Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	1	1	0	1	1	1	1 + S	Unconditional
SKIP													
SKC	Skip if C = 1	Skip if carry flag is true	0	1	0	1	1	0	1	0	1	1 + S	C = 1
SKMBT data	Skip if $(HL)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is true	0	1	1	0	0	1	D_1	D_0	1	1 + S	$(HL)_{bit} = 1$
SKMBF data	Skip if $(HL)_{bit} = 0$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is false	0	1	1	0	0	0	D_1	D_0	1	1 + S	$(HL)_{bit} = 0$
SKABT data	Skip if $A_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of A is true	0	1	1	1	0	1	D_1	D_0	1	1 + S	$A_{bit} = 1$
SKAEI data	Skip if A = data	Skip if A equals 4 bits of immediata data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	A = data
SKAEM	Skip if A = (HL)	Skip if A equals the RAM contents addressed by HL	0	1	0	1	1	1	1	1	1	1 + S	A = (HL)
PARALLEL I/O													
IPL	A ← P(L)	Input the Port addressed by L to A	0	1	1	1	0	0	0	0	1	1	
IP1	A ← P1	Input Port 1 to A	0	1	1	1	0	0	0	1	1	1	
OPL	P(L) ← A	Output A to the port addressed by L	0	1	1	1	0	0	1	0	1	1	
OP3	$P3 \leftarrow A_{1-0}$	Output the lower 2 bits of A to Port 3	0	1	1	1	0	0	1	1	1	1	
CPU CONTROL													
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

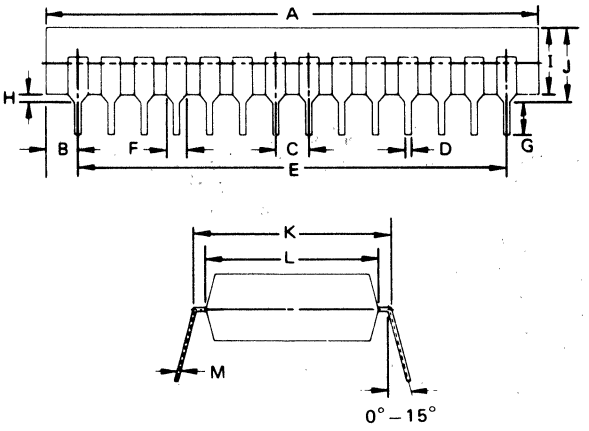
ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10° to +70°C
Storage Temperature	−40° to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltage	−15 to +0.3 Volts
Output Voltage	−15 to +0.3 Volts
Output Current (I_{OH} Total)	−100 mA
(I_{OL} Total)	90 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

PACKAGE OUTLINE
μPD7520C



PLASTIC

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$