NEC

MOS INTEGRATED CIRCUIT

μPD75336

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75336 is one of the "75X-series" 4-bit single-chip microcomputers enabled to process data with performance equivalent to that of 8-bit microcomputers.

The μPD75336 is a microcomputer with an expanded capacity of the ROM and RAM of conventional μPD75328 and an improved 8-bit data processing capacity. It can carry out A/D converter low-voltage operations.

For evaluation purposes for system development or small-quantity production, the μPD75P336 is available which is a product with the on-chip mask ROM of μPD75336 replaced with a one-time PROM.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μPD75336 User's Manual: IEU-725

FEATURES

- μPD75328 upward compatible
- Instruction execution time variable function useful for high-speed operations and power saving
  - 0.95, 1.91, 3.81, 15.3 μs (Main system clock: When operated at 4.19 MHz)
  - 122 μs (Subsystem clock: When operated at 32.768 kHz)
- Memory capacity: μPD75336 ROM: 16256 × 8 bits
  RAM: 768 × 4 bits
- On-chip 8-bit resolution A/D converter (successive approximation type): 8 channels
  - Low-voltage operation possible: V_{DD} = 2.7 to 6.0 V
- On-chip LCD controller/driver
  - Maximum of 20 × 4 segments drive possible
- Improved timer functions: 4 channels
- Improved 8-bit data processing capability
  - Transfer, add/subtract, increase/decrease and compare possible
- Ultra-compact package in use (80-pin plastic TQFP (fine pitch)(□12 mm))
- On-chip PROM (μPD75P336) operative at low voltages available
  - V_{DD} = 2.7 to 6.0 V

APPLICATIONS

Cameras, VCR integrated cameras, air conditioners, sphygmomanometers, etc.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

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ORDERING INFORMATION

Ordering Code	Package
μPD75336GC-×××-3B9	80-pin plastic QFP (□14 mm)
μPD75336GK-×××-BE9	80-pin plastic TQFP (fine pitch)(□12 mm)

Remarks "×××" is a ROM code number.

QUALITY GRADE

Ordering Code	Package	Quality Grade
μPD75336GC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD75336GK-×××-BE9	80-pin plastic TQFP (fine pitch)(□12 mm)	Standard

Remarks "×××" is a ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

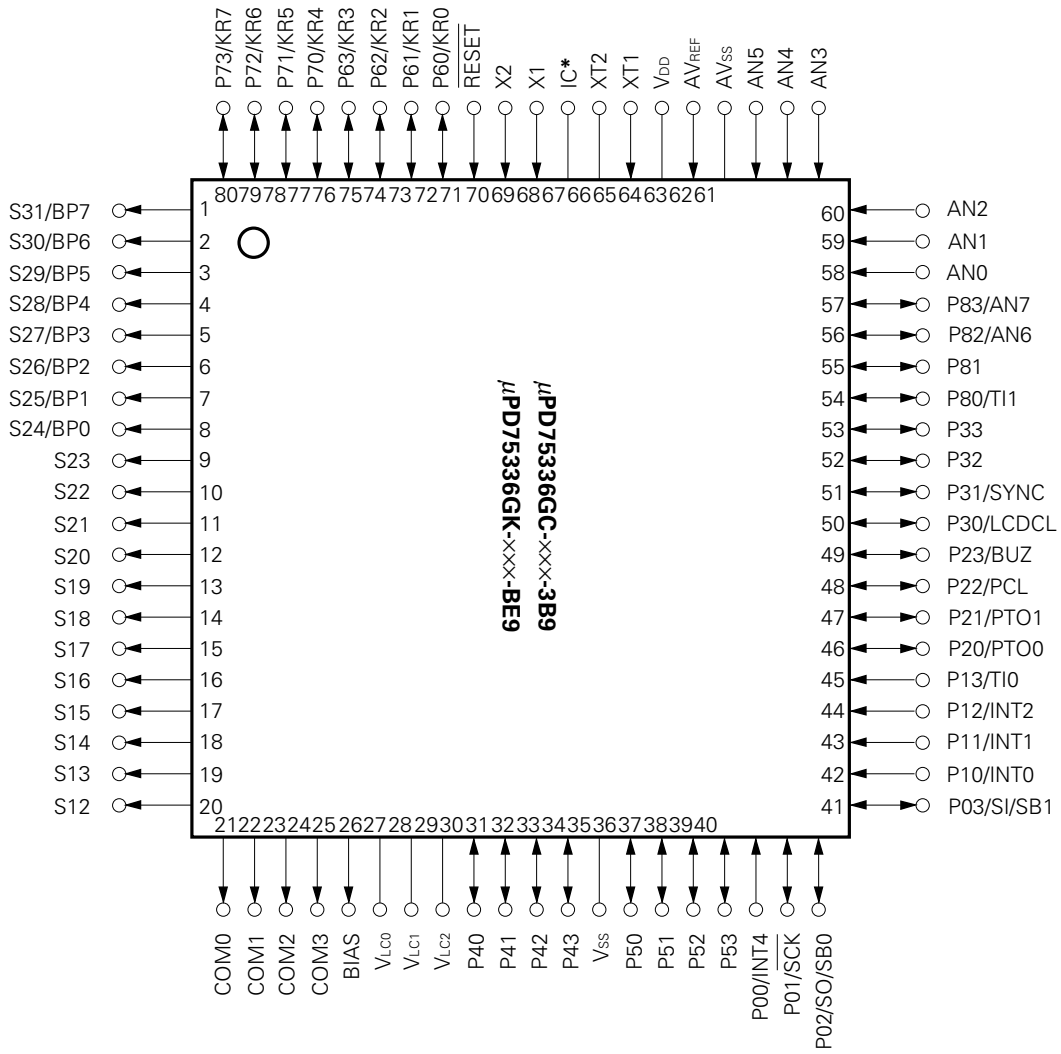
GENERAL DESCRIPTION OF FUNCTIONS

Item		Function			
Instruction execution time		When main system clock is selected: 0.95, 1.91, 3.81, 15.3 μs (when operated at 4.19 MHz) When subsystem clock is selected: 122 μs (when operated at 32.768 kHz)			
On-chip memory	ROM	16256 × 8 bits			
	RAM	768 × 4 bits			
General register		• 4-bit manipulation: 8 × 4 banks • 8-bit manipulation: 4 × 4 banks			
I/O line (The dual function pins for LCD-drive are included. The dedicated pins for LCD-drive are excluded.)	44	8 pins	CMOS input pins	Use of pull-up resistor enabled by software (except P00)	
		20 pins	CMOS input/output pin		
		8 pins	CMOS output pin	Dual function with segment pins	
		8 pins	N-ch open-drain input/output	10 V withstand voltage. On-chip specification of pull-up resistor enabled by mask option	
LCD controller/driver		• Output pins for LCD-drive • Segment output pins: 20 pins (dual-function pins with CMOS output: 8 pins) • Common output pins: 4 pins • Maximum 20 × 4 segment drive • Display mode selection: Static 1/2, 1/3, 1/4 duties			
A/D converter		On-chip 8-bit resolution A/D converter (successive approximation type) • 8-channel analog input • Low-voltage operable V_{DD} = 2.7 to 6.0 V • A/D conversion speed 40.1 μs (when operated at 4.19 MHz)			
Timer		4 channels { • 8-bit timer/event counter × 2 channels • 8-bit basic interval timer • Watch timer ... 0.5 sec time interval generation, buzzer output possible (2 kHz, 4 kHz, 32 kHz)			
Serial interface		• NEC standard serial bus interface (SBI) • Clocked serial interface			
Bit sequential buffer		Special bit manipulation memory: 16 bits			
Clock output (PCL)		Φ, 524 kHz, 262 kHz, 65.5 kHz (when operated at 4.19 MHz)			
Buzzer output (BUZ)		2 kHz, 4 kHz, 32 kHz (with main system clock or subsystem clock in operation)			
Vectored interrupt		• External: 3 • Internal: 4			
Test input		• External: 1 • Internal: 1			
8-bit data processing		Transfer, add/subtract, increase/decrease and compare			
System clock oscillator		• Ceramic/crystal oscillator for main system clock oscillation: 4.194304 MHz • Crystal oscillator for subsystem clock oscillation : 32.768 kHz			
Standby		STOP/HALT mode			
Operating voltage		V_{DD} = 2.7 to 6.0 V			
Package		• 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (fine pitch)(□12 mm)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (□14 mm)**
- **80-pin plastic TQFP (fine pitch)(□12 mm)**



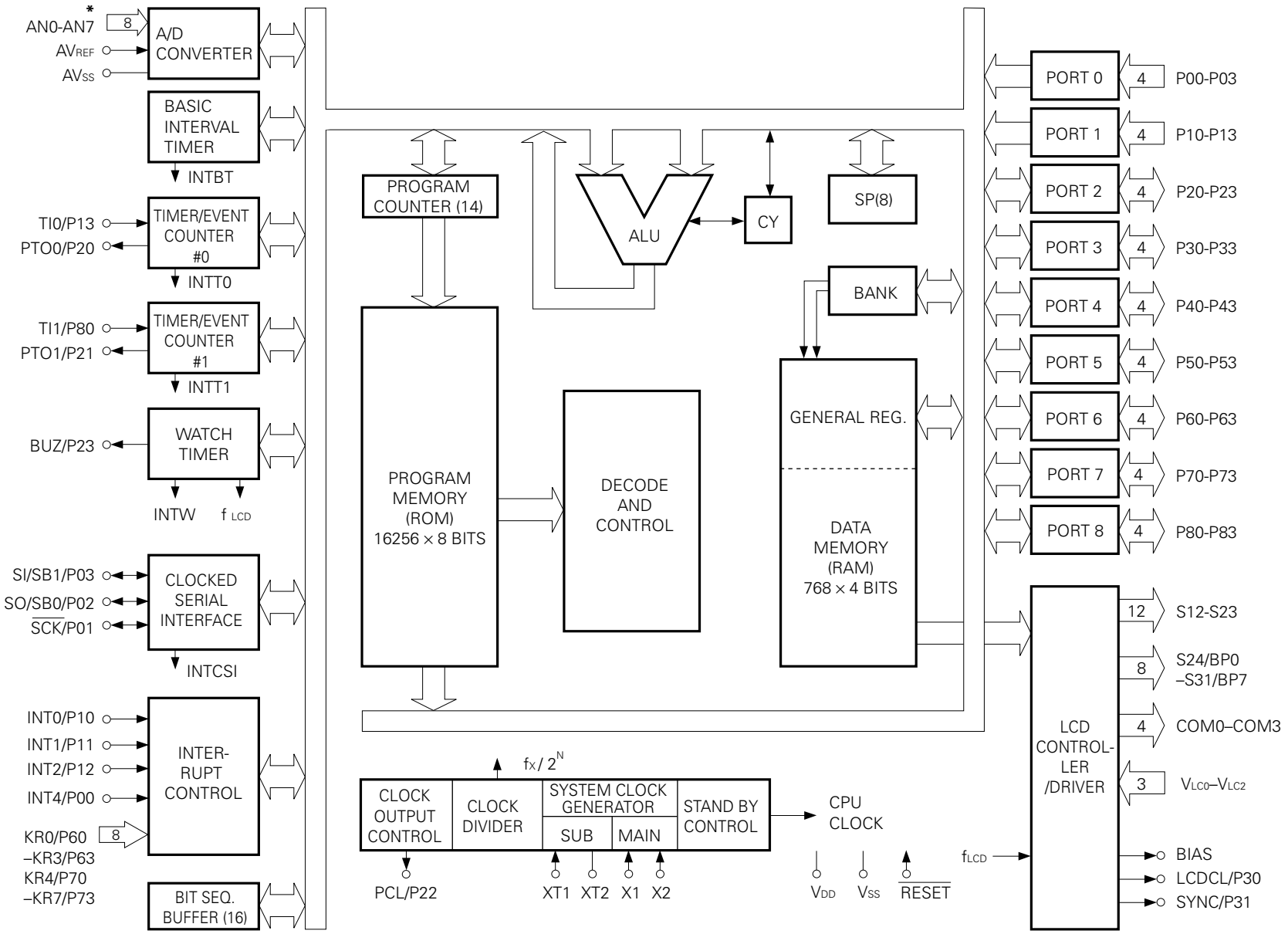
***** Internally connected. Connect the IC PIN to V_{DD} directly.

PIN NAMES

P00 to P03 : Port 0
P10 to P13 : Port 1
P20 to P23 : Port 2
P30 to P33 : Port 3
P40 to P43 : Port 4
P50 to P53 : Port 5
P60 to P63 : Port 6
P70 to P73 : Port 7
P80 to P83 : Port 8
BP0 to BP7 : Bit Port 0 to 7
KR0 to KR7 : Key Return 0 to 7
AV_{REF} : Analog Reference
AV_{SS} : Analog Ground
AN0 to AN7 : Analog Input 0 to 7
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output

SB0,1 : Serial Bus 0, 1
$\overline{RESET}$: Reset
S12 to S31 : Segment Output 12 to 31
COM0 to COM3 : Common Output 0 to 3
V_{LC0} to V_{LC2} : LCD Power Supply 0 to 2
BIAS : LCD Power Supply Bias Control
LCDCL : LCD Clock
SYNC : LCD Synchronization
TI0, 1 : Timer Input 0, 1
PTO0, 1 : Programmable Timer Output 0, 1
BUZ : Buzzer Clock
PCL : Programmable Clock
INT0, 1, 4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Input 2
X1, 2 : Main System Clock Oscillation 1, 2
XT1, 2 : Subsystem Clock Oscillation 1, 2
IC : Internally Connected
V_{DD} : Positive Power Supply
V_{SS} : Ground

2. BLOCK DIAGRAM



* AN6/P82, AN7/P83

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0) Pull-up resistor can be used for P01 to P03 as a 3-bit unit by software.	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ - A
P02	Input/output	SO/SB0				Ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ - C
P11		INT1	4-bit input port (PORT 1) Pull-up resistor can be used as a 4-bit unit by software.			
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT 2) Pull-up resistor can be used as a 4-bit unit by software.	×	Input	E - B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL	Programmable 4-bit input/output port (PORT 3) Input/output can be specified bit-wise. Pull-up resistor can be used as a 4-bit unit by software.	×	Input	E - B
P31 *2		SYNC				
P32 *2		—				
P33 *2		—				
P40 to P43 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4) On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: 10 V withstand voltage	○	High level (on-chip pull-up resistor) or high-impedance	M
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: 10 V withstand voltage		High level (on-chip pull-up resistor) or high-impedance	M

* **1.** ◯ : Schmitt triggered input
2. LED direct drive possible

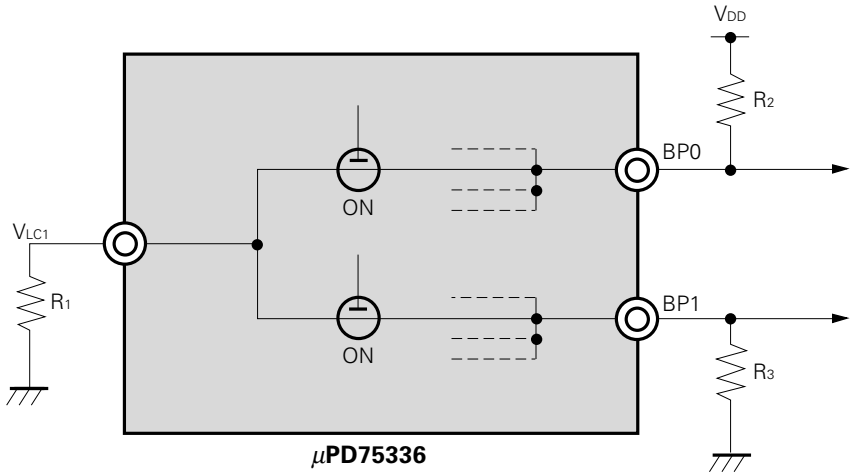
3.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	Reset	I/O Circuit Type *1
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT 6) Input/output can be specified bit-wise. Pull-up resistor can be used as a 4-bit unit by software.	○	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT 7) Pull-up resistor can be used as a 4-bit unit by software.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				
P80	Input/output	TI1	4-bit input/output port (PORT 8) Pull-up resistor can be used as a 4-bit unit by software.	×	Input	Ⓔ - E
P81		—				E - B
P82		AN6				Y - B
P83		AN7				
BP0	Output	S24	1-bit output port (BIT PORT) Also used as segment output pin.	×	* 2	G - C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

* **1.** ◯ : Schmitt triggered input

2. BP0 to BP7 select V_{LC1} as the input source.
However, the output level depends on BP0 to BP7 and V_{LC1} external circuit.

Example BP0 to BP7 are connected mutually within the μPD75336 as shown below. Therefore, the output level of BP0 to BP7 is determined by the value of R_1, R_2 and R_3.



3.2 NON-PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function		Reset	I/O Circuit Type *
TI0	Input	P13	External event pulse input to timer/event counter		Input	Ⓑ - C
TI1		P80				Ⓔ - E
PTO0	Output	P20	Timer/event counter output		Input	E - B
PTO1		P21				
PCL	Output	P22	Clock output		Input	E - B
BUZ	Output	P23	Fixed frequency output (for buzzer or system clock trimming)		Input	E - B
$\overline{SCK}$	Input/output	P01	Serial clock input/output		Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output Serial bus input/output		Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input Serial bus input/output		Input	Ⓜ - C
INT4	Input	P00	Edge detection vectored interrupt input (both rising edge and falling edge detection effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input (detection edge selectable)	Clocked	Input	Ⓑ - C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	Input	Ⓑ - C
KR0 to KR3	Input	P60 to P63	Parallel falling edge detection testable input		Input	Ⓕ - A
KR4 to KR7	Input	P70 to P73	Parallel falling edge detection testable input		Input	Ⓕ - A
X1	Input	—	Main system clock oscillation crystal/ceramic connection pin. For external clock, the external clock signal is input to X1 and its opposite phase is input to X2.		—	—
X2						
XT1	Input	—	Subsystem clock oscillation crystal connection pin. For external clock, the external clock signal is input to XT1 and XT2 is opened. XT1 can be used as a 1-bit input (test).		—	—
XT2	—					
$\overline{RESET}$	Input	—	System reset input		—	Ⓑ
IC	—	—	Internally Connected. Connect the IC pin to V_{DD} directly.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	GND potential		—	—

* ◯ : Schmitt triggered input

3.2 NON-PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	Reset	I/O Circuit Type
S12 to S23	Output	—	Segment signal output	***2**	G - A
S24 to S31	Output	BP0 to BP7	Segment signal output	***2**	G - C
COM0 to COM3	Output	—	Common signal output	***2**	G - B
V_{LC0} to V_{LC2}	Input	—	LCD drive power supply with on-chip split resistor (mask option)	—	—
BIAS	Output	—	Externally mounted split resistor cut output	***3**	—
LCDCL ***1**	Output	P30	Clock output for driving the externally extended driver	Input	E - B
SYNC ***1**	Output	P31	Clock output for synchronizing the externally extended driver	Input	E - B
AN0 to AN5	Input	—	A/D converter analogs signal input	Input	Y
AN6		P82			Y - B
AN7		P83			
AV_{REF}	Input	—	A/D converter reference voltage input	—	Z
AV_{SS}	—	—	A/D converter GND potential	—	Z

***** **1.** Reserved pins for future system extension. They are used now only as P30 and P31 pins.

2. For each display output, V_{LCX} is selected as the input source.

S12 to S31 : V_{LC1}
COM0 to COM2 : V_{LC2}
COM3 : V_{LC0}

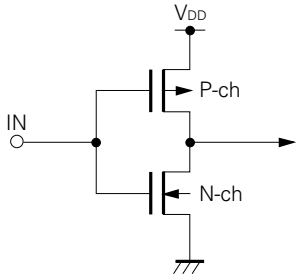
Each display output level varies depending on each display output and V_{LCX} external circuit.

3. Low level if there is an on-chip split resistor.
High impedance if there is no on-chip split resistor.

3.3 PIN INPUT/OUTPUT CIRCUITS

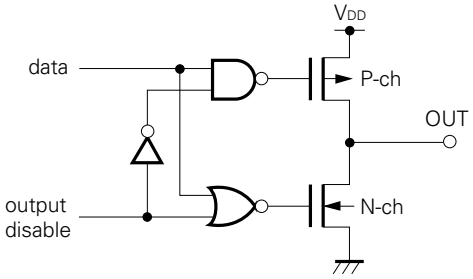
Input/output circuits of μPD75336 pins are shown in schematic form.

TYPE A (For TYPE E-B)



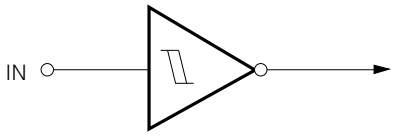
CMOS Standard Input Buffer

TYPE D (For TYPE E-B, F-A)



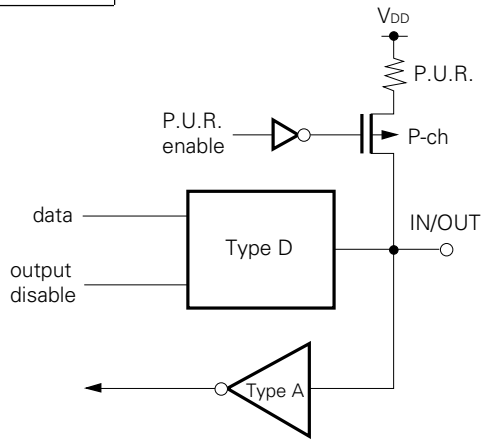
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

TYPE B



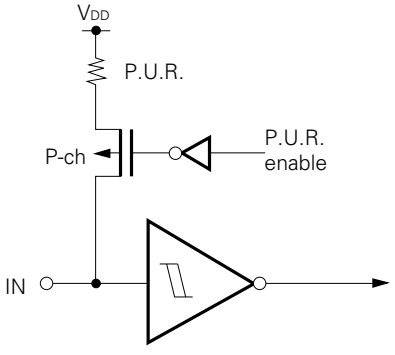
Schmitt-Triggered Input with Hysteresis Characteristic

TYPE E-B



P.U.R.:Pull-Up Resistor

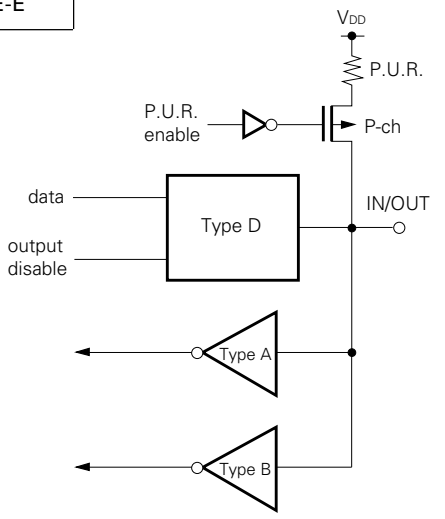
TYPE B-C



P.U.R. : Pull-Up Resistor

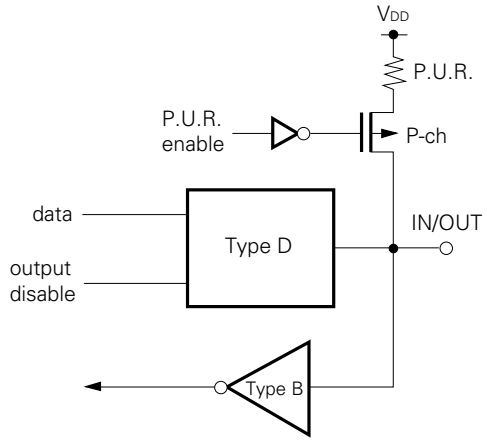
Schmitt-Triggered Input with Hysteresis Characteristic

TYPE E-E



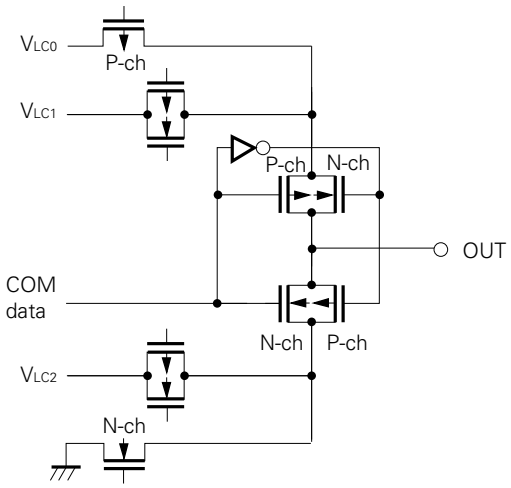
P.U.R.:Pull-Up Resistor

TYPE F-A

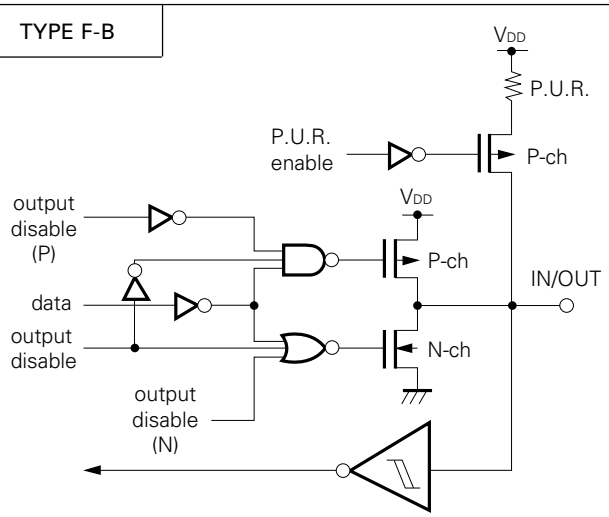


P.U.R.:Pull-Up Resistor

TYPE G-B

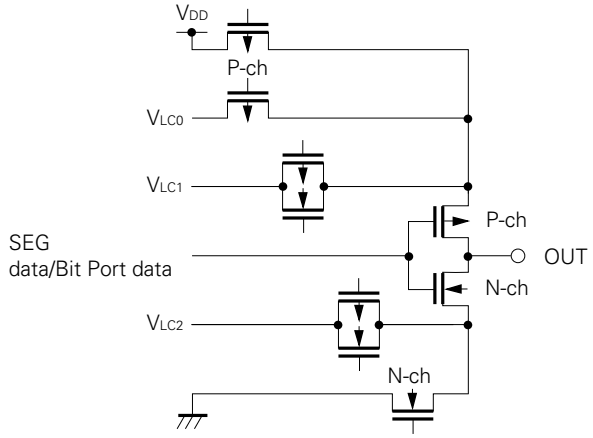


TYPE F-B

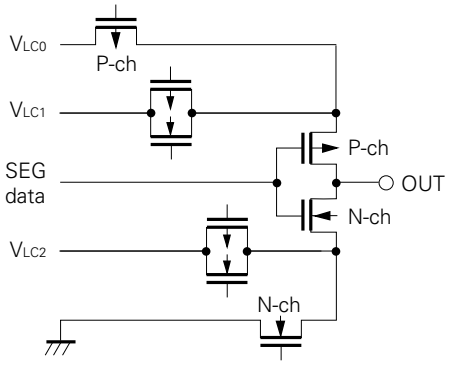


P.U.R.:Pull-Up Resistor

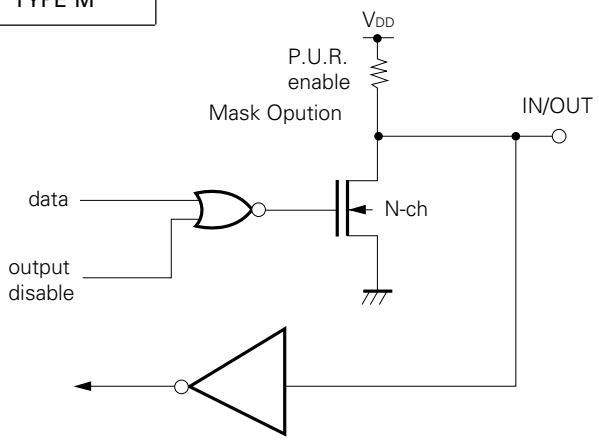
TYPE G-C



TYPE G-A

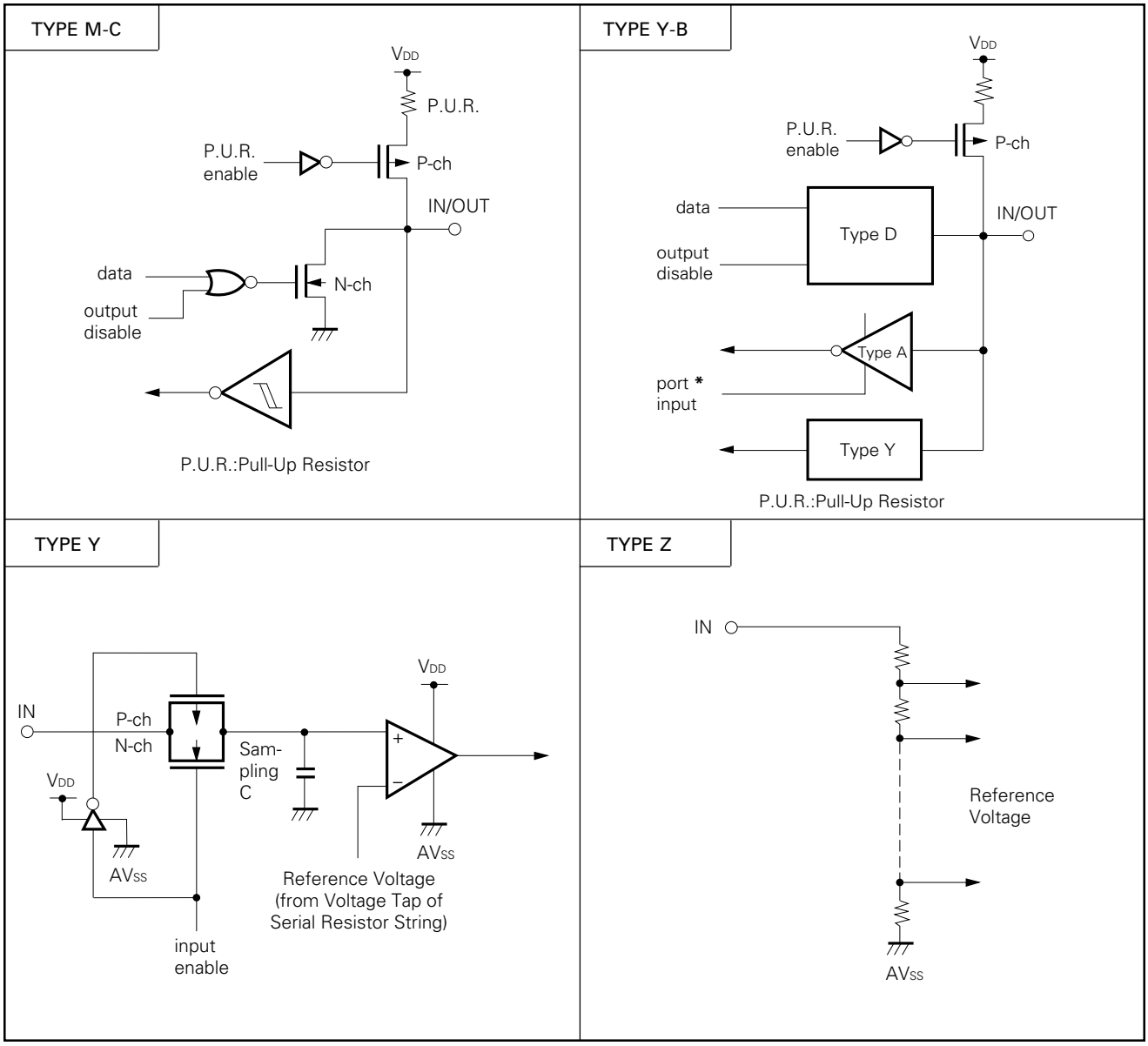


TYPE M



Middle-High Voltage Input Buffer
(+10 V Withstand Voltage)

P.U.R.:Pull-Up Resistor



* This becomes active in executing input instruction.

3.4 MASK OPTION SELECTION

The following mask options are available for the pins.

Pin	Mask Option	
P40 to P43, P50 to P53	① Pull-up resistor not available (specifiable bit-wise)	② Pull-up resistor available (specifiable bit-wise)
V_{LC0} to V_{LC2}, BIAS	① Split resistor available for LCD drive power supply (specifiable in 4 units)	② Split resistor not available for LCD drive power supply (specifiable in 4 units)
XT1, XT2	① Feedback resistor available (when subsystem clock is used)	② Feedback resistor not available (when subsystem clock is not used)

3.5 RECOMMENDED CONNECTION OF UNUSED PINS

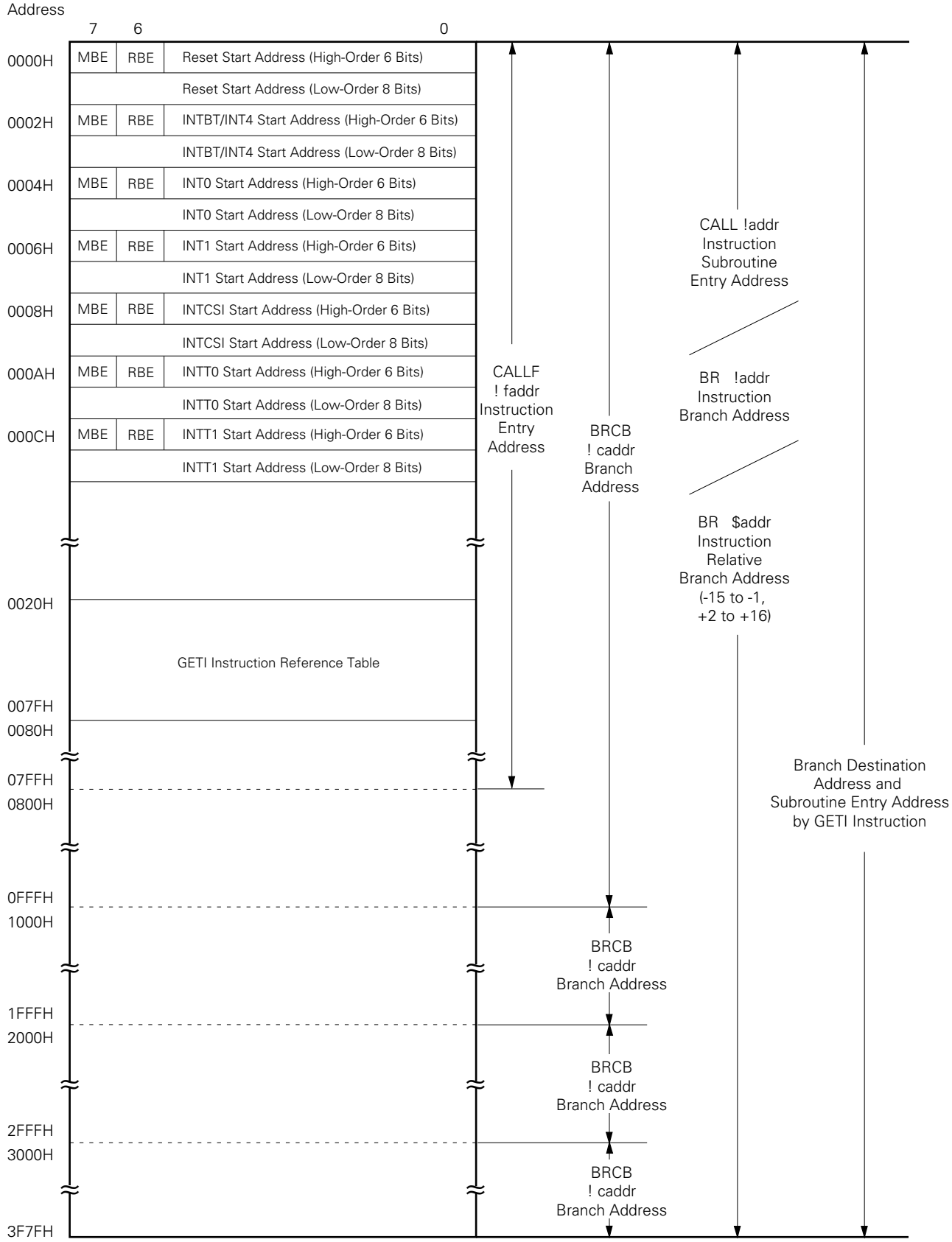
Pin	Recommended Connection
P00/INT4	Connect to V_{SS}.
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}.
P02/SO/SB0	
P03/SI/SB1	
P10/INT0 to P12/INT2	Connect to V_{SS}.
P13/TI0	Input status : Connect to V_{SS} or V_{DD}. Output status: Leave open.
P20/PTO0	
P21/PTO1	
P22/PCL	
P23/BUZ	
P30 to P33	
P40 to P43	
P50 to P53	
P60 to P63	
P70 to P73	
P80, P81	
P82/AN6, P83/AN7	
S12 to S23	Leave open.
S24/BP0 to S31/BP7	
COM0 to COM3	
V_{LC0} to V_{LC2}	Connect to V_{SS}.
BIAS	Connect to V_{SS} only when none of V_{LC0} to V_{LC2} are used. Leave open in all other cases.
XT1	Connect to V_{SS} or V_{DD}.
XT2	Leave open.
AN0 to AN5	Connect to V_{SS} or V_{DD}.
IC	Connect to V_{DD} directly.

4. MEMORY CONFIGURATION

- Program memory (ROM) .....16256 × 8 bits (0000H to 3F7FH)
  - · 0000H, 0001H : Vector table for writing the program start address by restart
  - · 0002H to 000DH : Vector table for writing the program start address by interrupt
  - · 0020H to 007FH : Table area referred to by GETI instruction

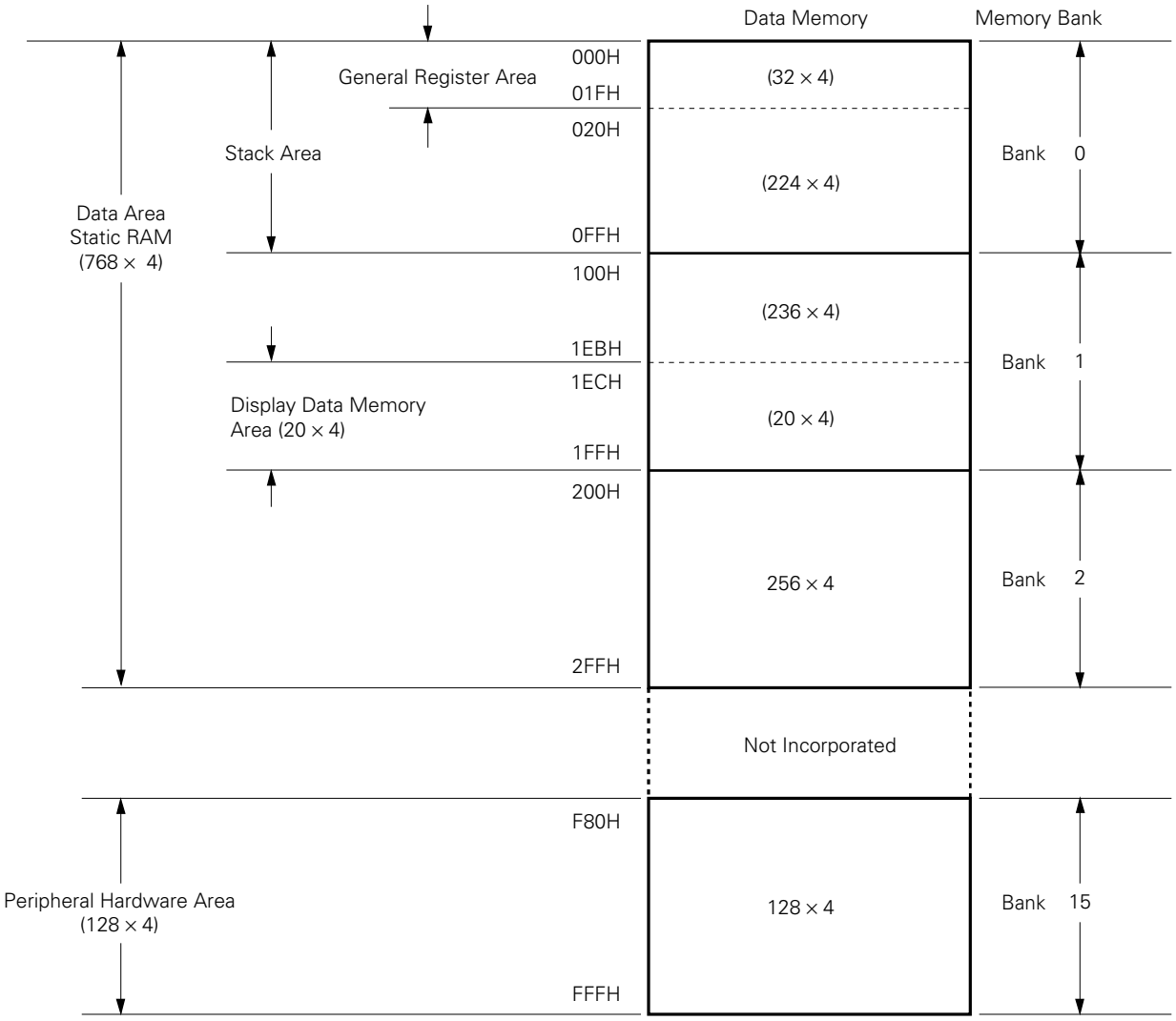
- Data memory
  - · Data area ...768 × 4 bits (000H to 2FFH)
  - ·Peripheral hardware area ...128 × 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map



Remarks Apart from the cases above, branching is possible to an address for which the PC low-order 8 bits only have been changed, by the BR PCDE or BR PCXA instruction.

Fig. 4-2 Data Memory Map



Remarks Banks 0, 1, 2 : 256 × 4 bits
Bank 15 : 128 × 4 bits

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

There are four types of I/O port as follows.

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 6, 7, 8) : 20
- CMOS output (BIT PORT) : 8
- N-ch open-drain input/output (PORT4, 5) : 8

Total 44

Table 5-1 Port Functions

Port (Symbol)	Function	Operation/Features	Remarks
PORT 0 PORT 1	4-bit input	Regardless of the operating mode of the shared pin, reading or test is always possible.	Dual-function pins as SO/SB0, SI/SB1, $\overline{SCK}$, INT0 to INT2, INT4 and TI0
PORT 3 * PORT 6	4-bit input/output	Can be set in the input or output mode bit-wise	Dual-function pins as LCDCL and SYNC.
			Dual-function pins as KR0 to KR3.
PORT 2		Can be set in the input or output mode as a 4-bit unit. Port 6 and Port 7 are paired for input and output of data as an 8-bit unit.	Dual-function pins as PTO0, PTO1, PCL and BUZ in port 2.
PORT 7			Dual-function pins as KR4 to KR7.
PORT 8			Dual-function pins as TI1, AN6 and AN7
PORT 4 * PORT 5 *	4-bit input/output (N-ch open-drain 10 V withstand voltage)	Can be set in the input or output mode as a 4-bit unit. Port 4 and port 5 are paired for input and output of data as an 8-bit unit.	In the case of the mask option, on-chip pull-up resistors can be specified bit-wise.
BP0 to BP7	1-bit output	Data are output bit-wise. Can be switched with LCD driver segment outputs S24 to S31 through software.	

* LED can be directly driven.

5.2 CLOCK GENERATOR

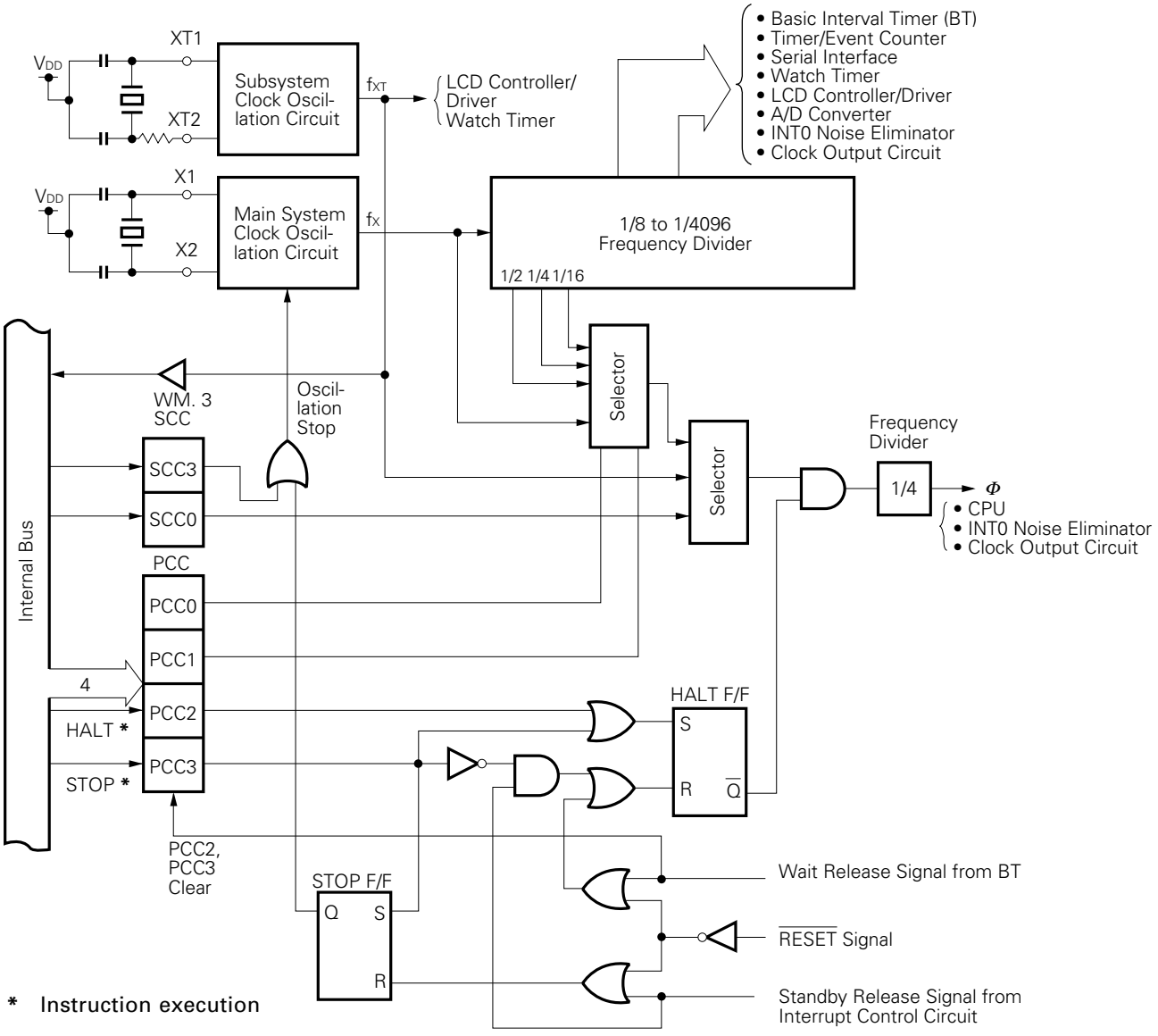
Clock generator operation is determined by the processor clock control register (PCC) and the system clock control register (SCC).

There are two types of clock: main system clock and subsystem clock.

The instruction execution time can also be changed.

- 0.95 μs/1.91 μs/3.81 μs/15.3 μs (main system clock: at 4.19 MHz operation)
- 122 μs (subsystem clock: at 32.768 kHz operation)

Fig. 5-1 Block Diagram of Clock Generator



* Instruction execution

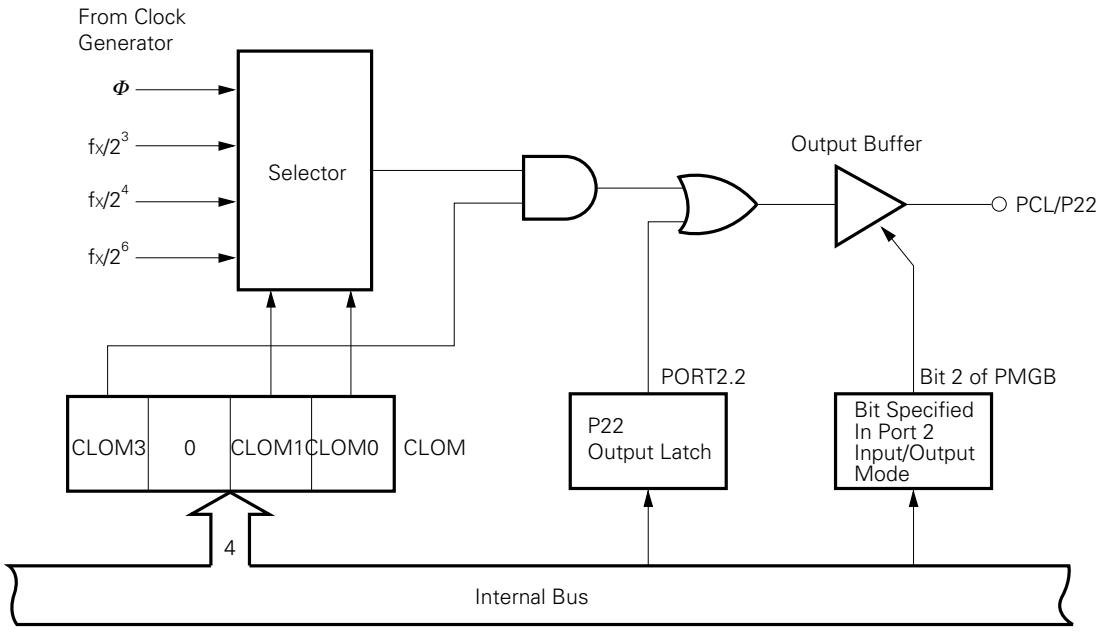
Remarks
1. fX = Main system clock frequency
2. fXT = Subsystem clock frequency
3. Φ = CPU clock
4. PCC: Processor clock control register
5. SCC: System clock control register
6. 1 clock cycle of Φ (tCY) is 1 machine cycle of instruction. For tCY, refer to "AC CHARACTERISTICS" in **10. "ELECTRICAL SPECIFICATIONS"**.

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit is intended to output clock pulses from the P22/PCL pin and is used for remote control or to supply clock pulses to peripheral LSIs.

- Clock output (PCL): Φ, 524 kHz, 262 kHz, 65.5 kHz (at 4.19 MHz operation)

Fig. 5-2 Clock Output Circuit Configuration



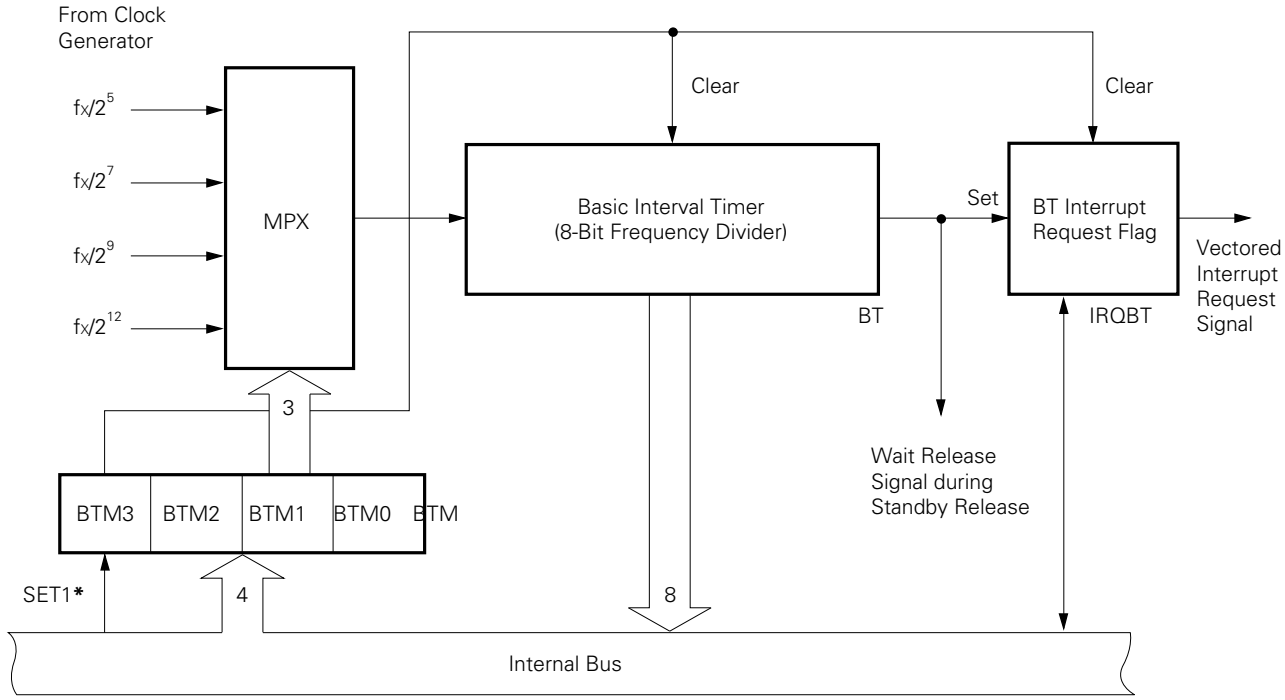
Remarks The clock circuit is so configured that short-width pulses are not generated when clock output enable/disable is switched.

5.4 BASIC INTERVAL TIMER

The basic interval timer has the following functions:

- Interval timer operation to generate reference time interrupts
- Watchdog timer application to detect program runaway
- Wait time selection and count after the standby mode is released
- Count content read

Fig. 5-3 Basic Interval Timer Configuration



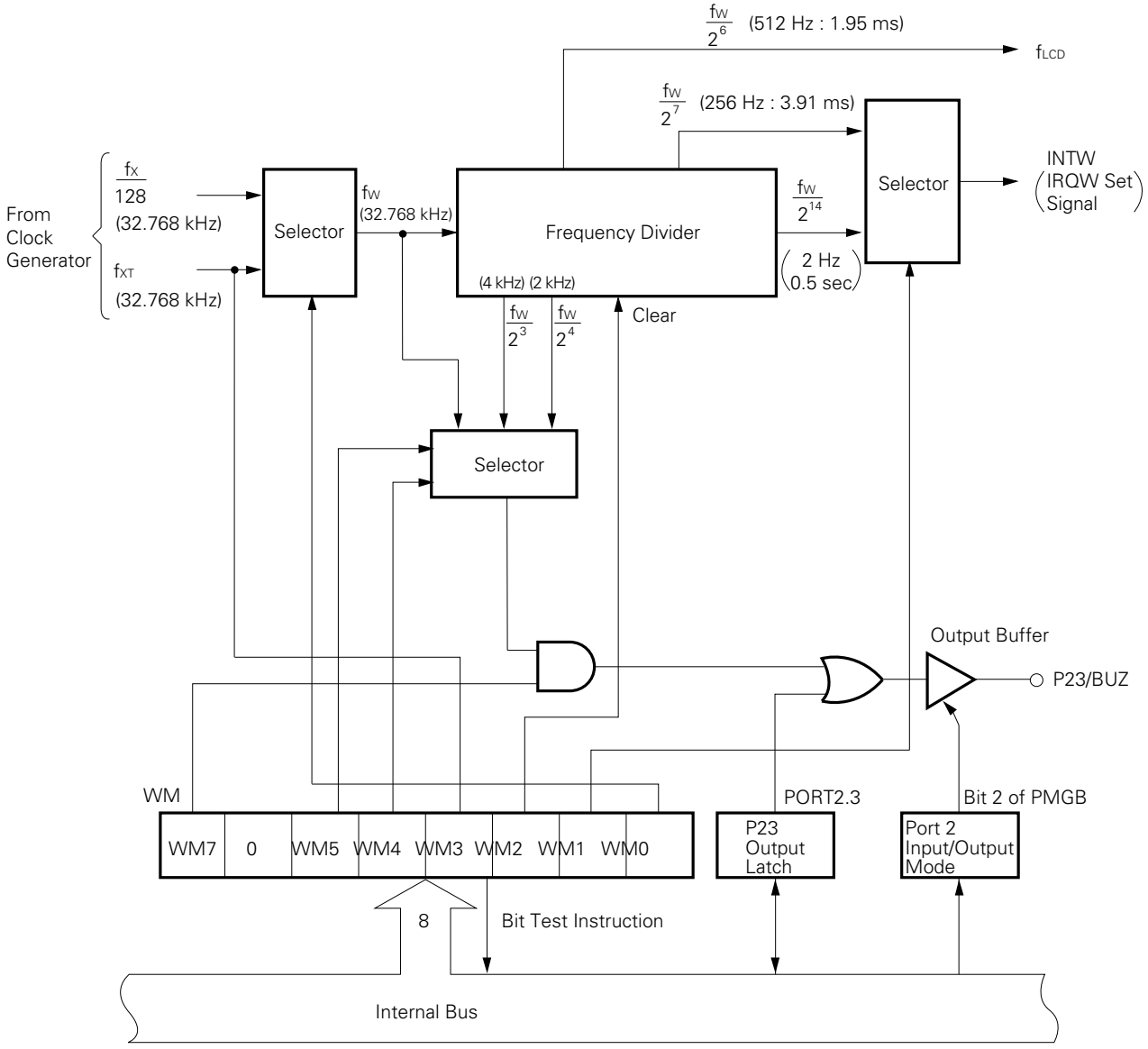
* Instruction execution

5.5 WATCH TIMER

The μPD75336 has one-channel on-chip watch timer. The watch timer has the following functions.

- Sets the test flag (IRQW) at a 0.5 sec. time interval.
  Can release the standby mode by IRQW.
- Can generate the 0.5 sec. time interval with the main system clock or the subsystem clock.
- Can carry out program debugging or inspection efficiently in the fast feed mode with a time interval set to 3.91 μs (128 times the normal feed mode).
- Can generate a frequency of 2.048, 4.096 or 32.768 kHz to the P23/BUZ pin to generate buzzer sound or trim the system clock oscillation frequency.
- Can start the watch at zero second since it can clear the divider.

Fig. 5-4 Block Diagram of Watch Timer



Values in parentheses are when fX = 4.194304 MHz and fXT = 32.768 kHz.

5.6 TIMER/EVENT COUNTER

(1) Timer/event counter configuration

The μPD75336 has two channels of timer/event counters.

Channels 0 and 1 of the timer/event counter have the following differences.

Table 5-2 Differences between Timer/Event Counter Channel 0 and Channel 1

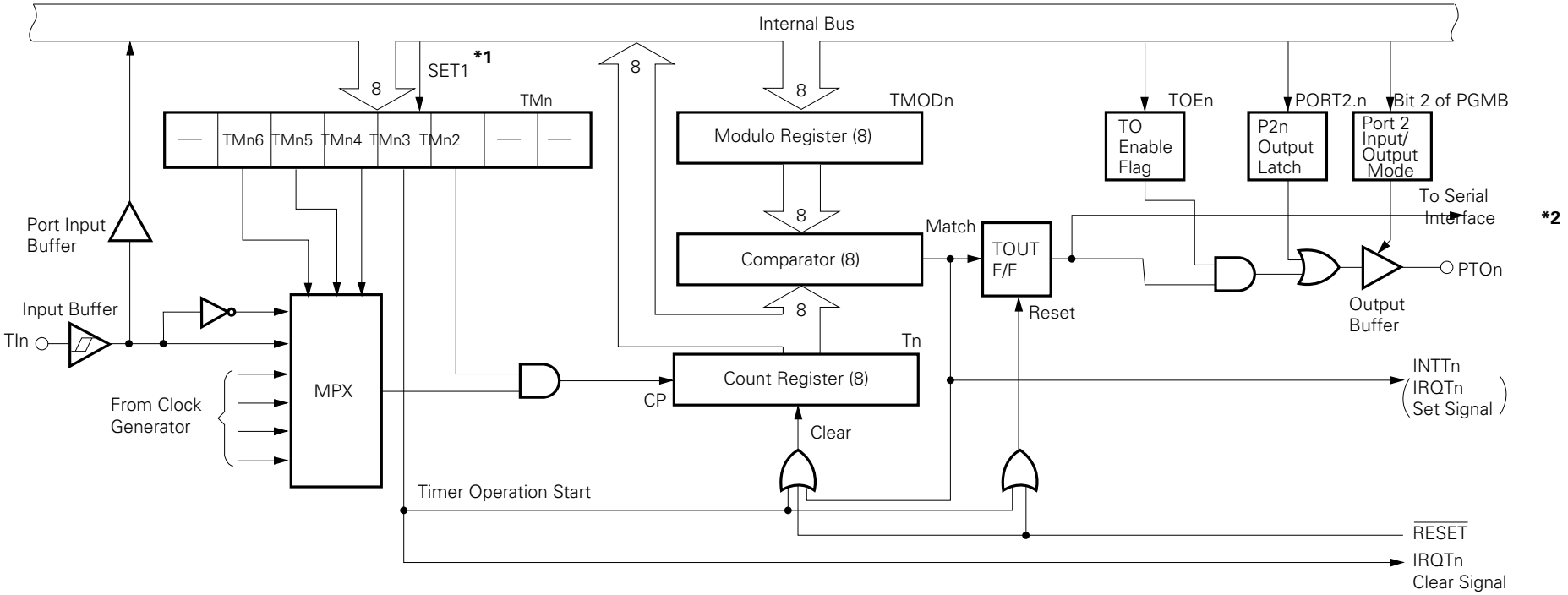
Differences	Channel 0	Channel 1
Selection count pulse	$f_X/2^{10}$, $f_X/2^8$, $f_X/2^6$, $f_X/2^4$,	$f_X/2^{12}$, $f_X/2^{10}$, $f_X/2^8$, $f_X/2^6$
Clock supply to the serial interface	Possible	Impossible

(2) Timer/event counter functions

The timer/event counter functions are:

- Programmable interval timer operation
- Output of square wave having any selected frequency to the PTOn pin
- Event counter operation
- Output of N-divided TIn pin input to the PTOn pin (frequency divider operation)
- Serial shift clock supply to the serial interface circuit
- Count status call function

Fig. 5-5 Timer/Event Counter Block Diagram



Remarks n = 0, 1 (n indicates channel number)

* **1.** Instruction execution

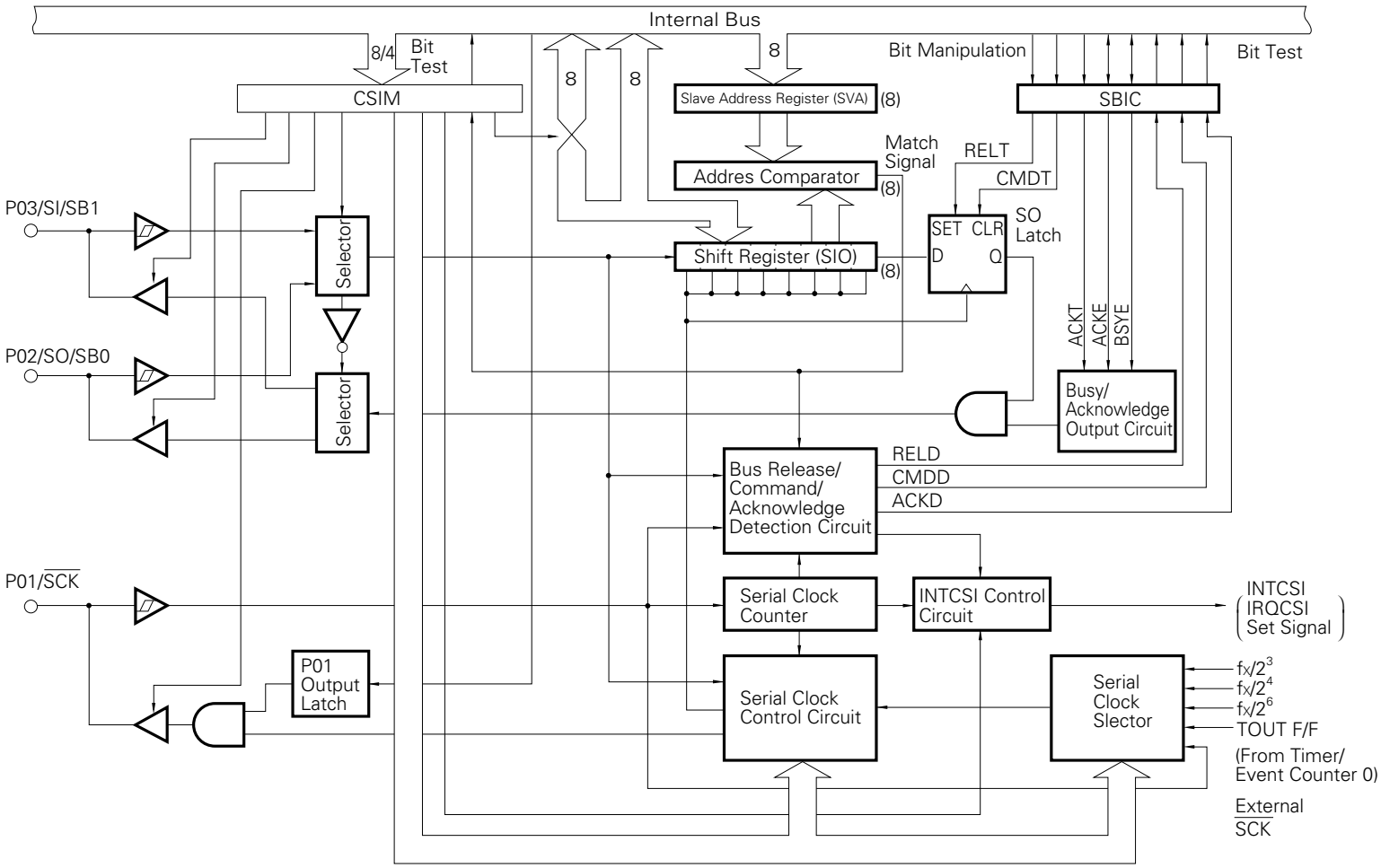
2. Only from channel 0 of timer/event counter

5.7 SERIAL INTERFACE

The μPD75336 incorporates a clocked 8-bit serial interface, with four modes available.

- Operation-halted mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode (serial bus interface mode)

Fig. 5-6 Serial Interface Block Diagram



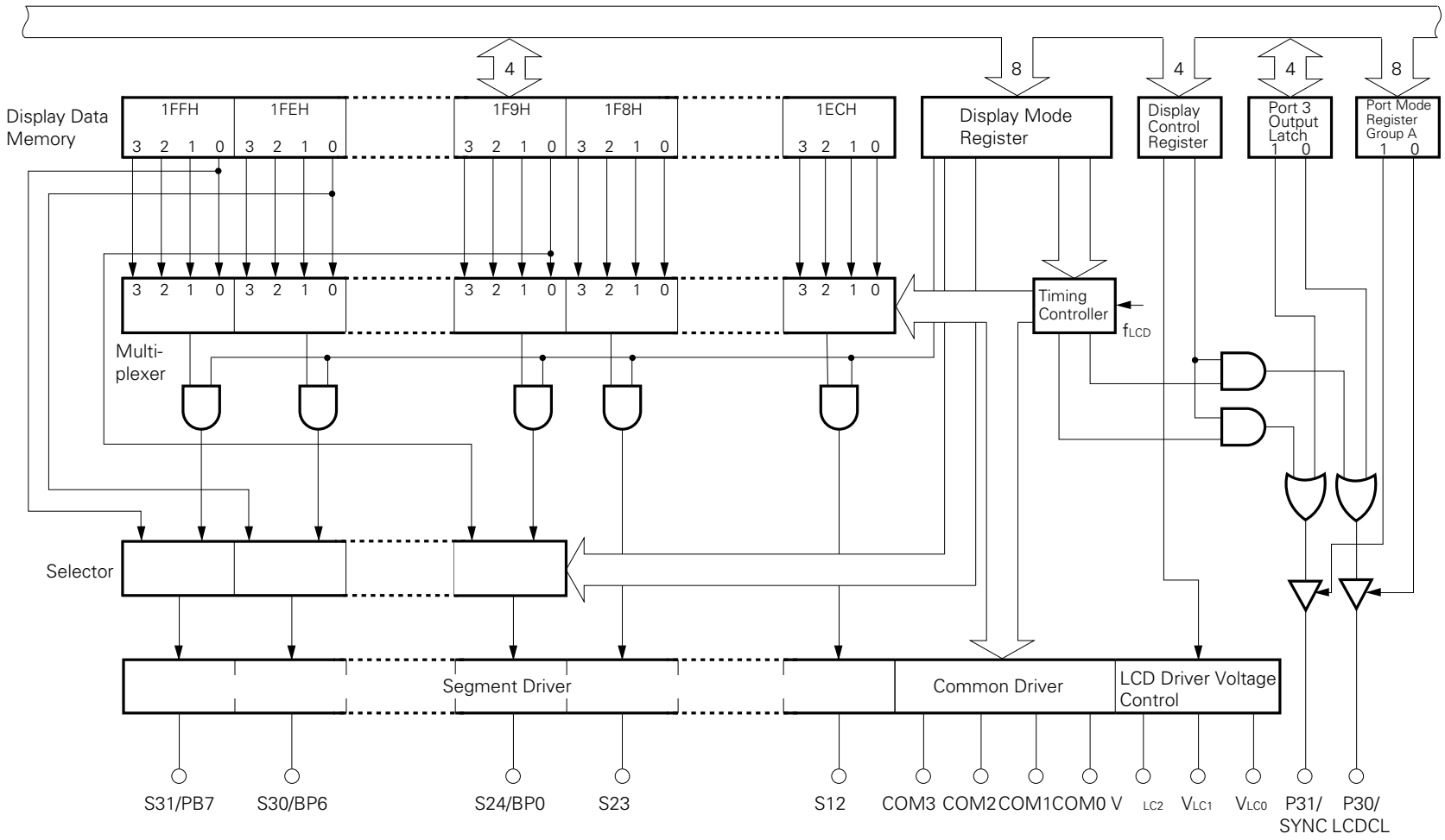
5.8 LCD CONTROLLER/DRIVER

The μPD75336 incorporates a display controller which generates a segment signal and a common signal in accordance with the display data memory and a segment drive and a common driver which can directly operate the LCD panel.

The LCD controller/driver has the following functions.

- Automatically read display data memory by DMA operation and generates segment and common signals.
- Can select one of the following 5 display modes.
  - ① Static
  - ② 1/2 duty (2-time multiplexing), 1/2 bias
  - ③ 1/3 duty (3-time multiplexing), 1/2 bias
  - ④ 1/3 duty (3-time multiplexing), 1/3 bias
  - ⑤ 1/4 duty (4-time multiplexing), 1/3 bias
- Can select one of the four frame frequencies in each display mode.
- Has a maximum of 20 segment signal outputs (S12 to S31) and a maximum of 4 common outputs (COM0 to COM3).
- The segment outputs (S24 to S27, S28 to S31) can be switched to output ports in 4 output units (BP0 to BP3, BP4 to BP7).
- Can incorporate a split resistor for LCD drive power supply (mask option).
  - Applicable to various types of bias methods and LCD drive voltage.
  - Cuts off current to the split resistor when display is off.
- The display data memory not used for display can be used as a normal data memory.
- Can operate with subsystem clock.

Fig. 5-7 LCD Controller/Driver Block Diagram

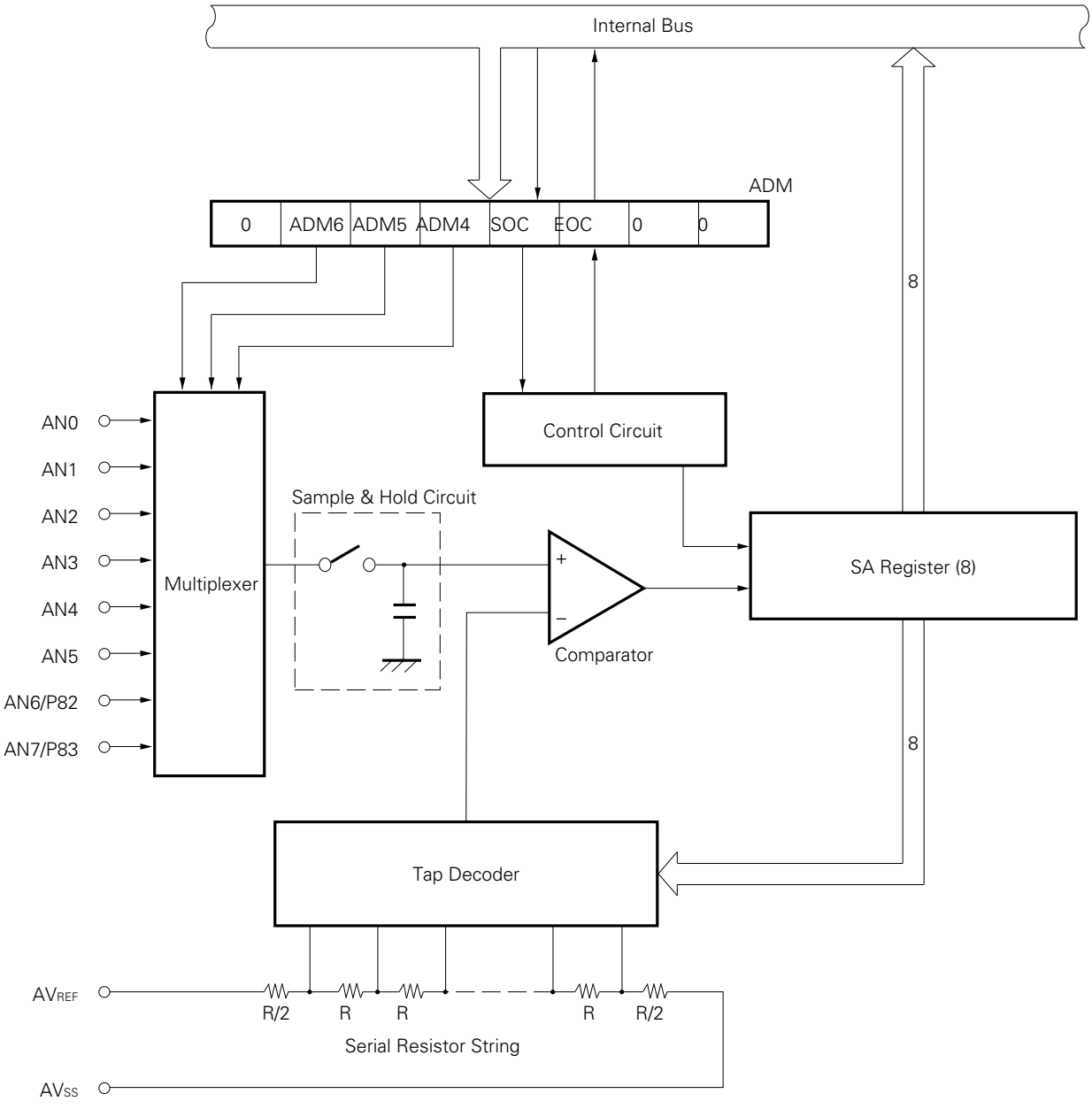


5.9 A/D CONVERTER

The μPD75336 incorporates an 8-bit resolution analog/digital (A/D) converter having 8-channel analog inputs (AN0 to AN7).

The A/D converter employs the successive approximation method.

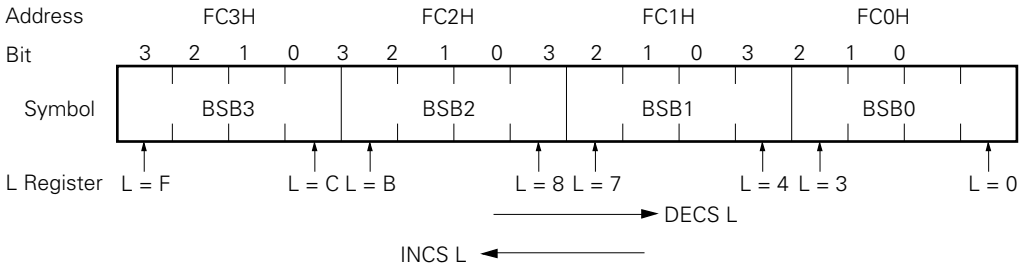
Fig. 5-8 A/D Converter Block Diagram



5.10 BIT SEQUENTIAL BUFFER.....16 BIT

The bit sequential buffer 0 to 3 (BSB0 to BSB3) is a special data memory for bit manipulation. Since it can carry out bit manipulation easily by sequentially changing the address and bit specification, the bit sequential buffer is useful to process data having a long bit length bit-wise.

Fig. 5-9 Bit Sequential Buffer Format



Remarks 1. In pmem.@L addressing, the specified bit shifts in accordance with the L register.

2. In pmem.@L addressing, BSB is always operable regardless of MBE, MBS specifications.

6. INTERRUPT FUNCTIONS

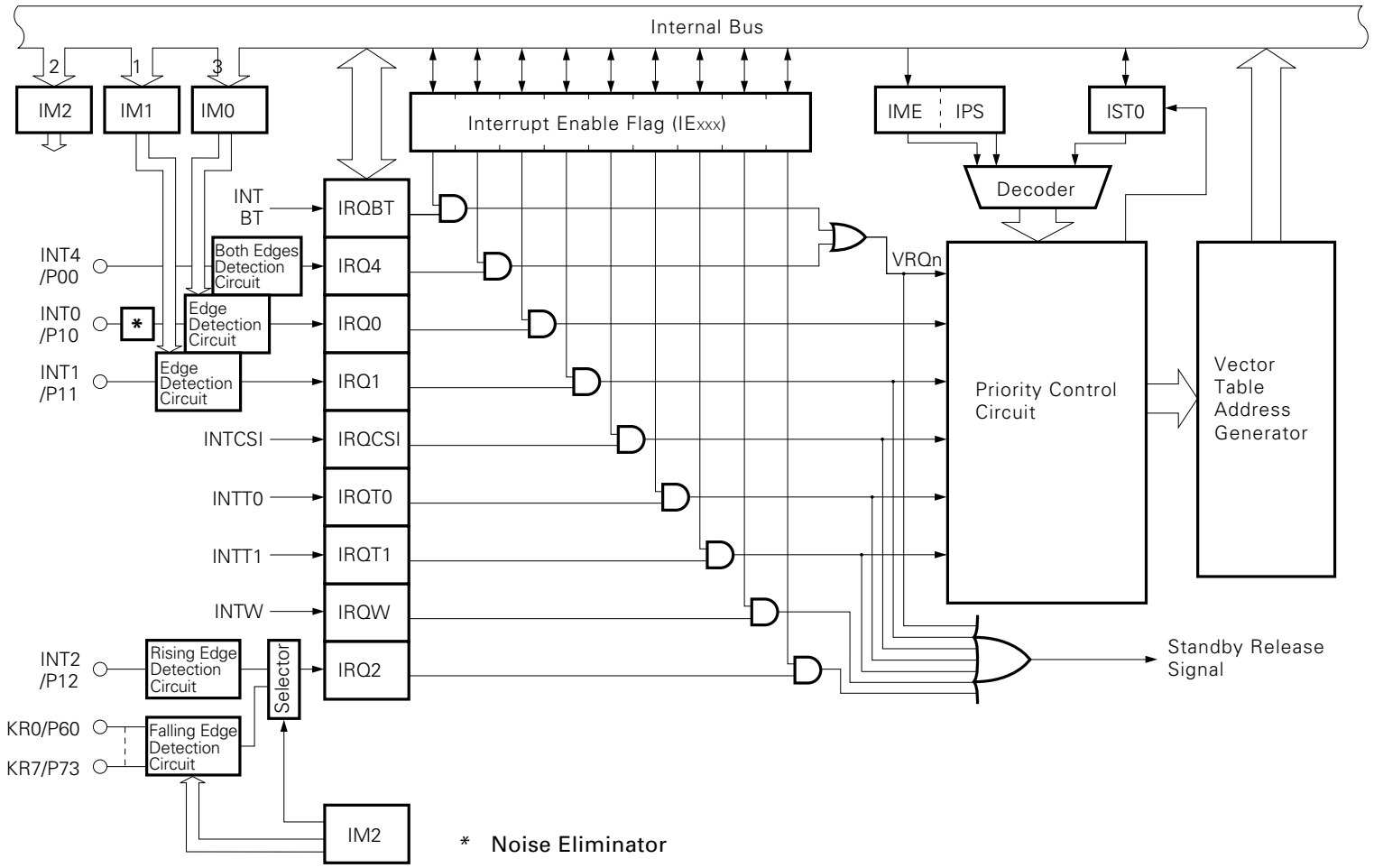
The μPD75336 has seven types of interrupt sources enabling multiplex interruption by the software control.

It has also two types of test source. INT2 of the test source is equipped with two types of edge detection testable inputs.

The μPD75336 interrupt control circuit has the following functions:

- Vectored interrupt function controlled by the hardware which can control enabling/disabling of interrupt acknowledge using interrupt flag (IE×××) and interrupt master enable flag (IME)
- Function of setting any interrupt start address
- Multiplex interruption function capable of specifying priority using the interrupt priority select register (IPS)
- Interrupt request flag (IRQ×××) test function (generation of interrupt can be checked by the software)
- Standby mode release function (interrupt to be released can be selected using the interrupt enable flag)

Fig. 6-1 Block Diagram Interrupt Control Circuit



7. STANDBY FUNCTIONS

Two standby modes (STOP mode and HALT mode) are available for the μPD75336 to reduce power consumption during standby for program.

Table 7-1 Operating Status in Standby Mode

Item \ Mode		STOP Mode	HALT Mode
Setting instruction		STOP instruction	HALT instruction
System clock at setting		Only main system clock settable	Main system clock or subsystem clock settable
Operation Status	Clock generator	Only main system clock oscillation stopped	Only CPU clock Φ stopped (oscillation continued)
	Basic interval timer	Operation stop	Operable only with main system clock oscillation (IRQBT set at reference time intervals)
	Serial interface	Operable only when external $\overline{SCK}$ input selected as serial clock	Operable with main system clock oscillation or when external $\overline{SCK}$ input is selected as serial clock.
	Timer/event counter	Operable only when TI0 and TI1 pin input specified as count clock	Operable with main system clock oscillation or T10 and TI1 pin input specified as count clock.
	Watch timer	Operable only when f_{XT} selected as count clock	Operable
	LCD controller	Operable only when f_{XT} selected as LCDCL	Operable
	A/D converter	Operation stop	Operable *
	External interrupt	INT1, 2, 4: Operable Only INT0 inoperable	
	CPU	Operation stop	
Release signal		Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input	Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input

* Operation possible only during main system clock oscillation

8. RESET FUNCTIONS

The μPD75336 is set by $\overline{\text{RESET}}$ input and each hardware is initialized as shown in Table 8-1. Reset operation timing is shown in Fig. 8-1.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

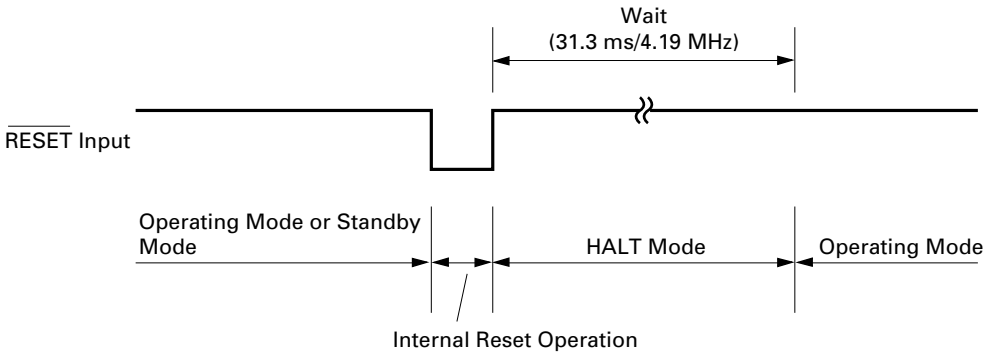


Table 8-1 Status after Reset of Each Hardware (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program counter (PC)		Low-order 6 bits of program memory address 0000H are set to PC13 to PC8 and the contents of address 0001H are set in PC7 to PC0.	Low-order 6 bits of program memory address 0000H are set to PC13 to PC8 and the contents of address 0001H are set in PC7 to PC0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0)	0	0
	Bank enable flag (MBE, RBE)	Bit 6 of program memory address 0000H is set in RBE, and bit 7 is set to MBE.	Bit 6 of program memory address 0000H is set in RBE, and bit 7 is set to MBE.
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held*	Undefined
General register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection register (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter (n = 0, 1)	Counter (Tn)	0	0
	Modulo register (TMODn)	FFH	FFH
	Mode register (TMn)	0	0
	TOEn, TOUT F/F	0, 0	0, 0
Watch timer	Mode register (WM)	0	0
Serial interface	Shift register (SIO)	Held	Undefined
	Operating mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
LCD controller	Display mode register (LCDM)	0	0
	Display control register (LCDC)	0	0
A/D converter	Mode register (ADM), EOC	04H (EOC = 1)	04H (EOC = 1)
	SA register	7FH	7FH

* Data of data memory addresses 0F8H to 0FDH becomes undefined by $\overline{\text{RESET}}$ input.

Table 8-1 Status after Reset of Each Hardware (2/2)

Hardware			$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Interrupt function	Interrupt request flag (IRQ×××)	IRQ1, IRQ2, IRQ4	Undefined	Undefined
		Other than above	0	0
	Interrupt enable flag (IE×××)		0	0
	Priority select register (IPS)		0	0
	INT0, 1, 2 mode registers (IM0, IM1, IM2)		0, 0, 0	0, 0, 0
Digital port	Output buffer		OFF	OFF
	Output latch		Clear (0)	Clear (0)
	I/O mode register (PMGA, PMGB, PMGC)		0	0
	Pull-up resistor specification register (POGA, POGB)		0	0
Pin status	P00 to P03, P10 to P13, P20 to P23, P30 to P33, P60 to P63, P70 to P73, P80 to P83		Input	Input
	P40 to P43, P50 to P53		• High level: With an on-chip pull-up resistor • High impedance: In open-drain	• High level: With an on-chip pull-up resistor • High impedance: In open-drain
	S12 to S31, COM0 to COM3		*	*
	BIAS		• Low level: With an on-chip split resistor • High impedance: Without an on-chip split resistor	• Low level: With an on-chip split resistor • High impedance: Without an on-chip split resistor
Bit sequential buffer (BSB0 to BSB3)			Held	Undefined

★

* Each display output selects the following V_{LCX} as input source.

S12 to S31: V_{LC1}

COM0 to COM2: V_{LC2}

COM3: V_{LC0}

However, the level of each display output varies depending on each display output and V_{LCX} external circuit.

9. INSTRUCTION SET

(1) Operand representation and description methods

In the operand column of each instruction, operands are entered in accordance with the description method for the operand representation of the instruction (refer to **RA75X Assembler Package User's Manual Language Volume (EEU-730)** for details). If there is more than one description method, select one method. Alphabetic capital letters, plus and minus signs are keywords. Describe them what they are.

In the case of immediate data, describe appropriate numeric values or labels.

Symbols of various registers and flags can be described as labels in place of mem, fmem, pmem, bit, etc. (Refer to **μPD75336 User's Manual (IEU-725)** for details.) However, labels which can be written for fmem and pmem are limited.

Identifier	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label * 2-bit immediate data or label
fmem pmem	FB0H to FBFH, FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label
addr caddr faddr	0000H to 3F7FH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H to 7FH immediate data (however, bit0 = 0) or label
PORTn IE××× RBn MBn	PORT 0 to PORT 8 IEBT, IET0, IET1, IE0 to IE2, IE4, IECSI, IEW RB0 to RB3 MB0, MB1, MB2, MB15

* Only even address can be entered for mem in 8-bit data processing.

(2) Operation description legend

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA′	:	Expanded register pair (XA′)
BC′	:	Expanded register pair (BC′)
DE′	:	Expanded register pair (DE′)
HL′	:	Expanded register pair (HL′)
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Portn (n = 0 to 8)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority select register
IE×××	:	Interrupt enable flag
RBS	:	Register bank select register
MBS	:	Memory bank select register
PCC	:	Processor clock control register
•	:	Address, bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Description of symbols in the addressing area column

*1	MB = MBE • MBS (MBS = 0, 1, 2, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS (MBS = 0, 1, 2, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3F7FH	Program memory addressing
*7	addr = (Current PC) –15 to (Current PC) –1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H to 0FFFH ($PC_{13, 12}$ = 00B) or 1000H to 1FFFH ($PC_{13, 12}$ = 01B) or 2000H to 2FFFH ($PC_{13, 12}$ = 10B) or 3000H to 3F7FH ($PC_{13, 12}$ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	

Remarks 1. MB indicates an accessible memory bank.
2. In *2, MB = 0 irrespective of MBE and MBS.
3. In *4 and *5, MB = 15 irrespective of MBE and MBS.
4. *6 to *10 indicate addressable areas.

(4) Description of machine cycle column

S indicates the number of machine cycles required for an instruction with skip function to carry out skip operation. The value of S varies as follows:

- When not skipped ..... S = 0
- When the skipped instruction is a 1-byte or 2-byte instruction ..... S = 1
- When the skipped instruction is a 3-byte instruction (BR !adder, CALL !adder instructions) ..... S = 2

Note GETI instruction is skipped in a 1 machine cycle.

The 1 machine cycle is equal to one cycle of CPU clock Φ (=t_{CY}) and four time periods are selectable by setting the PCC.

Note 1	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A ← n4		Stack A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		Stack A
		HL, #n8	2	2	HL ← n8		Stack B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ← (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ↔ (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Note 2	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		

Note **1.** Instruction Group
2. Table reference

Note 1	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← (H + mem_{3-0} .bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit, CY	2	2	(H + mem_{3-0} .bit) ← CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA – rp'		borrow
		rp'1, XA	2	2 + S	rp'1 ← rp'1 – XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
		XA, rp'	2	2	XA, CY ← XA – rp' – CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 – XA – CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
		XA, rp'	2	2	XA ← XA ⊻ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ⊻ XA		

Note Instruction Group

Note 1	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Note 2	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp'	2	2 + S	rp' ← rp' – 1		rp' = FFH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, reg	2	2 + S	Skip if XA = rp'		XA = rp'
Note 3	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Note **1.** Instruction Group
2. Accumulator operation
3. Carry flag operation

Note	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) ← 1	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) ← 0	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ⊻ (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ⊻ (H + mem$_{3-0}$.bit)	*1	
Branch	BR	addr	—	—	PC$_{13-0}$ ← addr (The assembler selects the optimum instruction from among the BR !addr, BRCB !caddr, and BR $addr instructions.)	*6	
		!addr	3	3	PC$_{13-0}$ ← addr	*6	
		$addr	1	2	PC$_{13-0}$ ← addr	*7	
		PCDE	2	3	PC$_{13-0}$ ← PC$_{13-8}$ + DE		
		PCXA	2	3	PC$_{13-0}$ ← PC$_{13-8}$ + XA		
	BRCB	!caddr	2	2	PC$_{13-0}$ ← PC$_{13,12}$ + caddr$_{11-0}$	*8	

Note Instruction Group

Note 1	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALL	!addr	3	2	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13}, PC_{12} PC_{13-0} ← addr, SP ← SP – 4	*6	
	CALLF	!faddr	2	2	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13}, PC_{12} PC_{13-0} ← 000 + faddr, SP ← SP – 4	*9	
	RET		1	3	PC_{11-0} ← (SP) (SP + 3) (SP + 2) MBE, RBE, PC_{13}, PC_{12} ← (SP + 1) SP ← SP + 4		
	RETS		1	3+S	PC_{11-0} ← (SP) (SP + 3) (SP + 2) MBE, RBE, PC_{13}, PC_{12} ← (SP + 1) SP ← SP + 4, then skip unconditionally		Unconditional
	RETI		1	3	PC_{11-0} ← (SP) (SP + 3) (SP + 2) MBE, RBE, PC_{13}, PC_{12} ← (SP + 1) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1) (SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1) (SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Note 2	EI		2	2	IME(IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME(IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		
Input/output	IN*	A, PORTn	2	2	A ← $PORT_n$ (n = 0–8)		
		XA, PORTn	2	2	XA ← $PORT_{n+1}$, $PORT_n$ (n = 4, 6)		
	OUT*	PORTn, A	2	2	$PORT_n$ ← A (n = 2–8)		
		PORTn, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA (n =4, 6)		
Note 3	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0 – 3)		
		MBn	2	2	MBS ← n (n = 0, 1, 2, 15)		
	GETI	taddr	1	3	• **TBR Instruction** PC_{13-0} ← (taddr) $_{5-0}$ + (taddr + 1)	*10	
					• **TCALL Instruction** (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13}, PC_{12} PC_{13-0} ← (taddr) $_{5-0}$ ← (taddr + 1) SP ← SP – 4		
					• **Other than TBR and TCALL Instruction** Execution of an instruction addressed at (taddr) and (taddr + 1)		Depends on the referred instruction

* At IN/OUT instruction execution, MBE = 0 or MBE = 1, MBS =15 must be set in advance.

Remarks TBR and TCALL instructons are assembler pseudo instructions for GETI instruction table definition.

Note **1.** Instruction Group **2.** Interrupt control **3.** CPU control

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Power supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Except ports 4 and 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4 and 5	On-chip pull-up resistor	–0.3 to V_{DD} +0.3	V
			Open–drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	One pin		–15	mA
		All pins		–30	mA
Output current low	I_{OL}*	One pin	Peak value	30	mA
			rms	15	mA
		Total of ports 0, 2, 3, 5 and 8	Peak value	100	mA
			rms	60	mA
		Total of ports 4, 6, and 7	Peak value	100	mA
			rms	60	mA
Storage temperature	T_{stg}			–65 to +150	°C

* Rms is calculated using the following expression: [rms] = [peak value] × $\sqrt{\text{duty}}$

★ **Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

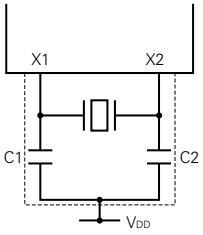
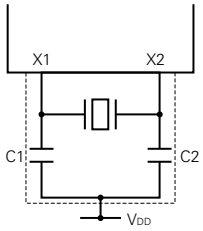
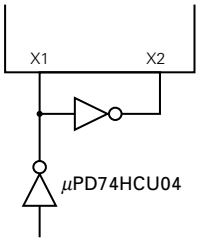
★ **GUARANTEED OPRERATING RANGE**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply voltage	V_{DD}		2.7		6.0	V
Operating temperature	T_{opt}		–40		+85	°C

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_X)***1**		1.0		5.0***3**	MHz
		Oscillation stabilization time***2**	After V_{DD} reaches the MIN. value of the oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_X)***1**		1.0	4.19	5.0***3**	MHz
		Oscillation stabilization time***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)***1**		1.0		5.0***3**	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		100		500	ns

***** **1.** The oscillator frequency and X1 input frequency indicate only the oscillator characteristics. For the instruction execution time refer to the AC CHARACTERISTICS.

2. The oscillation stabilization time is necessary for oscillation to stabilize after V_{DD} reaches the MIN. value of the oscillation voltage range or releasing the STOP mode.

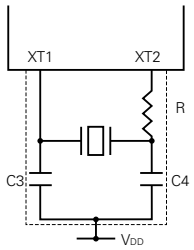
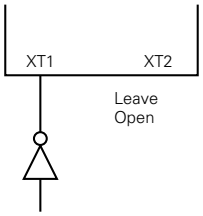
3. When the oscillator frequency is "4.19 MHz < f_X ≤ 5.0 MHz" PCC = 0011 should for the instruction execution time. If PCC = 0011 is selection, 1 machine cycle is less than 0.95 μs with the result that the specified MIN. value, 0.95 μs cannot be observed.

Note When using the main system clock oscillator or the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance. ★

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines or not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should always be the same as V_{SS}. Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

The subsystem clock oscillator is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Therefore, when using the subsystem clock, special care is required in wiring methods.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT}) *1*		32	32.768	35	kHz
		Oscillation stabilization time *2*	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) *1*		32		100	kHz
		XT1 input high-/ low-level width (t_{XTH},t_{XTL})		5		15	μs

* **1.** The oscillator frequency and X1 input frequency indicate only the oscillator characteristics. For the instruction execution time refer to the AC CHARACTERISTICS.

2. The oscillation stabilization time is necessary for oscillation to stabilize after V_{DD} reaches the MIN. value of the oscillation voltage range or releasing the STOP mode.

★ **Note When using the main system clock oscillator or the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines or not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should always be the same as V_{SS}. Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

The subsystem clock oscillator is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Therefore, when using the subsystem clock, special care is required in wiring methods.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2, 3 and 8		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	On-chip pull-up resistor	0.7 V_{DD}		V_{DD}	V
			Open–drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4, 5 and 8		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage high	V_{OH1}	Ports 0, 2, 3, 6, 7, 8 BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = –1 mA	V_{DD} –1.0			V
			I_{OH} = –100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (with 2 I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = –100 μA	V_{DD} –2.0			V
			I_{OH} = –50 μA	V_{DD} –1.0			V
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6, 7 and 8	Ports 3, 4 and 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.4	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, SB1	Open–drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5 (open–drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (open–drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (2/2)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
On-chip pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6, 7 and 8 (Except P00) V_{IN} = 0 V	V_{DD} = 5.0 V ±10%		15	40	80	kΩ
			V_{DD} = 3.0 V ±10%		30		300	kΩ
	R_{L2}	Ports 4 and 5 V_{OUT} = V_{DD} –2.0 V	V_{DD} = 5.0 V ±10%		15	40	70	kΩ
			V_{DD} = 3.0 V ±10%		10		60	kΩ
LCD drive voltage	V_{LCD}				2.5		V_{DD}	V
LCD split resistor	R_{LCD}				60	100	140	kΩ
LCD output voltage deviation***1** (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3 2.7 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2	V
LCD output voltage deviation***1** (segment)	V_{ODS}	I_O = ±1 μA			0		±0.2	V
Supply current***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ±10%***4**			2.5	8	mA
			V_{DD} = 3 V ±10%***5**			0.35	1.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10%		500	1500	μA
				V_{DD} = 3 V ±10%		150	450	μA
	I_{DD3}	32 kHz***6** crystal oscillation	Operating mode	V_{DD} = 3 V ±10%		30	90	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10%			0.5	20	μA
			V_{DD} = 3 V ±10%			0.1	10	μA
				T_a = 25 °C		0.1	5	μA

* **1.** The voltage deviation is the difference between the output voltage and the segment or common output desired value (V_{LCDn}; n = 0, 1, 2)

2. Current which flows in the on-chip pull-up resistor or LCD split resistor is not included.

3. Including oscillation of the subsystem clock.

4. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

5. When PCC is set to 0000 and the device is operated in the low-speed mode.

6. When the system clock control register (SCC) is set to 1011 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

A/D CONVERTER CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Resolution				8	8	8	bit
Absolute accuracy ***1**		2.5 V ≤ AV_{REF} ≤ V_{DD}	–10 ≤ Ta ≤ +85 °C			±1.5	LSB
			–40 ≤ Ta < –10 °C			±2.0	
Conversion time	t_{CONV}	***2**				168/f_X	s
Sampling time	t_{SAMP}	***3**				44/f_X	s
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF}	V
Analog Input impedance	R_{AN}				1000		MΩ
AV_{REF} current	I_{REF}				1.0	2.0	mA

* **1.** Absolute accuracy excluding quantization (±1/2 LSB) error.

2. Time up to end of conversion (EOC = 1) after execution of the conversion start instruction. (40.1 μs: f_X = 4.19 MHz operation)

3. Time up to end of sampling after execution of the conversion start instruction. (10.5 μs: f_X = 4.19 MHz operation)

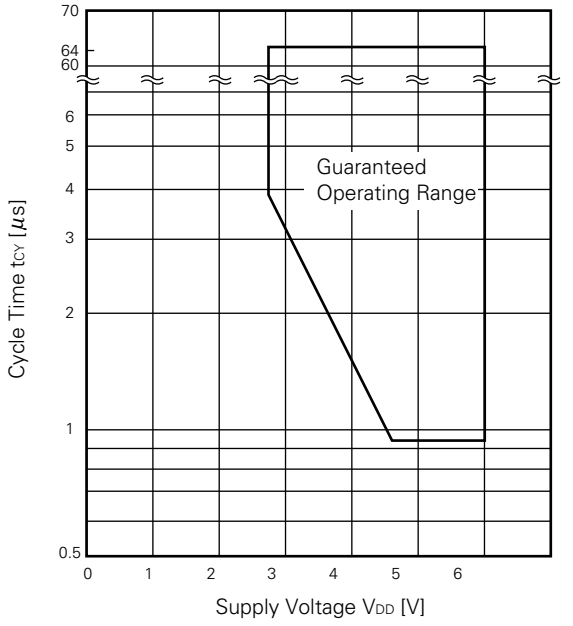
AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)***1**	t_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0, TI1 input width high/low	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input width high/low	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, INT2, INT4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ width low	t_{RSL}			10			μs

* **1.** CPU clock (Φ) cycle time is determined by the oscillator frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic with the main system clock operating.

2. $2t_{CY}$ or $128/f_X$ is set by setting the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Operating on Main System Clock)



SERIAL TRANSFER OPERATION

2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ width high/low	t_{KL1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KH1}			t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ width high/low	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (to SCK↑)	t_{SIK2}			100			ns
SI hold time (from SCK ↑)	t_{KSI2}			400			ns
SO output delay time from SCK↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are load resistor and load capacitance of the SO output line.

SBI Mode ($\overline{SCK}$ ... Internal clock output (Master))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ width high/low	t_{KL3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
	t_{KH3}			t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 width low	t_{SBL}			t_{KCY3}			ns
SB0, 1 width high	t_{SBH}			t_{KCY3}			ns

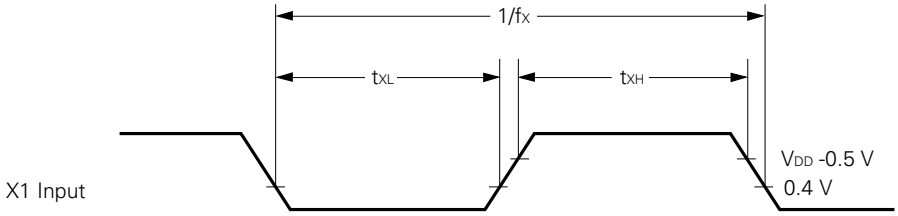
SBI Mode ($\overline{SCK}$ ... External clock input (Slave))

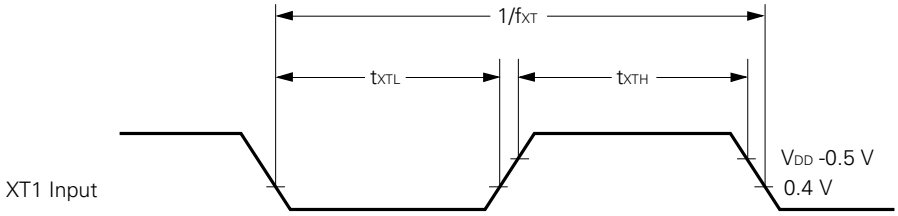
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ width high/low	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 width low	t_{SBL}			t_{KCY4}			ns
SB0, 1 width high	t_{SBH}			t_{KCY4}			ns

***** R_L and C_L are load resistor and load capacitance of the SB0, 1 output lines.

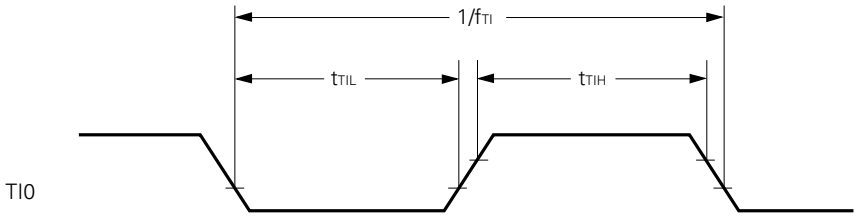
AC Timing Test Point (Excluding X1 and XT1 inputs)

Clock Timings



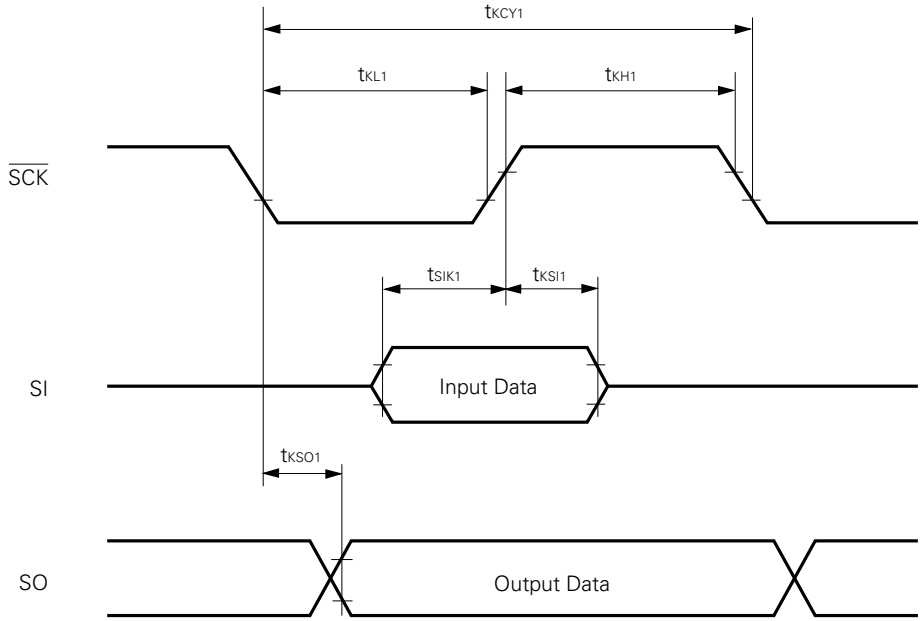


TI0 Timing

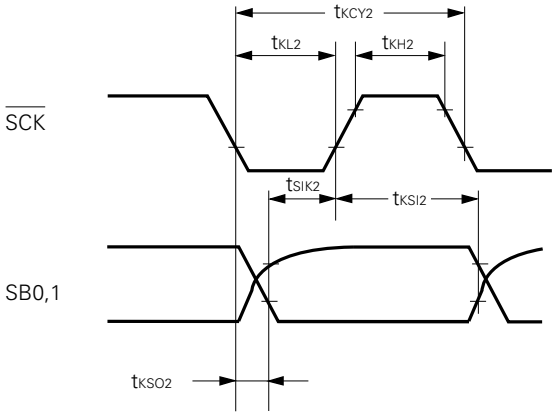


Serial Transfer Timing

3-wired serial I/O mode:

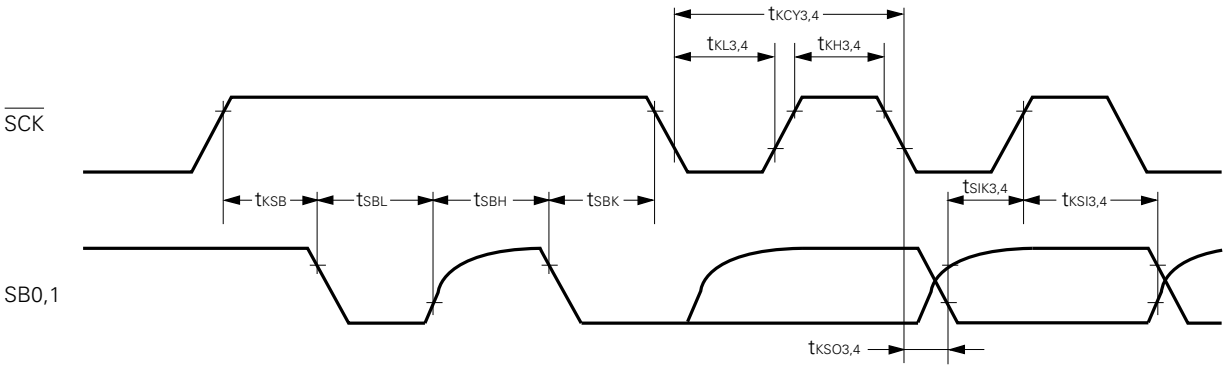


2-wired serial I/O mode:

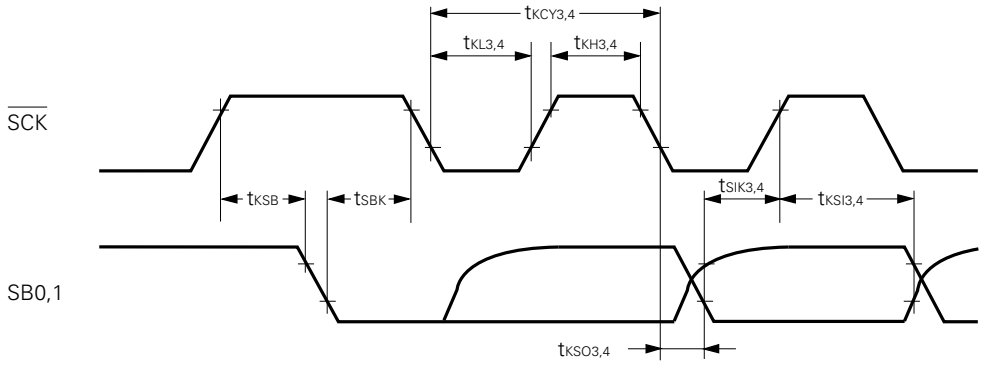


Serial Transfer Timing

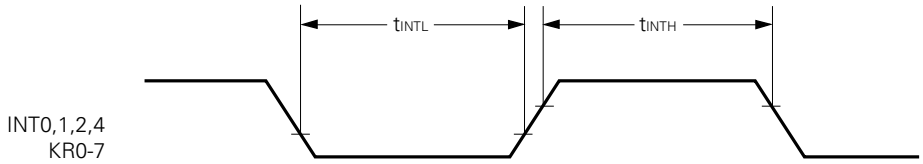
Bus release signal transfer:



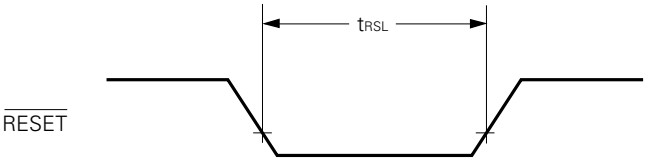
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current***1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time***2**	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		***3**		ms

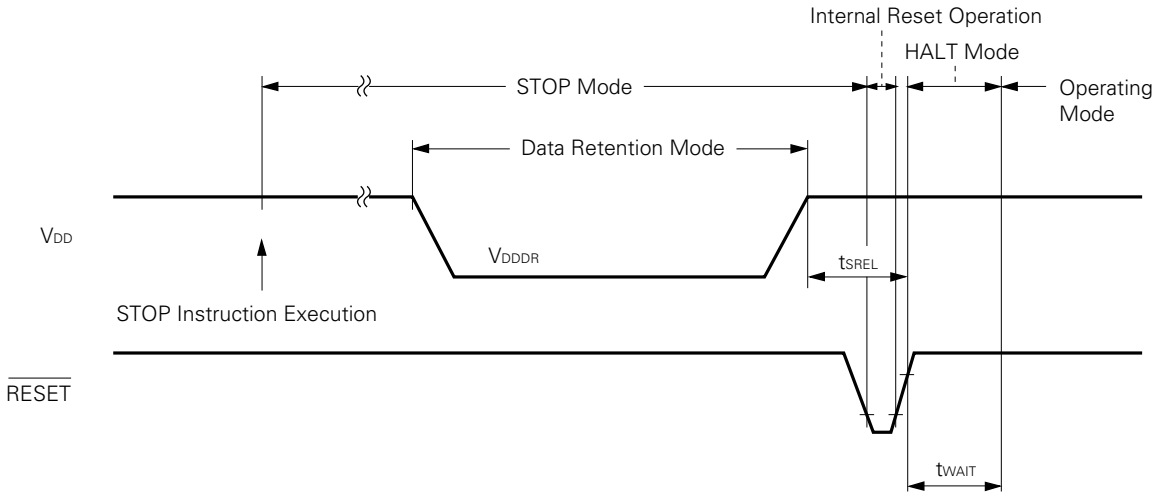
* **1.** Current which flows in the on-chip pull-up resistor is not included.

2. The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

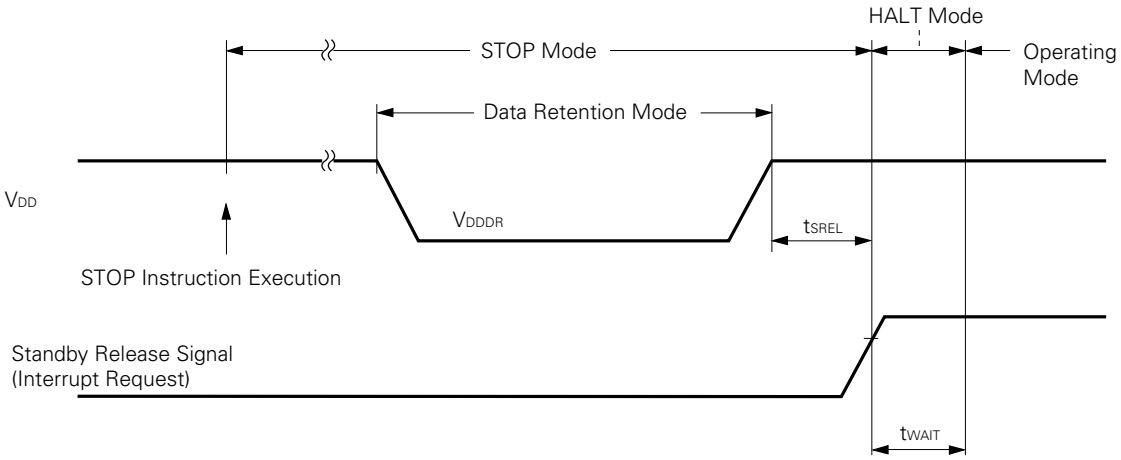
3. Depends on the basic interval timer mode register (BTM) setting (table below).

BTM3	BTM2	BTM1	BTM0	WAIT TIME (Figures in parentheses are for operation at fx = 4.19 MHz)
—	0	0	0	2^{20}/fx (approx. 250 ms)
—	0	1	1	2^{17}/fx (approx. 31.3 ms)
—	1	0	1	2^{15}/fx (approx. 7.82 ms)
—	1	1	1	2^{13}/fx (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

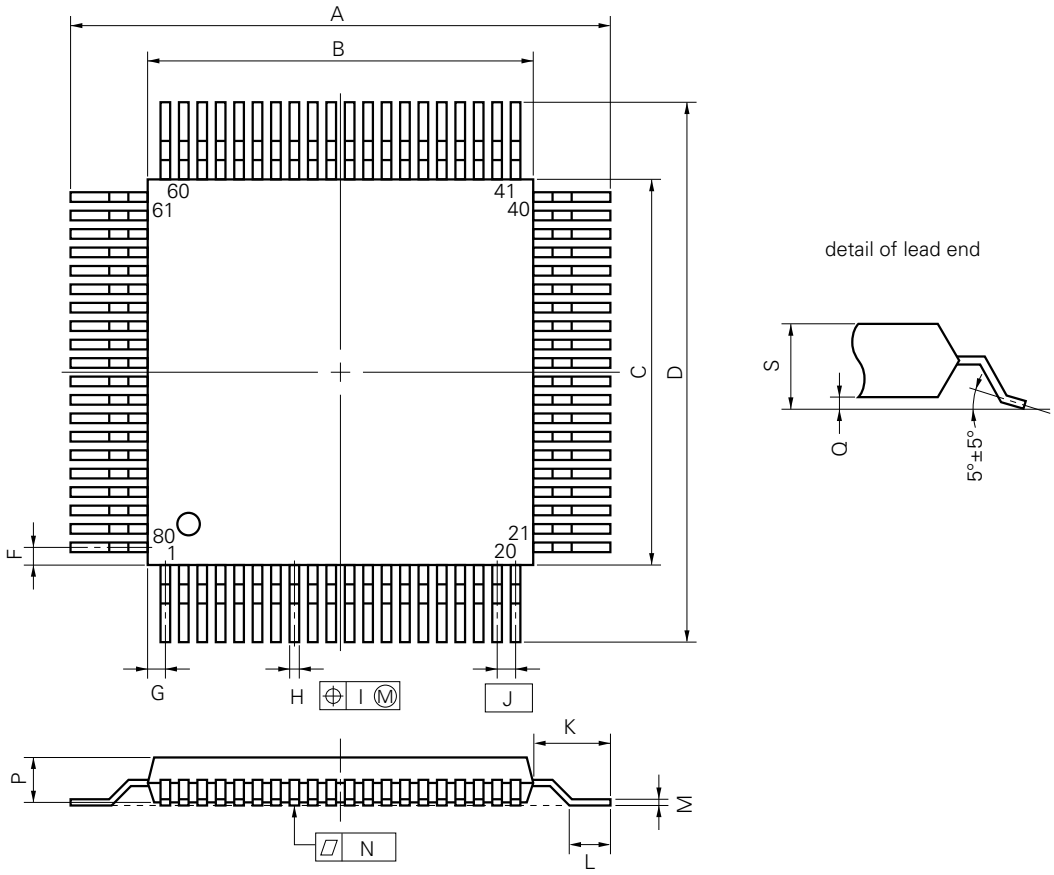


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



11. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14)



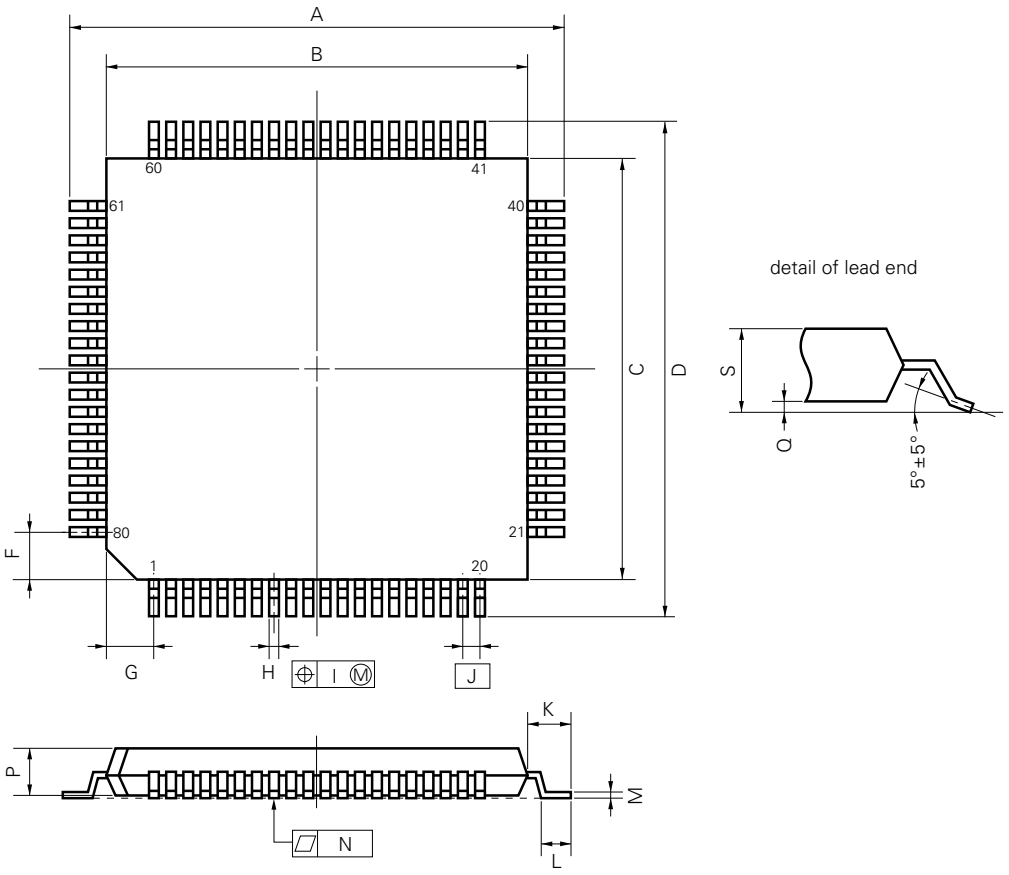
S80GC-65-3B9-3

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



P80GK-50-BE9-3

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.4	0.551±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.4	0.551±0.016
F	1.25	0.049
G	1.25	0.049
H	0.20±0.10	0.008±0.004
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.001}$
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
S	1.27 MAX.	0.05 MAX.

★ 12. RECOMMENDED SOLDERING CONDITIONS

The μPD75336 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to information document **"Surface Mount Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 12-1 Surface Mounting Type Soldering Conditions

(1) μPD75336GC-×××-3B9 : 80-pin plastic QFP (□14mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C above), Number of times: Once, Time limit: 7 days* (thereafter 10 hours prebaking required at 125°C)	IR30-107-1
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C above), Number of times: Once, Time limit: 7 days* (thereafter 10 hours prebaking required at 125°C)	VP15-107-1
Wave soldering	Solder bath temperature: 260°C max., Duration: 10 sec. max., Number of times: Once, Preliminary heat temperature: 120°C max. (Package surface temperature), Time limit: 7 days* (thereafter 10 hours prebaking required at 125°C)	WS60-107-1
Pin part heating	Pin part temperature: 300°C max., Duration: 3 sec. max. (per device side)	———

(2) μPD75336GK-×××-BE9 : 80-pin plastic TQFP (fine pitch)(□12mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C above), Number of times: Once, Time limit: 1 days* (thereafter 16 hours prebaking required at 125°C)	IR30-161-1
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C above), Number of times: Once, Time limit: 1 days* (thereafter 16 hours prebaking required at 125°C)	VP15-161-1
Pin part heating	Pin part temperature: 300°C max., Duration: 3 sec. max. (per device side)	———

* For the storage period after dry-pack decompression, storage conditions are max. 25°C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Notice

A version of this product with improved recommended soldering conditions is available.
For details (improvements such as infrared reflow peak temperature extension (235°C), number of times: twice, relaxation of time limit, etc.), contact NEC sales personnel.

APPENDIX A. DIFFERENCES BETWEEN μPD75336 AND μPD75328 FUNCTIONS

Product Name		μPD75336	μPD75328
CPU core		75X High End	75X Standard
ROM (Byte)		16256	8064
RAM (× 4 bits)		768	512
General register		4 bits × 8 × 4	4 bits × 8 × 1
Instruction cycle	Main system clock	0.95 μs, 1.91 μs, 3.81 μs, 15. 3 μs (at 4.19 MHz operation)	0.95 μs, 1.91 μs, 15.3 μs (at 4.19 MHz operation)
	Subsystem clock	122 μs (at 32.768 kHz operation)	
A/D converter		• 8-bit resolution × 8 channels (successive approximation) • A/D operating range: V_{DD} = 2.7 to 6.0 V	• 8-bit resolution × 6 channels (successive approximation) • A/D operating range: V_{DD} = 3.5 to 6.0 V
Timer/counter		• Basic interval timer × 1 • Timer/event counter × 2 • Watch timer × 1	• Basic interval timer × 1 • Timer/event counter × 1 • Watch timer × 1
Vectored interrupt		• External: 3 • Internal: 4	• External: 3 • Internal: 3
Buzzer output (BUZ)		2 kHz, 4 kHz, 32 kHz	2 kHz
8-bit data processing		Transfer, add/subtract, increase/decrease, compare	Transfer
Package		• 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (fine pitch)(□12 mm)	• 80-pin plastic QFP (□14 mm)
Product with on-chip PROM		μPD75P336	μPD75P328

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75336.

Hardware	IE-75000-R*1 IE-75001-R	75X series in-circuit emulator
	IE-75000-R-EM*2	IE-75000-R/IE-75001-R emulation board
	EP-75336GC-R EV-9200GC-80	μPD75336 emulation probe. 80-pin conversion socket EV-9200GC-80 added.
	EP-75336GK-R EV-9500GK-80	μPD75336 emulation probe. 80-pin conversion socket EV-9500GK-80 added.
	PG-1500	PROM programmer
	PA-75P328GC	μPD75P336GC PROM programmer adapter, connected to PG-1500
	PA-75P336GK	μPD75P336GK PROM programmer adapter, connected to PG-1500
Software	IE control program	Host Machine • PC-9800 series (MS-DOS™ Ver. 3.30 to 5.00A*3) • IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

* 1. Maintenance products
2. Not incorporated in the IE-75001-R.
★ 3. The task swap function, which is provided with Ver. 5.00/5.00A, is not available with this software.

Remarks For development tools manufactured by a third party, see the **"75X Series Selection Guide (IF-151)"**.

APPENDIX C. RELATED DOCUMENTS ★

Device Related Documents

Document Name	Document Number
User's Manual	
Instruction Application Table	
75X Series Selection Guide	

Development Tools Related Documents

	Document Name		Document Number
Hardware	IE-75000-R/IE-75001-R User's Manual		
	IE-75000-R-EM User's Manual		
	EP-75336GC-R User's Manual		
	EP-75336GK-R User's Manual		
	PG-1500 User's Manual		
Software	RA75X Assembler Package User's Manual	Operation Volume	
		Language Volume	
	PG-1500 Controller User's Manual		

Other Related Documents

Document Name	Document Number
Package Manual	
Surface Mount Technology Manual	
Quality Grade on NEC Semiconductor Devices	
NEC Semiconductor Device Reliability & Quality Control	
Electrostatic Discharge (ESD) Test	
Semiconductor Devices Quality Guarantee Guide	
Microcomputer Related Products Guide Other Manufactures Volume	

Note The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

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