1. PIN FUNCTIONS

1.1 Port Pins (1/2)

Pin name	I/O	Also used for	Function	8-bit I/O	At reset	Input/output circuit type (Note 1)
P00	I	INT4	4-bit input port (PORT0). Internal pull-up resistor can be specified for P01-P03 in 3-bit units by using software.	x	I	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓔ-A
P02	I/O	SO/SB0				Ⓔ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	I	INT0	With noise removal function	x	I	Ⓑ-C
P11		INT1	4-bit input port (PORT1) Internal pull-up resistor can be specified in 4-bit units by using software.			
P12		INT2				
P13		T10				
P20	I/O	PTO0	4-bit input/output port (PORT2). Internal pull-up resistor can be specified in 4-bit units by using software.	x	I	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30(Note 2)	I/O	LCDCL / MD0	Programmable 4-bit input/output port (PORT3). The input or output mode can be specified bitwise. Internal pull-up resistor can be specified in 4-bit units by using software.	x	I	E-B
P31(Note 2)		SYNC / MD1				
P32(Note 2)		MD2				
P33(Note 2)		MD3				
P40-P43(Note 2)	I/O	—	N-ch open drain 4-bit input/output port (PORT4). Data input/output pins (low-order four bits) during program memory (PROM) write and verify.	o	High impedance	M-A

1.1 Port Pins (2/2) Con'd

Pin name	I/O	Also used for	Function	8-bit I/O	At reset	Input/output circuit type (Note 1)
P50-P53 (Note 2)	I/O	—	N-ch open drain 4-bit input/output port (PORT5). Data input/output pins (low-order four bits) during program memory (PROM) write and verify.	o	High impedance	M-A
P60	I/O	KR0	Programmable 4-bit input/output port (PORT6). The input or output mode can be specified bitwise. Internal pull-up resistor can be specified in 4-bit units by using software.	o	I	Ⓔ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	4-bit input/output port (PORT7). Internal pull-up resistor can be specified in 4-bit units by using software.		I	Ⓔ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	I/O	—	4-bit input/output port (PORT8). Internal pull-up resistor can be specified in 4-bit units by using software.	x	I	E-B
P81						
P82						
P83						
BP0	O	S24	1-bit output port (BIT PORT). The pin is also used for a segment output pin.	x	Note 3	G-C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	O	S28				
BP5		S29				
BP6		S30				
BP7		S31				

Note 1: o Schmitt trigger input.

2: LED can be directly driven.

3: Each display output is selected by using the following V_{LCX} as input source:
S12-S31: V_{LC1}, COM0-COM2: V_{LC2}, COM3: V_{LC0}
However, the level of each display output varies depending on each display output and V_{LCX} external circuit.

1.2 Pins Other Than Port Pins (1/3)

Pin name	I/O	Also used for	Function	At reset	Input/output circuit type (Note 1)
T10	I	P13	External event pulse input pin to timer/event counter	—	Ⓑ-C
PTO0	O	P20	Timer/event counter output pin	I	E-B
PCL	I/O	P22	Clock output pin.	I	E-B
BUZ	I/O	P23	Fixed frequency output pin (for buzzer or system clock trimming).	I	E-B
$\overline{SCK}$	I/O	P01	Serial clock input/output pin.	I	Ⓕ-A
SO/SB0	I/O	P02	Serial data output pin. Serial bus input/output pin.	I	Ⓕ-B
SI/SB1	I/O	P03	Serial data input pin. Serial bus input/output pin.	I	Ⓜ-C
INT4	I	P00	Edge detection vectored interrupt input pin (rising or falling edge detection).	—	Ⓑ
INT0	I	P10	Edge detection vectored interrupt input pin (detected edge can be selected).	—	Ⓑ-C
INT1		P11			
INT2	I	P12	Edge detection testable input pin (rising edge detection).	—	Ⓑ-C
KR0-KR3	I/O	P60-P63	Testable input/output pins (parallel falling edge detection).	I	Ⓕ-A
KR4-KR7	I/O	P70-P73	Testable input/output pins (parallel falling edge detection).	I	Ⓕ-A
S12-S23	O	—	Segment signal output pins.	(Note 3)	G-A
S24-S31	O	BP0-7	Segment signal output pins.	(Note 3)	G-C
COM0-COM3	O	—	Common signal output pins.	(Note 3)	G-B

1.2 Pins Other Than Port Pins (2/3) Con'd

Pin name	I/O	Also used for	Function	At reset	Input/output circuit type (Note 1)
V_{LC0} -V_{LC2}	—	—	LCD driving power pins.	—	
BIAS	O	—	Output pin to cut external split resistor	High impedance	
LCDCL(Note 2)	I/O	P30	External extended driver driving clock output pin.	I	E-B
SYNC(Note 2)	I/O	P31	External extended driver synchronizing clock output pin.	I	E-B
AN0-AN5	I	—	Analog input pins to A/D converter.	—	Y
AV_{REF}	I	—	A/D converter reference voltage input pin.	—	Z
AV_{SS}	—	—	A/D converter GND potential pin.	—	
X1, X2	—	—	Main system clock oscillating crystal/ ceramic connection pins. When external clock is used, it is input to X1 and the opposite phase in input to X2.	—	
XT1, XT2	—	—	Subsystem clock oscillating crystal connection pins. When external clock is used, it is input to XT1 and XT2 is not connected. XT1 can be used as a 1-bit input (test) pin.	—	
$\overline{RESET}$	I	—	System reset input pin (active low).	—	Ⓑ
MD0-MD3	I/O	P30-P33	Mode selection pins during program memory (PROM) write and verify.	I	E-B
V_{PP}	—	—	Program voltage apply pin during program memory (PROM) write and verify. Connect it to V_{DD} during normal operation. +12.5 V is applied during PROM write and verify.	—	

1.2 Pins Other Than Port Pins (3/3) Con'd

Pin name	I/O	Also used for	Function	At reset	Input/output circuit type (Note 1)
V_{DD}	—	—	Positive power pin.	—	
V_{SS}	—	—	GND potential pin.	—	

Note 1: o Schmitt trigger input.

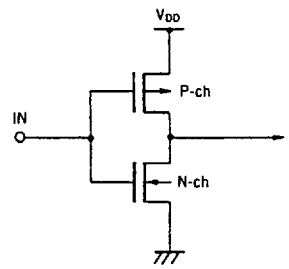
2: The pins are provided for future extension. They are used only as P30 and P31 pins at present.

3: Each display output is selected by using the following V_{LCX} as input source:
S12-S31: V_{LC1}, COM0-COM2: V_{LC2}, COM3: V_{LC0}
However, the level of each display output varies depending on each display output and V_{LCX} external circuit.

1.3 Pin Input/Output Circuits

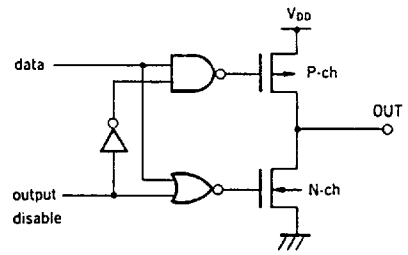
The uPD75P328 pin input/output circuits are shown schematically.

TYPE A (TYPE E-B)



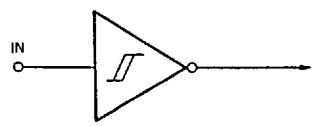
CMOS specification input buffer.

TYPE D (TYPE E-B, F-A)



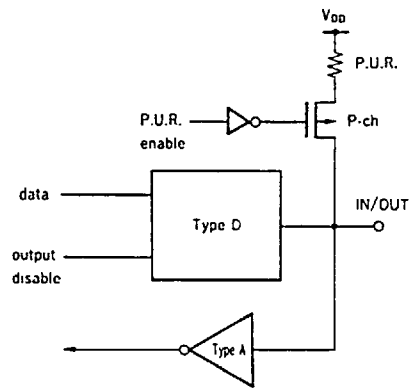
Push-pull output that can be placed in the impedance (both P-ch and N-ch off).

TYPE B



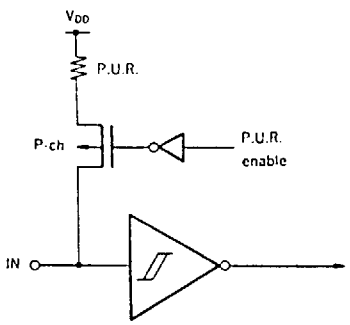
Schmitt trigger input having hysteresis characteristics.

TYPE E-B



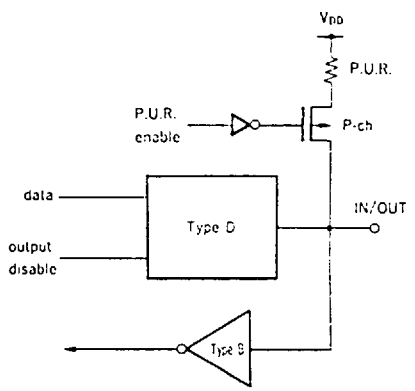
P.U.R. : Pull-Up Resistor

TYPE B-C



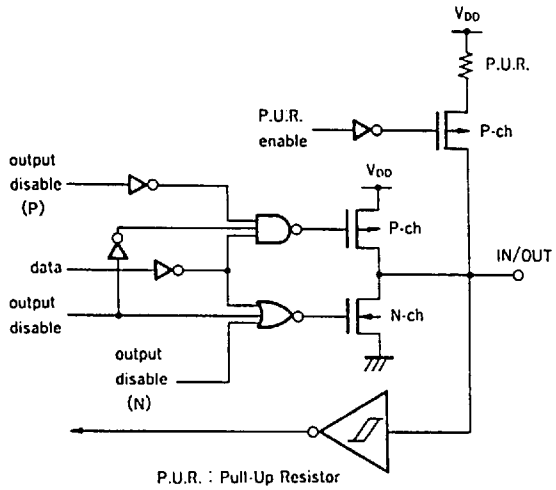
P.U.R. : Pull-Up Resistor

TYPE F-A



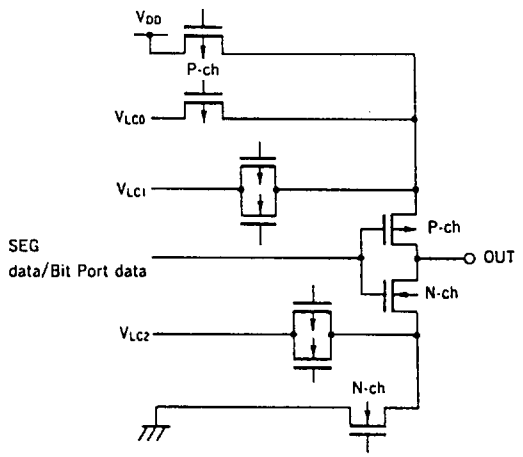
P.U.R. : Pull-Up Resistor

TYPE F-B

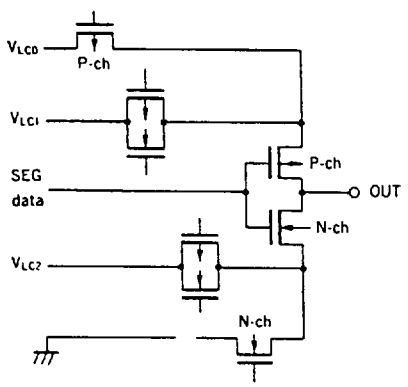


P.U.R. : Pull-Up Resistor

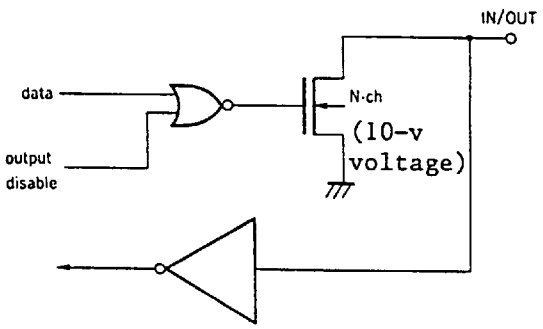
TYPE G-C



TYPE G-A

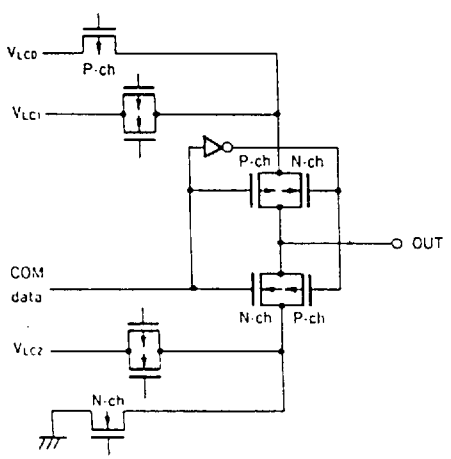


TYPE M-A

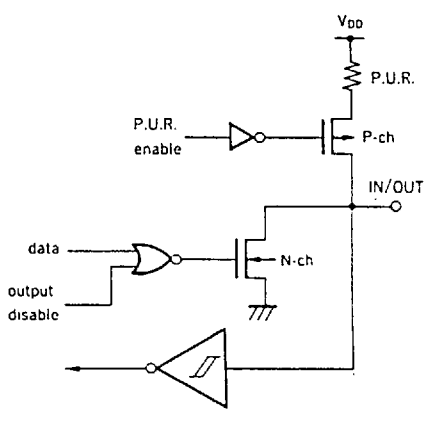


Medium voltage
input buffer
(+10-V voltage)

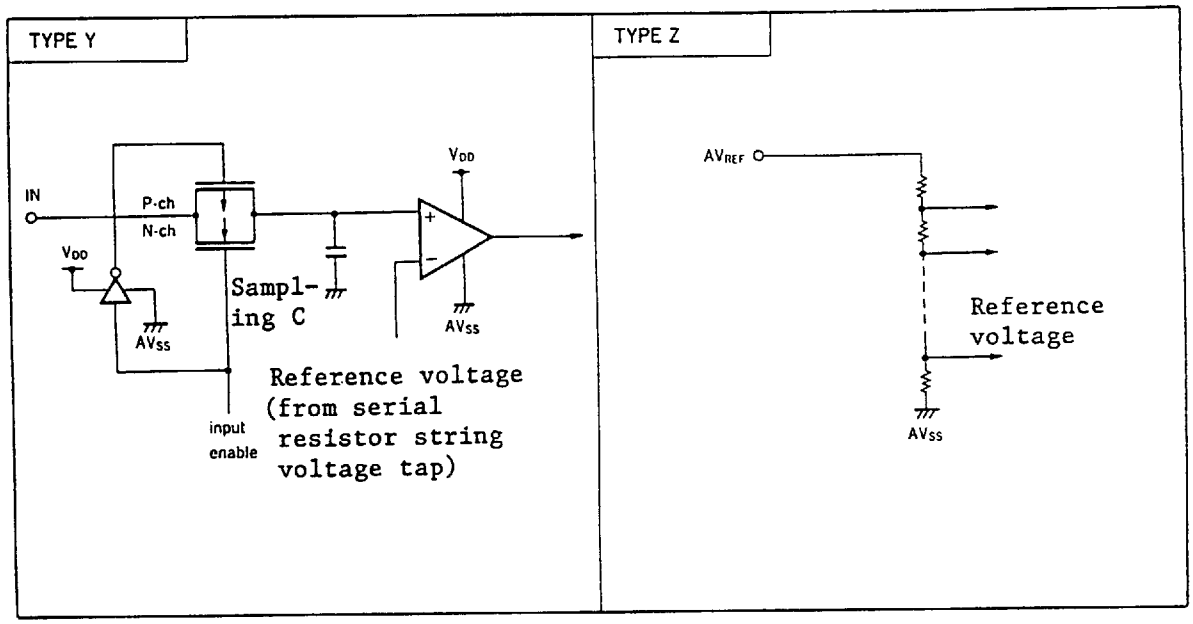
TYPE G-B



TYPE M-C



P.U.R. : Pull-Up Resistor



1.4 Cautions on Use of P00/INT4 and $\overline{\text{RESET}}$ Pins

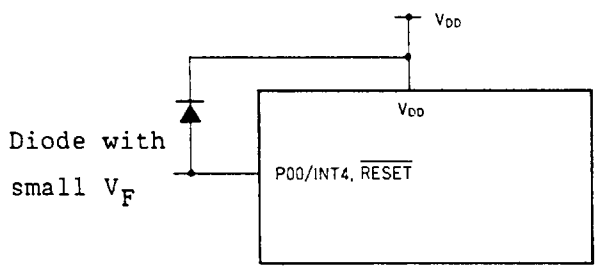
The P00/INT4 and $\overline{\text{RESET}}$ pins have a function to set the test mode for testing the internal operation of the uPD75P328 (used only for IC test) in addition to the functions described in 1.1 and 1.2.

When a voltage exceeding V_{DD} is applied to either of the pins, the test mode is set. Therefore, if noise exceeding V_{DD} is applied, even when the uPD75P328 operates normally, the test mode is entered and the normal operation is hindered.

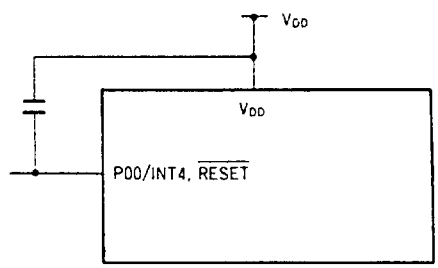
For example, if wiring for the P00/INT4 and $\overline{\text{RESET}}$ pins is long, interconnection noise may be applied to the pins, causing the problem to occur.

Wire so as to suppress interconnection noise as much as possible. If noise cannot be suppressed, use external parts for noise countermeasures, as shown below:

o Connect a diode with small V_F between the pin and V_{DD}



o Connect a capacitor between the pin and V_{DD}



2. DIFFERENCES BETWEEN uPD75P328 AND uPD75328

The uPD75P328 is a product which contains one-time PROM (only once programmable memory) in place of the program memory of the uPD75328 which contains mask ROM. Table 2.1 lists the differences between uPD75P328 and uPD75328. To use one-time ROM for debugging and preproduction of application systems and then use mask ROM for mass production, check these differences.

Refer to the uPD75328 User's Manual (Document No. IEM-5045) for detailed information on the CPU function and internal hardware.

Table 2-1 Differences Between uPD75P328 and uPD75328

Item		uPD75P328 (One-time PROM product)	uPD75328 (Mask ROM product)
Program memory		o One-time PROM o 8064 x 8 bits o 0000H - 1F7FH	o Mask ROM o 8064 x 8 bits o 0000H - 1F7FH
Port 4, 5 pull-up resistor		None	Mask option
Split resistor to supply LCD driving power		None	Mask option
Subsystem clock oscillating feed back resistor		On-chipped	Mask option
Pin connection	Pins 50-53	P30/LCDCL/MD0-P33/MD3	P30/LCDCL-P33
	Pin 69	V_{PP}	NC
Electrical characteristics		PROM and mask ROM products differ in consumption current, operating temperature range, etc. For details, refer to the Electrical Characteristics on their Data Sheets.	
Operation supply voltage range		5 V ± 5%	2.7 to 6.0 V
Operating temperature range		-10 to +70°C	-40 to +85°C
Package		80-pin plastic QFP (□ 14mm)	
Others		Since PROM and mask ROM products differ in circuit scale or mask layout, they differ in noise proof amount, noise radiation, etc.	

Caution: The PROM and mask ROM products differ in noise proof amount or noise radiation. To discuss replacement of PROM products with mask ROM products at a process from preproduction to mass production, make sufficient evaluation with CS (rather than ES) mask ROM products.

3. ONE-TIME PROM(PROGRAM MEMORY) WRITE AND VERIFY

Program memory contained in the uPD75P328 is one-time PROM (8064 x eight bits) which can be electrically written. The pins listed in the table given below are used for one-time PROM write and verify. Address is updated by clock input from the X1 pin instead of address input.

Pin name	Function
V_{PP}	Program voltage apply pin (normally, V_{DD} potential) during program memory write and verify.
X1, X2	Address update clock input during program memory write and verify. The opposite phase signal to the X1 pin is input to the X2 pin.
MD0-MD3	Operation mode selection pins during program memory write and verify.
P40-P43 (low-order four bits) P50-P53 (high-order four bits)	8-bit data input/output pins during program memory write and verify.
V_{DD}	Supply voltage apply pin. 5 V ± 5% is applied during normal operation; 6 V is applied during program memory write and verify.

Caution 1: Handle the pins not used during program memory write and verify as follows:

- o Other than the XT2 pin: Connect to V_{SS} via pull-down resistor.
- o XT2 pin: Do not connect the pin.

2: The uPD75P328 does not have an erasion window, thus the program memory contents cannot be erased with ultraviolet rays.

3.1 Operation Mode during Program Memory Write and Verify

The uPD75P328 is placed in the program memory write/verify mode by applying +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin. The operation mode is set according to how the MD0-MD3 pins are set as listed below:

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibition mode

x: L or H

3.2 Program Memory Write Procedure

The program memory write procedure is described below: (High speed write is enabled.)

(1) Pull down unused pins to V_{SS} via resistor. Make the X1 pin low.

(2) Supply 5 V to the V_{DD} and V_{PP} pins.

(3) Wait for 10 us.

(4) Select the program memory address clear mode.

(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.

(6) Select the program inhibition mode.

(7) Write data in the 1 ms write mode.

(8) Select the program inhibition mode.

(9) Select the verify mode. If data is written correctly, proceed to (10); if data is not written, repeat (7) to (9).

(10) Perform additional write of X (write count in (7) to (9)) x 1 ms.

(11) Select the program inhibition mode.

(12) Increment the program memory address by one by inputting four pulses to the X1 pin.

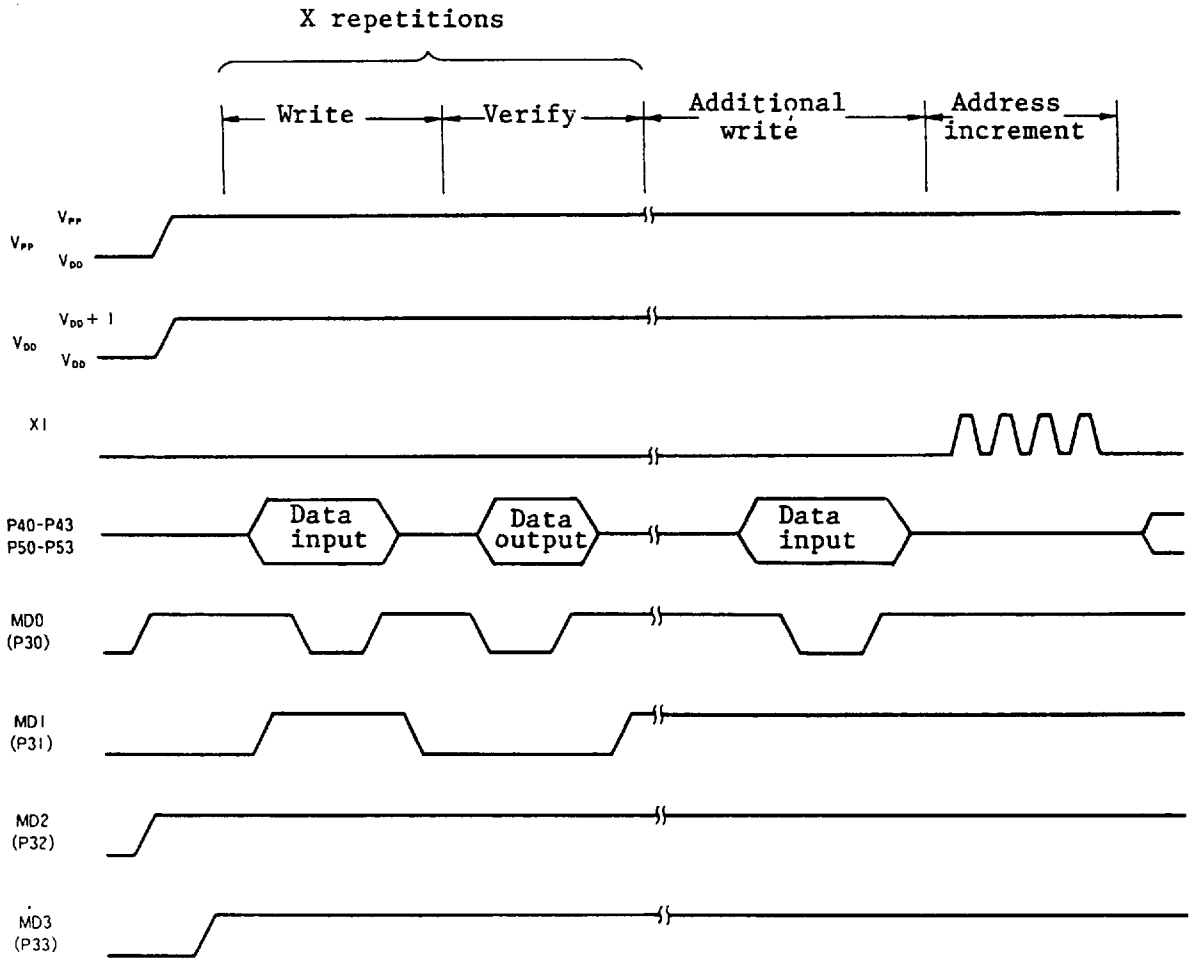
(13) Repeat (7) to (12) until the end address is reached.

(14) Select the program memory address clear mode.

(15) Change the V_{DD} and V_{PP} pin voltage to 5 V.

(16) Turn off the power.

Steps (2) to (12) are shown below:



3.3 Program Memory Read Procedure

The uPD75P328 program memory contents can be read according to the following procedure:

(1) Pull down unused pins to V_{SS} via resistor. Make the X1 pin low.

(2) Supply 5 V to the V_{DD} and V_{PP} pins.

(3) Wait for 10 us.

(4) Select the program memory address clear mode.

(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.

(6) Select the program inhibition mode.

(7) Select the verify mode. Whenever four clock pulses are input to the X1 pin, data is output in sequence one address at a time.

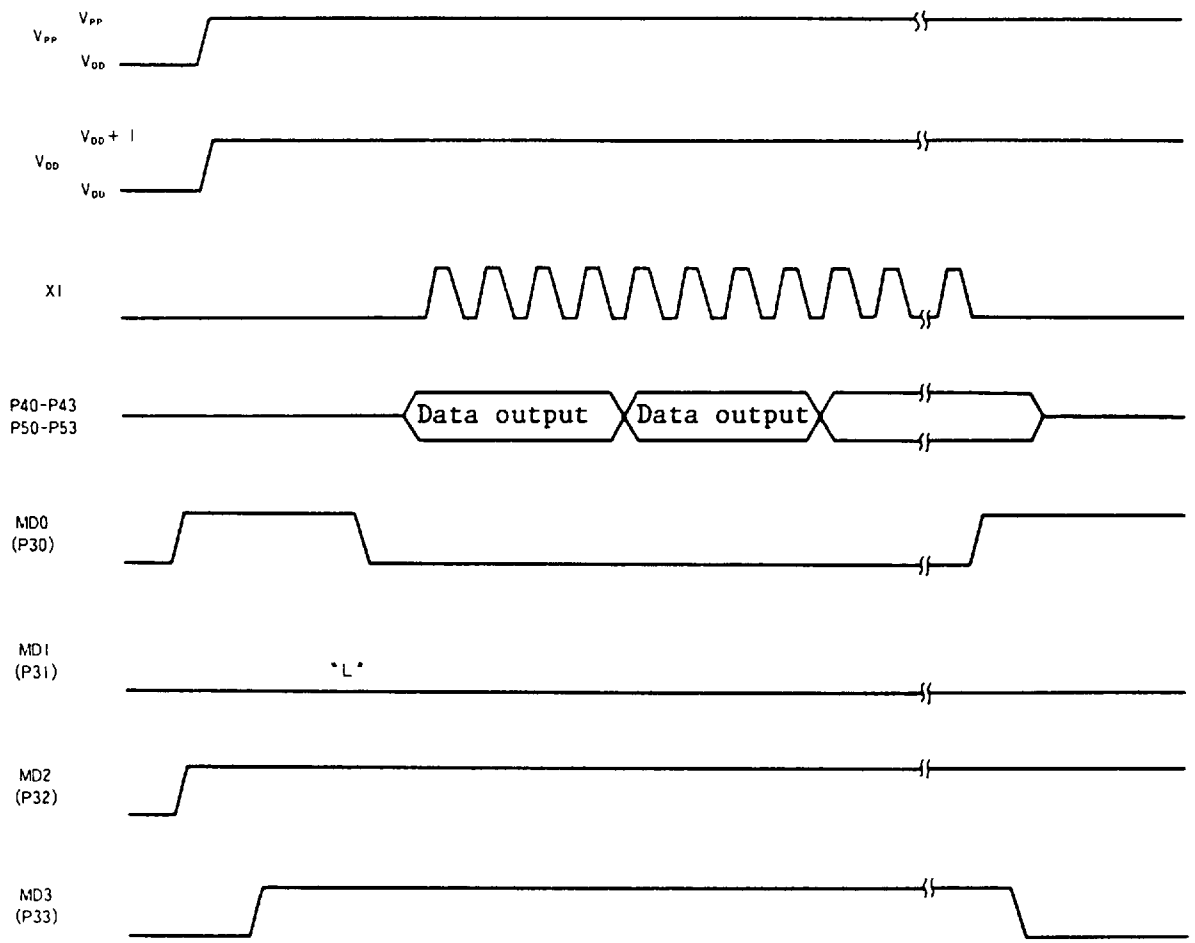
(8) Select the program inhibition mode.

(9) Select the program memory address clear mode.

(10) Change the V_{DD} and V_{PP} pin voltage to 5 V.

(11) Turn off the power.

Steps (2) to (9) are shown below:



4. ELECTRICAL CHARACTERISTIC

Absolute Maximum Rating (Ta = 25°C)

Parameter	Symbol	Test conditions			Ratings	Unit
Supply voltage	V_{DD}				-0.3 to +7.0	V
	V_{PP}				-0.3 to +13.5	V
Input voltage	V_{I1}	Other than ports 4 and 5			-0.3 to V_{DD}+0.3	V
	(Note 1) V_{I2}	Ports 4 and 5	Open drain		-0.3 to +11	V
Output voltage	V_O				-0.3 to V_{DD}+0.3	V
High level output current	I_{OH}	Single pin			-15	mA
		All pins			-30	mA
Low level output current	(Note 2) I_{OL}	Single pin		Peak value	30	mA
				rms	15	mA
		Total of ports 0, 2, 3, 5 and 8		Peak value	100	mA
				rms	60	mA
		Total of ports 4, 6, and 7		Peak value	100	mA
				rms	60	mA
Operating temperature	T_{opt}				-10 to +70	°C
Storage temperature	T_{stg}				-65 to +150	°C

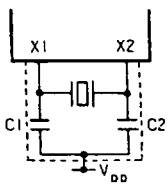
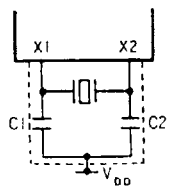
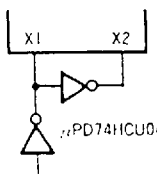
Note 1: When voltage exceeding 10 V is applied to port 4 or 5, power supply impedance (pull-up resistor) should be set to 50 kΩ or more.

Note 2: Root mean square (rms) = (peak value) x $\sqrt{\text{duty}}$

Capacitance (Ta = 25°C, V_{DD} = 0V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pin turned to be 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input/output capacitance	C_{IO}				15	pF

Characteristics of Main System Clock Oscillator (Ta = -10 to +70°C, V_{DD} = 5 V ± 5%)

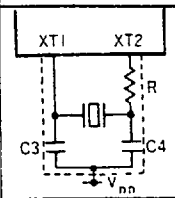
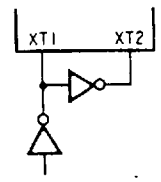
Resonator	Recommended contents	Parameter	Test condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator		(Note 1) Oscillation frequency (f_X)		1.0		(Note3) 5.0	MHz
		(Note 2) Oscillation stabilization time	After V_{DD} reaches the minimum value in the oscillator operating voltage range			4	ms
Crystal resonator		(Note 1) Oscillation frequency (f_X)		1.0	4.19	(Note3) 5.0	MHz
		(Note 2) Oscillation stabilization time				10	ms
External clock		(Note 1) X1 input frequency (f_X)		1.0		(Note3) 5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		500	ns

Note 1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator. Refer to the AC characteristics for instruction execution time.

2: Required time for oscillation to become stable after V_{DD} reaches MIN. of the oscillation voltage range or the STOP mode is released.

3: If the oscillation frequency is 4.19MHz < fx ≦ 5.0MHz, do not select PCC=0011 as the instruction execution time. If PCC=0011 is set, one machine cycle becomes less than 0.95us, and the specified MIN. value 0.95 cannot be followed.

Characteristics of Subsystem Clock Oscillator (Ta = -10 to +70°C, V_{DD} = 5 V ± 5%)

Resonator	Recommended contents	Parameter	Test condition	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time (Note)			1.0	2	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	us

Note: Required time for oscillation to become stable after V_{DD} reaches MIN. of the oscillation voltage range or the STOP mode is released.

Caution: To use the main system clock and subsystem clock oscillators, wire the portions surrounded by [----] to avoid wiring capacitance affection, etc., as follows:

- Make wiring as extremely short as possible.
- Do not cross the oscillator and any other signal line over each other. Do not put the oscillator near any line where high current fluctuates.
- Be sure to place oscillator capacitor ground point in the same potential as the V_{DD} pin.
  Do not connect to any ground pattern where high current flows.
- Do not take out any signal from the oscillator.

Particulary, the subsystem clock oscillator is low in amplification degree to consume low current and a noise error is liable to occur on the subsystem clock oscillator as compared with the main system clock oscillator. To use the subsystem clock osicllator, pay particular attention to the wiring method.

Recommended resonators

Main system clock: Ceramic resonator (Ta = -40°C to +85°C, V_{DD} = 5 V ± 5%)

Manufacturer	Product name	Frequency (MHz)	Recommended circuit constant	
			C1(pF)	C2(pF)
Murata	CSAX.XXMG093	2.00 to 2.44	30	30
	CSTX.XXMG093		Not required	Not required
	CSAX.XXMGU	2.45 to 5.00	30	30
	CSTX.XXMGU		Not required	Not required
	CSAX.XXMG	2.00 to 5.00	30	30
	CSTX.XXMG		Not required	Not required
Kyocera	KBR-2.0MS	2.00	47	47
	KBR-4.0MS	4.00	33	33
	KBR-5.0M	5.00	33	33

Main system clock: Crystal resonator (Ta = -20°C to +70°C, V_{DD} = 5 V ± 5%)

Manufacturer	Product name	Frequency (MHz)	Recommended circuit constant	
			C1(pF)	C2(pF)
Kinseki	HC-18U HC-43U, 49/U	2.0 to 5.0	22(Note)	22

Note: Adjust the oscillation frequency in the range of C1=15-33 pF.

Subsystem clock: Crystal resonator (Ta = -10°C to +60°C, V_{DD} = 5 V ± 5%)

Manu-facturer	Product name	Frequency (MHz)	Recommended circuit constant		
			C3(pF)	C4(pF)	R(kΩ)
Kinseki	P3	32.768	22(Note)	22	330

Note: Adjust the oscillation frequency in the range of C3=3 to 30 pF.

DC Characteristics (Ta = -10 to +70°C, V_{DD} = 5 V ± 5%)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	Ports 2, 3 and 8		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7 and $\overline{RESET}$ pin		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	Ports 4 and 5	Open drain	$0.7V_{DD}$		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}-0.5		V_{DD}	V
Low level input voltage	V_{IL1}	Ports 2, 3, 4, 5, and 8		0		$0.3V_{DD}$	V
	V_{IL2}	Ports 0, 1, 6, 7, and $\overline{RESET}$ pin		0		$0.2V_{DD}$	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High level output voltage	V_{OH1}	Ports 0, 2, 3, 6, 7 and 8 BIAS	I_{OH} = -1 mA	V_{DD}-1.0			V
	V_{OH2}	BP0-BP7	(Note1) I_{OH} = -100 uA	V_{DD}-2.0			V
Low level output voltage	V_{OL1}	Ports 0, 2, 3, 6, 7, and 8	Ports 3, 4 and 5 I_{OL} = 15 mA		0.4	2.0	V
			I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, 1 Open drain	Pull up R = 1 kΩ or more			$0.2V_{DD}$	V
	V_{OL3}	BP0-BP7	(Note1) I_{OL} = 100 uA			1.0	V
High level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	uA
	I_{LIH2}		X1, X2, XT1			20	uA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5			20	uA
Low level input leakage current	I_{LIL1}	V_{IN} = 0 V	Other than below			-3	uA
	I_{LIL2}		X1, X2, XT1			-20	uA
High level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	uA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5			20	uA
Low level output leakage current	I_{LOL}	V_{OUT} = 0 V				-3	uA
Internal pull-up resistor	R_{LI}	Ports 0, 1, 2, 3, 6, 7 and 8 (other than P00): V_{IN} = 0 V		15	40	80	kΩ
LCD	V_{LCD}			2.5		V_{DD}	V
(Note2) LCD output voltage deviation (Common)	V_{ODC}	I_O = ±5 uA	V_{LCD0}=V_{LCD} V_{LCD1}=V_{LCD}x2/3 V_{LCD2}=V_{LCD}x1/3 2.7 V≤V_{LCD}≤V_{DD}	0		±0.2	V
(Note2) LCD output voltage deviation (Segment)	V_{ODS}	I_O = ±1 uA		0		±0.2	V
(Note3) Supply current	I_{DD1}	(Note4) 4.19 MHz crystal resonator C1 = C2 = 22 pF	Note5		5	15	mA
	I_{DD2}		HALT mode		500	1500	uA
	I_{DD3}	(Note6) 32 kHz ceramic resonator			350	1000	uA
			HALT mode		35	100	
	I_{DD4}	XT1 = 0 V STOP mode			0.5	20	uA

Note 1: When two of BP0-BP3 and two of BP4-BP7 are output at the same time.

2: Voltage deviation shows differences between the expected values (V_{LCDn}; n = 0, 1, 2) of the segment and common output and output voltage.

3: Current flowing into internal pull-up resistor is not contained.

4: The case where subsystem clock is oscillated is also contrained.

5: When the processor clock control register (PCC) is set to 0011 and operated in the high speed mode.

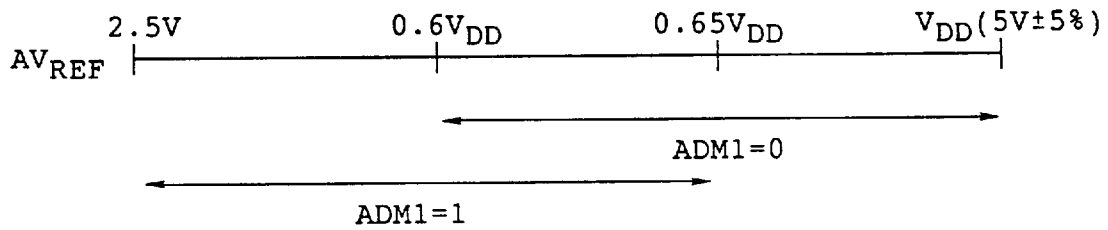
6: When the system clock control register (SCC) is set to 1001, main system clock oscillation is stopped, and operated with subsystem clock.

AD Converter Characteristics (Ta = -10 to +70°C, V_{DD} = 5 V ± 5%, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Absolute accuracy (Note1)		2.5 V ≦ V_{REF} ≦ V_{DD} (Note2)			±1.5	LSB
Conversion time	t_{CONV}	Note3			$168/f_X$	s
Sampling time	t_{SAMP}	Note4			$44/f_X$	s
Analog input voltage	V_{IAN}		AV_{SS}		V_{AREF}	V
Analog input impedance	R_{AN}			1000		MΩ
AV_{REF} current	I_{REF}			1.0	2.0	mA

Note 1: Absolute accuracy except for quantization error (±1/2 LSB).

2: ADM1 is set for the A/D converter reference voltage (AV_{REF}), as shown below:



If $0.6V_{DD} \leqq AV_{REF} \leqq 0.65V_{DD}$, it can be used for either 0 or 1.

3: Time to EOC = 1 after conversion start instruction execution (40.1 us when f_X = 4.19 MHz)

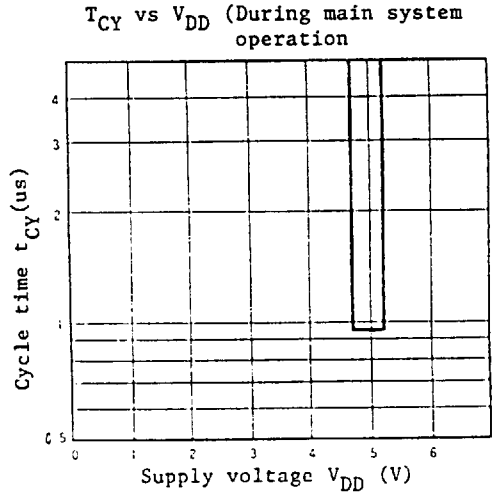
4: Time to sampling end after conversion start instruction execution (10.5 us when f_X = 4.19 MHz)

AC Characteristics (Ta = -10 to +70°C, V_{DD} = 5 V ± 5%)

Operation other than serial transfer

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
(Note 1) CPU clock cycle time (minimum instruction execution time = 1 machine cycle	t_{CY}	Operation with main system clock	0.95		64	us
		Operation with subsystem clock	114	122	125	us
TI0 input frequency	f_{TI}		0		1	MHz
TI0 input high/low level width	t_{TIH}, t_{TIL}		0.48			us
Interrupt input high/low level width	t_{INTH},	INT0	(Note 2)			us
	t_{INTL}	KR0-KR7, INT1, 2, 4	10			us
$\overline{RESET}$ low level widht	t_{RSL}		10			us

Note 1: The cycle time of CPU clock (Φ) is determined by the oscillation frequency of the connected resonator, the system clock control register (SCC), and the processor clock control register (PCC). The figure shows the V_{DD} to cycle time (t_{CY}) when operated with the main system clock.



2: $2t_{CY}$ or $128/f_X$, depending on the setting of the interrupt mode register (IM0).

Serial Transfer Operation

2-line/3-line serial I/O mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCYI}		Output	1600			ns
$\overline{SCK}$ high/low level width	t_{KHI}, t_{KLI}		Output	$t_{KCYI}/2-50$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIKI}			150			ns
SI hold time (to $\overline{SCK}\uparrow$)	t_{KSII}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSOI}	(Note) R_L=1kΩ, C_L=100pF				250	ns

2-line/3-line serial I/O mode ($\overline{SCK}$: External clock input)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		Input	800			ns
$\overline{SCK}$ high/low level width	t_{KH2}, t_{KL2}		Input	400			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (to $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	(Note) R_L=1kΩ, C_L=100pF				300	ns

Note: R_L and C_L are SO output line load resistance and load capacitance.

SBI Mode ($\overline{SCK}$: Internal Clock Output (Master)):

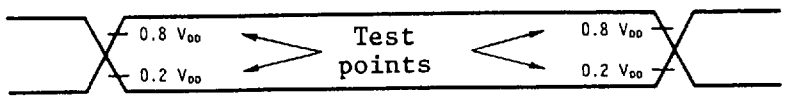
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}		1600			ns
$\overline{SCK}$ high/low level width	t_{KH3}, t_{KL3}		$t_{KCY3}/2-50$			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK3}		150			ns
SB0, 1 hold time (to $\overline{SCK}$↑)	t_{KSI3}		$t_{KCY3}/2$			ns
SB0, 1 output delay time from $\overline{SCK}$↓	t_{KSO3}	(Note) R_L=1kΩ, C_L=100kΩ	0		250	ns
SB0, 1 from $\overline{SCK}$↓	t_{KSB}		t_{KCY3}			ns
$\overline{SCK}$↓ from SB0, 1↓	t_{SBK}		t_{KCY3}			ns
SB0, 1 low level width	t_{SBL}		t_{KCY3}			ns
SB0, 1 high level width	t_{SBH}		t_{KCY3}			ns

SBI Mode ($\overline{SCK}$: External Clock Input (Slave)):

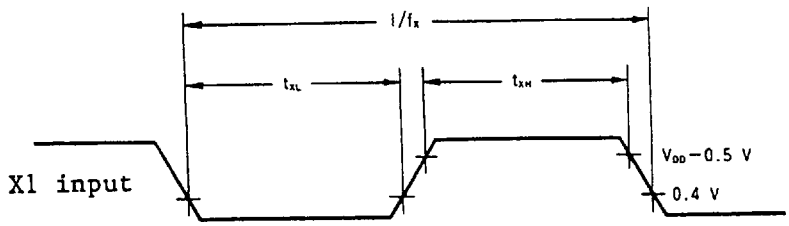
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK}$ high/low level width	t_{KH4}, t_{KL4}		400			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK4}		100			ns
SB0, 1 hold time (to $\overline{SCK}$↑)	t_{KSI4}		$t_{KCY4}/2$			ns
SB0, 1 output delay time from $\overline{SCK}$↓	t_{KSO4}	(Note) R_L=1kΩ, C_L=100kΩ	0		300	ns
SB0, 1↓ from $\overline{SCK}$↑	t_{KSB}		t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, 1↓	t_{SBK}		t_{KCY4}			ns
SB0, 1 low level width	t_{SBL}		t_{KCY4}			ns
SB0, 1 high level width	t_{SBH}		t_{KCY4}			ns

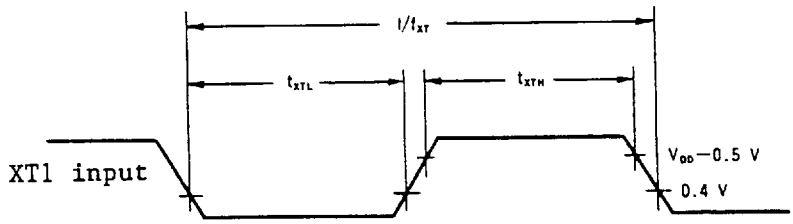
Note: R_L and C_L are SO output line load resistance and load capacitance.

AC Timing Test Points (except X1 and XT1 input)

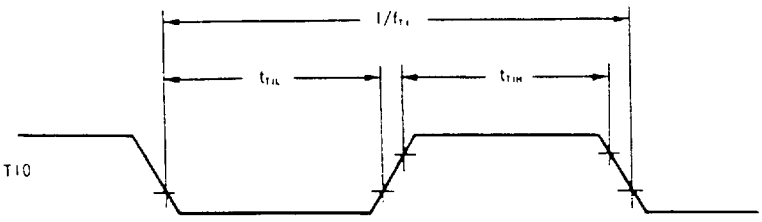


Clock Timing



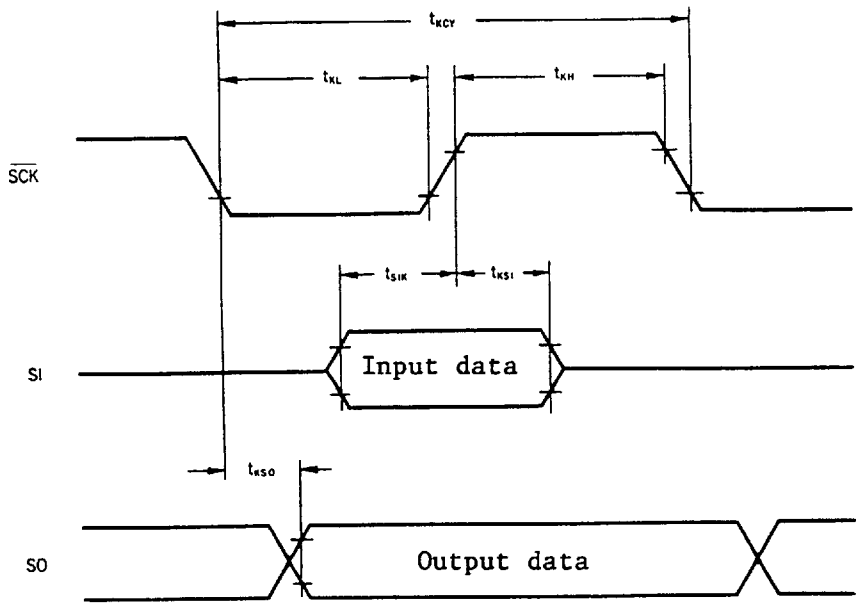


TI0 Timing

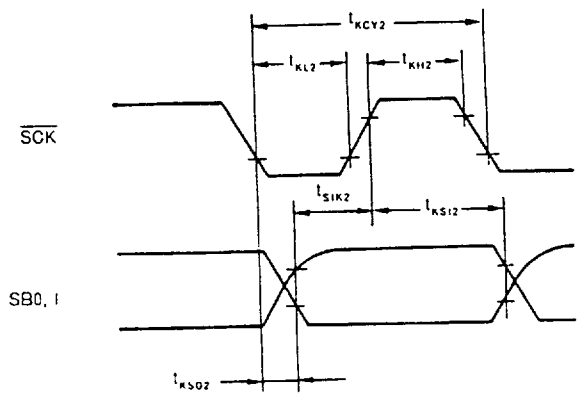


Serial Transfer Timing

3-line serial I/O mode:

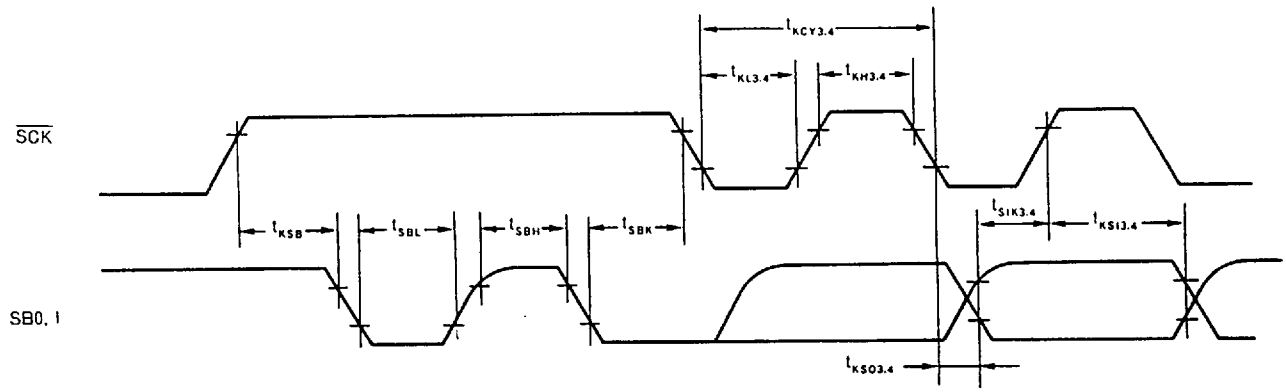


2-line serial I/O mode:

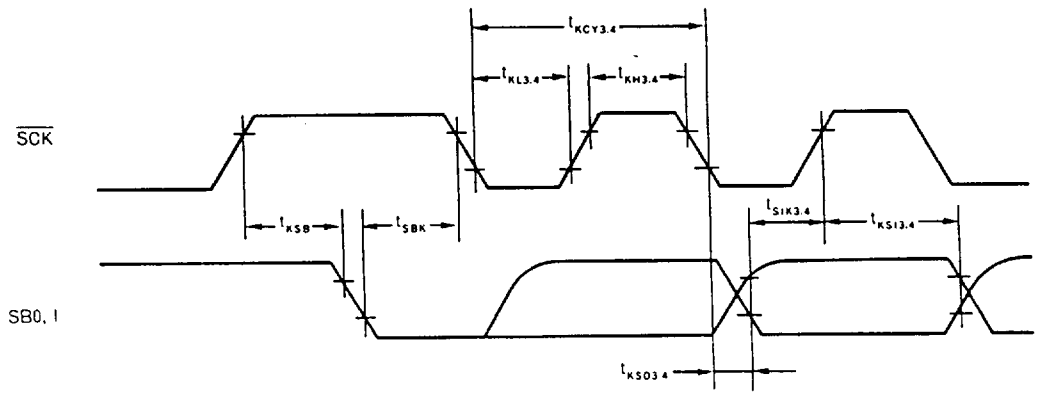


Serial Transfer Timing (SBI Mode)

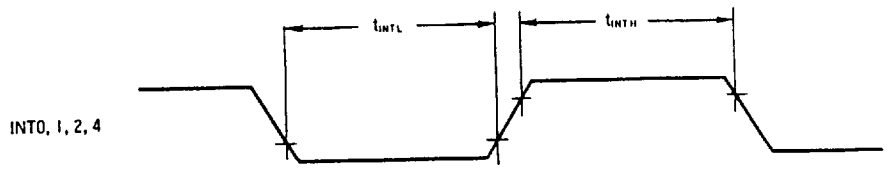
Bus release signal transfer:



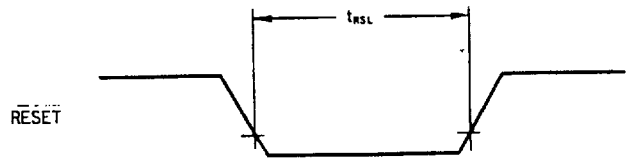
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data Memory STOP Mode Low Voltage Data Retention Characteristics (Ta = -10 to +70°C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current (Note1)	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	uA
Release signal setup time	t_{SREL}		0			us
Oscillation stable time (Note2)	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		(Note3)		ms

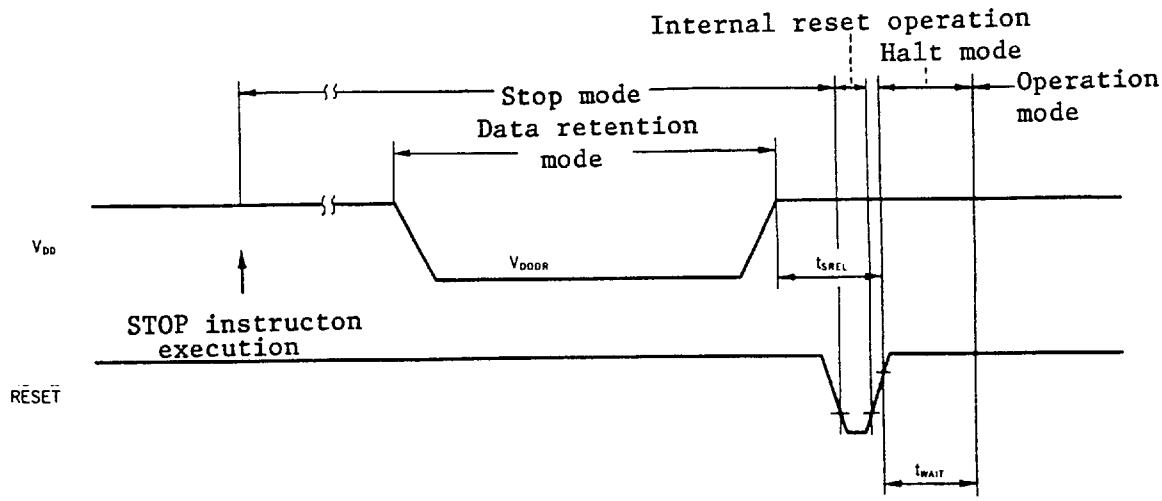
Note 1: Current flowing into the internal pull-up resistors is not contained.

2: The oscillation stable time is the time required before beginning CPU operation in order to prevent unstable CPU operation when oscillation is initiated.

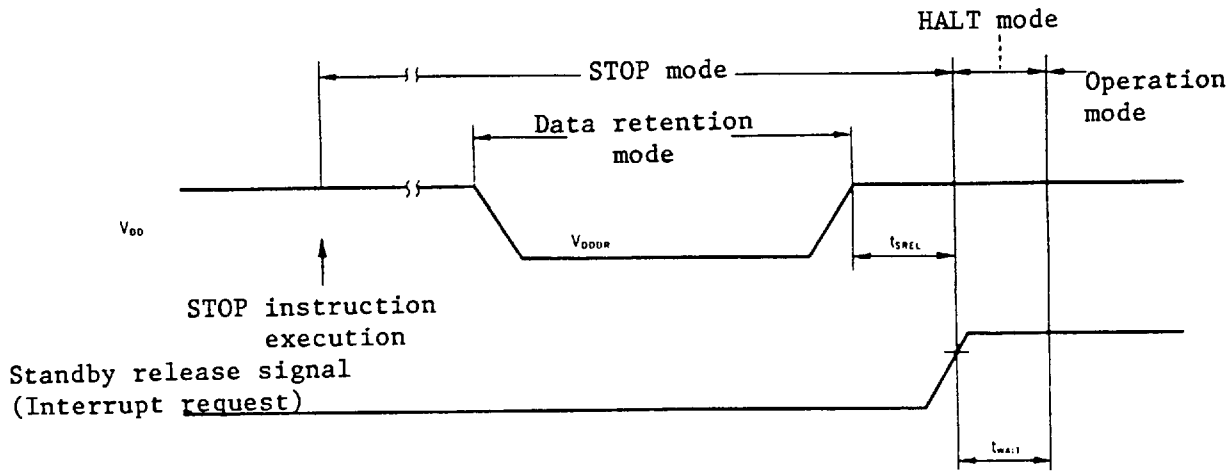
3: Depends on the setting of the basic interval timer mode register (BTM) (refer to the table below)

BTM3	BTM2	BTM1	BTM0	WAIT time ( ) indicates f_X = 4.19 MHz
-	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
-	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
-	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
-	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

Data Retention Timing (STOP Mode Released by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode is Released by Interrupt Signal)



DC Programming characteristics

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH1}	Except XI or X2	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	XI, X2	$V_{DD}-0.5$		V_{DD}	V
Input low voltage	V_{IL1}	Except X1 or X2	0		$0.3V_{DD}$	V
	V_{IL2}	XI, X2	0		0.4	V
Input leakage current	I_{L1}	$V_{IN}=V_{IL}$ or V_{IH}			10	uA
Output high voltage	V_{OH}	$I_{OH}=-1mA$	$V_{DD}-1.0$			V
Output low voltage	V_{OL}	$I_{OL}=1.6mA$			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MDO=V_{IL}, MDI=V_{IH}			30	mA

Caution 1: Suppress V_{PP} to less than +13.5 V containing overshoot.

2: Apply voltage to V_{DD} before V_{PP} and disconnect V_{DD} after V_{PP}.

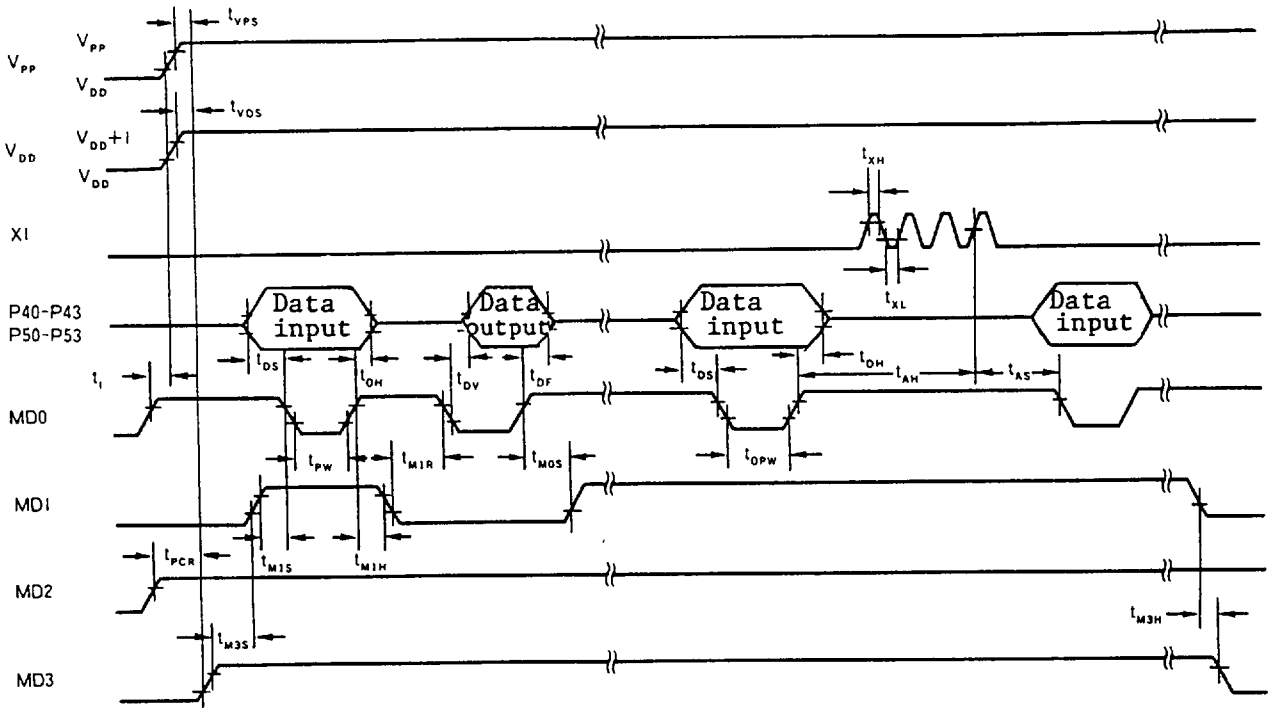
AC programming characteristics (Ta=25±5°C, V_{DD}=6.0±0.25V, V_{PP}=12.5±0.3V, V_{SS}=0V)

Parameter	Symbol	(Note)	Test conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to MD0↓) (Note 2)	t_{AS}	t_{AS}		2			us
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			us
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			us
Address hold time (from MD0↓) (Note 2)	t_{AH}	t_{AH}		2			us
Data hold time (from MD0↓)	t_{DH}	t_{DH}		2			us
MD0↑ → data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			us
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			us
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{MOS}	t_{CES}		2			us
MD0↓ → data output delay time	t_{DV}	t_{DV}	MD0=MD1=V_{IL}			1	us
MD1 hold time (from MD0↓)	t_{M1H}	t_{OEH}	$t_{M1H}+t_{M1R}\geq 50us$	2			us
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			us
Program counter reset time	t_{PCR}	-		10			us
X1 input high, low level width	t_{XH},t_{XL}	-		0.125			us
X1 input frequency	f_X	-				4.19	MHZ
Initial mode set time	t_I	-		2			us
MD3 setup time (to MD1↑)	t_{M3S}	-		2			us
MD3 hold time (from MD1↑)	t_{M3H}	-		2			us
MD3 setup time (to MD0↓)	t_{M3SR}	-	When program memory is read	2			us
Address → data output delay time (Note 2)	t_{DAD}	t_{ACC}	When program memory is read			2	us
Address → data output hold time (Note 2)	t_{HAD}	t_{OH}	When program memory is read	0		130	ns
MD3 hold time (from MD0↓)	t_{M3HR}	-	When program memory is read	2			us
MD3↓ → data output float delay time	t_{DFR}	-	When program memory is read			2	us

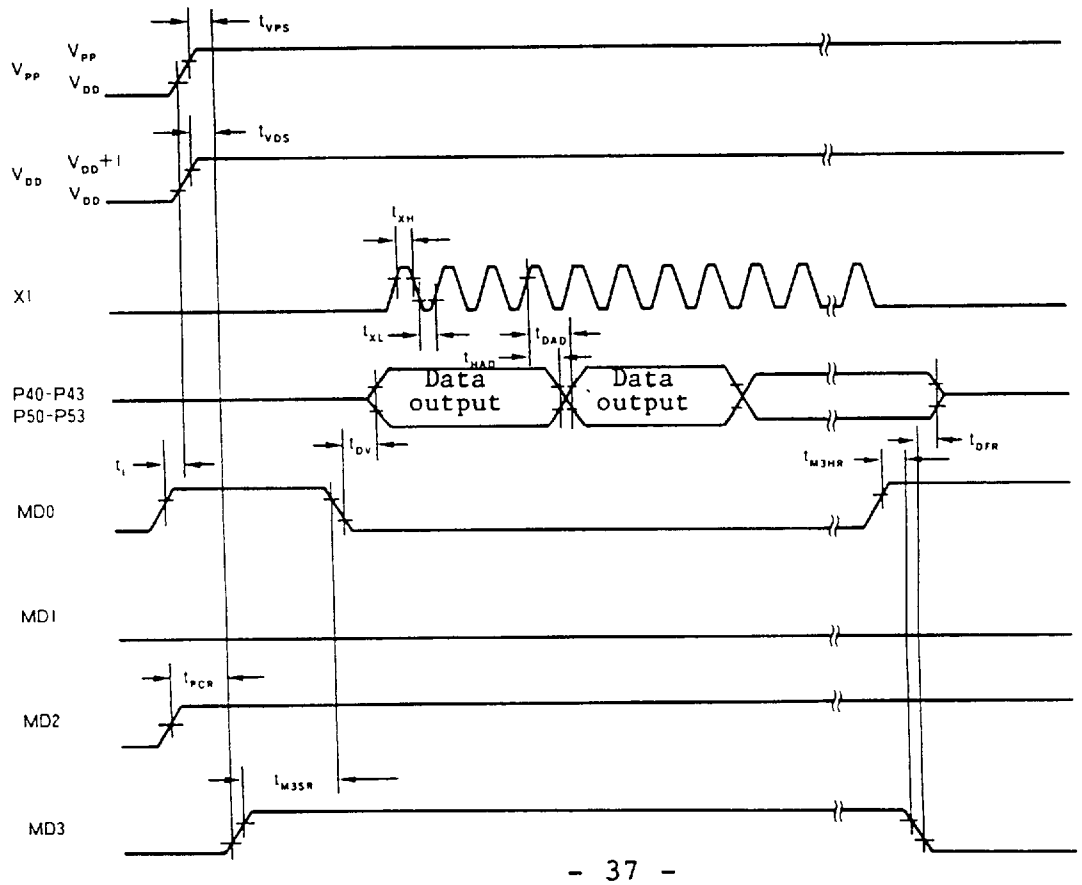
Note 1: Corresponding uPD27C256A symbol.

2: The internal address signal is incremented by one on the fourth X1 input rising edge, and is not connected to pin.

Program memory write timing

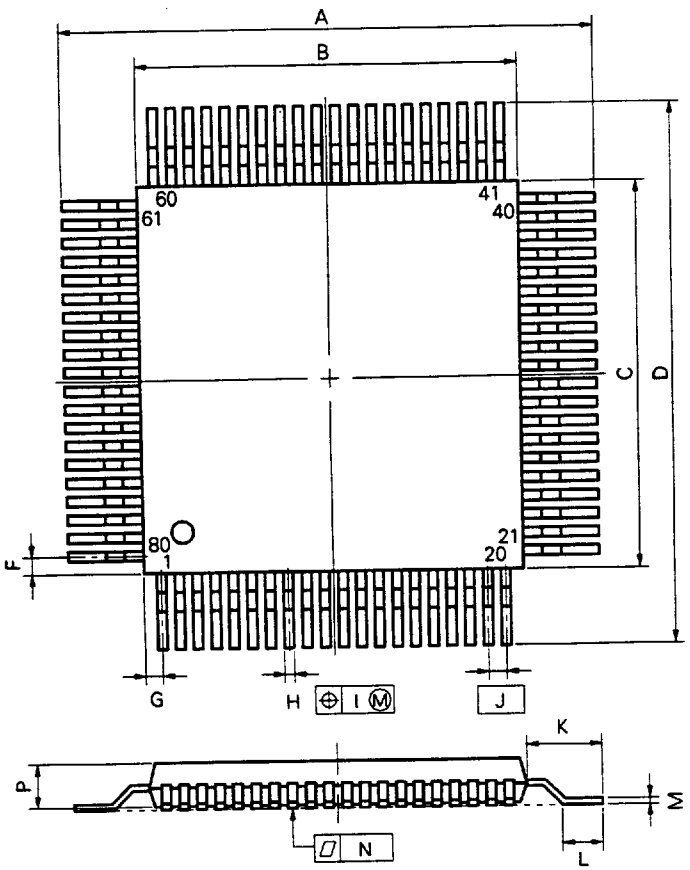


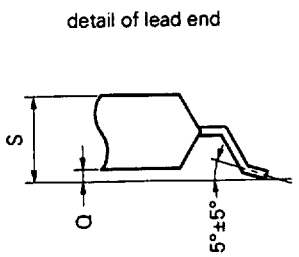
Program memory read timing



5. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14)





S80GC-65-3B9-3

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

6. RECOMMENDED CONDITIONS FOR SOLDERING

Solder the uPD75P328 under the recommended conditions listed below.

Refer to the infomation document "Semiconductor Device Mount Manual" (IEI-616) for details of the recommended conditions for soldering.

Consult the NEC sales person about soldering methods and soldering conditions other than listed below.

Table 6-1 List of recommended conditions for soldering

uPD75P328GC-3B9: 80-pin plastic quad-flat package (□ 14mm)

Soldering method	Soldering method	Recommended condition symbol
Infrared reflow	Package peak temperature: 230°C, Time: Within 30s (at 210°C or higher), Count: Once Limited number of days: Two days(Note) (after the days, prebake is required at 125°C for 16 hours)	IR30-162-1
VPS	Package peak temperature: 215°C, Time: Within 40s (at 200°C or higher), Count: Once, Limited number of days: Two days(Note) (after the days, preabake is required at 125°C for 16 hours)	VP15-162-1
Wave soldering	Soldering tank temperature: 260°C or less, Time: Within 10s, Count: Once, Preheating temperature: 120°C MAX. (Package surface temperature), Limited number of days: Two days(Note) (after the days, prebake is required at 125°C for 16 hours)	WS60-162-1
Pin part heating	Pin part temerature: 300°C, Time: Within 3s (per frame of device)	——

Note: Number of storage days under storage conditions of 25°C and 65%RH or less after the dry pack is opened.

Caution: Do not use the soldering methods together (except the pin part heating).

Information

The product contains a soldering recommended condition improvement product.
(Improvement contents: Infrared ray reflow peak temperature extension (235°C), count twice, lessening of the number of limited days, etc.)
For details, ask the NEC sales person.

APPENDIX A DEVELOPMENT TOOLS

The following development tools are provided for system development using the uPD75P328:

Hardware	IE-75000-R(Note 1) IE-75001-R	In-circuit emulators for 75X series
	IE-75000-R-EM(Note 2)	Emulation board for IE-75000-R and IE-75001-R
	EP-75328GC-R EV-9200GC-80	uPD75P328 emulation probe, 80-pin conversion socket EV-9200GC-80 is attached.
	PG-1500	PROM programmer
	PA-75P328GC	uPD75P328 PROM programmer adapter which is connected to PG-1500.
Software	IE control program	Host machine PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A(Note 3)) IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

Note 1: Maintenance product

2: Not contained in IE-75001-R.

3: Although Ver. 5.00/5.00A provides the task swap function, the function cannot be used under the software.

Remarks: For development tools developed by third parties, refer to 75X Series Selection Guide (IF-151).

APPENDIX B RELATED DOCUMENTS

Documents related to device

Title	Doc. No
User's Manual	IEM-5045
Instruction Quick Reference	IEM-5031
75X Series Selection Guide	IF-151

Documents related to development tool

Title			Doc. No
Hard-ware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75328GC-R User's Manual		EEU-690
	PG-1500 User's Manual		EEU-651
Soft-ware	RA75X Assembler Package User's Manual	Operation	EEU-731
		Language	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Documents related to device

Title	Doc. No
Package Manual	IEI-635
Semiconductor Mount Technology Manual	IEI-616
Quality Grades on NEC Semiconductor Devices	IEI-620
NEC Semiconductor Device Reliability/ Quality Control System	IEM-5068
Electrostatic Discharge (ESD) Test	MEM-539
Guide to Quality Assurance for Semiconductor Devices	MEI-603
Microcomputer-Related Product Guide - Third Party Products -	MEI-604

Caution: The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.