DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The NEC μPD7720 Signal Processing Interface (SPI) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the SPI to efficiently implement signal processing functions in a wide range of environments and applications.

The NEC SPI is the state of the art in signal processing today, and for the future.

APPLICATIONS

- Speech Synthesis and Analysis
- Digital Filtering
- Fast Fourier Transforms (FFT)
- Dual-Tone Multi-Frequency (DTMF) Transmitters/Receivers
- High Speed Data Modems
- Equalizers
- Adaptive Control
- Sonar/Radar Image Processing
- Numerical Processing

PERFORMANCE BENCHMARKS

• Second Order Digital Filter (BiQuad)	2.25 μs
• SINE/COS of Angles	5.25 μs
• μ/A LAW to Linear Conversion	0.50 μs
• FFT: 32 Point Complex	0.7 ms
64 Point Complex	1.6 ms

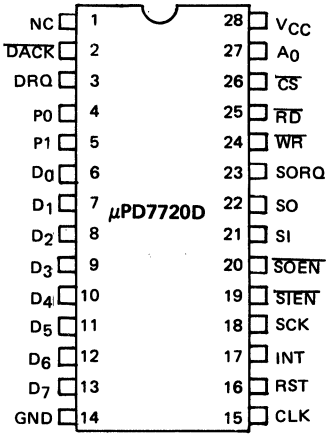
FEATURES

- Fast Instruction Execution – 250 ns
- 16 Bit Data Word
- Multi-Operation Instructions for Optimizing Program Execution
- Large Memory Capacities
  - Program ROM 512 x 23 Bits
  - Coefficient ROM 510 x 13 Bits
  - Data RAM 128 x 16 Bits
- Fast (250 ns) 16 x 16-31 Bit Multiplier
- Dual Accumulators
- Four Level Subroutine Stack for Program Efficiency
- Multiple I/O Capabilities
  - Serial
  - Parallel
  - DMA
- Compatible with Most Microprocessors, Including:
  - μPD8080
  - μPD8085
  - μPD8086
  - μPD780 (Z80™*)
- Power Supply +5V
- Technology NMOS
- Package – 28 Pin Dip

9

*Z80 is a trademark of Zilog Corporation.

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Fabricated in high speed NMOS, the μPD7720 SPI is a complete 16-bit microcomputer on a single chip. ROM space is provided for program and coefficient storage, while the on-chip RAM may be used for temporary data, coefficients and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 x 16 bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 nsec instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughput. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional μP for more sophisticated applications. Handshaking signals, including DMA controls, allow the SPI to act as a sophisticated programmable peripheral as well as a stand alone microcomputer.

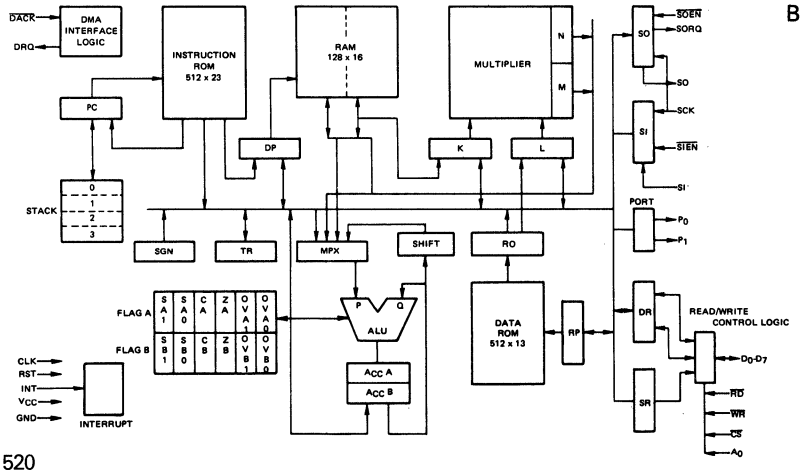
MEMORY

Memory is divided into three types, Program ROM, Data ROM, and Data RAM. The 512 x 23 bit words of Program ROM are addressed by a 9-bit Program Counter which can be modified by an external reset, interrupt, call, jump, or return instruction.

The Data ROM is organized in 512 x 13 bit words and is also addressed through a 9-bit ROM pointer (RP Reg.) which may be modified as part of an arithmetic instruction so that the next value is available for the next instruction. The Data ROM is ideal for storing the necessary coefficients, conversion tables and other constants for all your processing needs.

The Data RAM is 128 x 16 bit words and is addressed through a 7-bit Data Pointer (DP Reg.). The DP has extensive addressing features that operate simultaneously with arithmetic instructions so that no added time is taken for addressing or address modification.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN	NAME	I/O	FUNCTION
1	NC	I	No Connection.
2	$\overline{DACK}$	I	DMA Request Acknowledge. Indicates to the μPD7720 that the Data Bus is ready for a DMA transfer. ($\overline{DACK} = \overline{CS} \bullet A_0 = 0$)
3	DRQ	O	DMA Request signals that the μPD7720 is requesting a data transfer on the Data Bus.
4,5	P_0, P_1	O	P_0, P_1 are general purpose output control lines.
6-13	D_0-D_7	I/O Tristate	Port for data transfer between the Data Register or Status Register and Data Bus.
14	GND		
15	CLK	I	Single phase Master Clock input.
16	RST	I	Reset initializes the μPD7720 internal logic and sets the PC to 0.
17	INT	I	Interrupt. A low to high transition on this pin will (if interrupts are enabled by the program) execute a call instruction to location 100H.
18	SCK	I	Serial Data Input/Output Clock. A serial data bit is transferred when this pin is high.
19	$\overline{SIEN}$	I	Serial Input Enable. This line enables the shift clock to the Serial Input Register.
20	$\overline{SOEN}$	I	Serial Output Enable. This pin enables the shift clock to the Serial Output Register.
21	SI	I	Serial Data Input. This pin inputs 8 or 16 bit serial data words from an external device such as an A/D converter.
22	SO	O	Serial Data Output. This pin outputs 8 or 16 bit data words to an external device such as an D/A converter.
23	SORQ	O	Serial Data Output Request. Specifies to an external device that the Serial Data Register has been loaded and is ready for output. SORQ is reset when the entire 8 or 16 bit word has been transferred.
24	$\overline{WR}$	I	Write Control Signal writes the contents of data bus into the Data Register.
25	$\overline{RD}$	I	Read Control Signal. Enables an output to the Data Port from the Data or Status Register.
26	$\overline{CS}$	I	Chip Select. Enables data transfer with Data or Status Port with $\overline{RD}$ or $\overline{WR}$.
27	A_0	I	Selects Data Register for Read/Write (low) or Status Register for read (high).
28	V_{CC}		+5V Power

ARITHMETIC CAPABILITIES

General

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multipler, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add, or other arithmetic operation, and move data between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit 2's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators (ACCA/ACCB)

Associated with the ALU are a pair of 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). In addition to Zero Result, Sign Carry, and Overflow Flags, the SPI incorporates auxiliary Overflow and Sign Flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as 3 successive additions or subtractions.

FLAG A	SA1	SA0	CA	ZA	OVA1	OVA0
FLAG B	SB1	SB0	CB	ZB	OVB1	OVB0

ACC A/B FLAG REGISTERS

Sign Register (SGN)

When OVA1 (or OVB1) is set, the SA1 (or SB1) bit will hold the corrected sign of the overflow. The SGN Register will use SA1 (SB1) to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated valve.

Multiplier

Thirty-one bit results are developed by a 16 x 16 bit 2's complement multiplier in 250 ns. The result is automatically latched in 2-16-bit registers M&N (LSB in N is zero) at the end of each instruction cycle. The ability to have a new product available and to be able to use it in each instruction cycle, provides significant advantages in maximizing processing speed for real time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

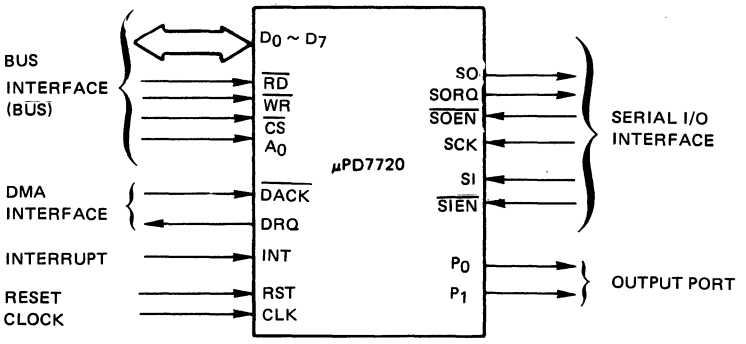
Interrupt

A single level interrupt is supported by the SPI. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register is automatically reset to 0 thus disabling the interrupt facilities until reenabled under program control.

INPUT/OUTPUT

General

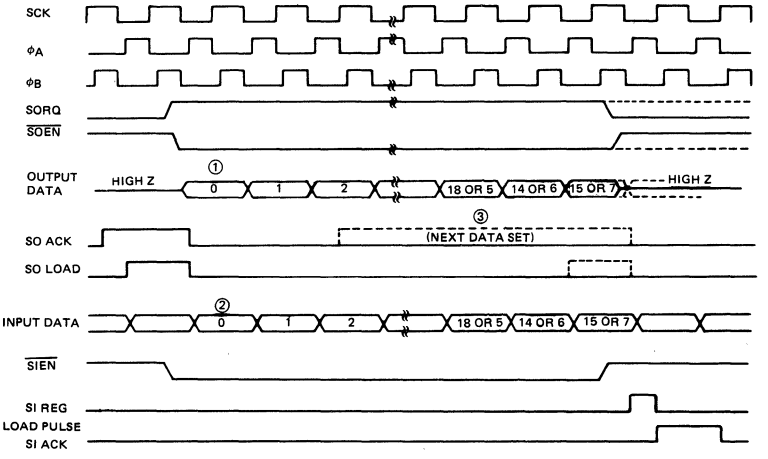
The NEC SPI has 3 communication ports; 2 serial and one 8-bit parallel, each with their own control lines for interface handshaking. The parallel port also includes DMA control lines (DRQ and $\overline{DACK}$) for high speed data transfer and reduced processor overhead. A general purpose 2 bit output (see Figure 1) port, rounds out a full complement of interface capability.



Serial I/O

Two shift registers (SI, SO) that are software-configurable to 8 or 16 bits and are externally clocked (SCK) provide simple interface between the SPI and serial peripherals such as, A/D and D/A converters, codecs, or other SPIs.

SERIAL I/O TIMING



① Data clocked out on falling edge of SCK.

② Data clocked in on rising edge of SCK.

③ Broken line denotes consecutive sending of next data.

PARALLEL I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status. Data transfer is handled through a 16-bit Data Register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085 and 8086 processor buses and may be used with other processors and computer systems.

PARALLEL R/W OPERATION

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	OPERATION
1	X	X	X	No effect on internal operation. D_0-D_7 are at high impedance levels.
X	X	1	1	
0	0	0	1	Data from D_0-D_7 is latched to DR ①
0	0	1	0	Contents of DR are output to D_0-D_7 ①
0	1	0	1	Illegal
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal

① Eight MSBs or 8 LSBs of data register (DR) are used depending on DR status bit (DRS).
The condition of $\overline{DACK}$ = 0 is equivalent to A_0 = $\overline{CS}$ = 0.

Status Register (SR)

MSB LSB

RQM	USF1	USF0	DRS	DMA	DRC	SOC	SIC	EI	0	0	0	0	0	P1	P0

The status register is a 16-bit register in which the 8 most significant bits may be read by the system's MPU for the latest I/O and processing status.

RQM – (Request for Master): A read or write from DR to IDB sets RQM = 1. An Ext read (write) resets RQM = 0.

USF1 – (User Flag 1):
USF0 – (User Flag 0): General purpose flags which may be read by an external processor for user defined signalling

DRS – (DR Status): For 16 bit DR transfers (DRC = 0) DRS = 1 after first 8 bits have been transferred, DRS = 0 after all 16 bits

DMA– (DMA Enable): DMA = 0 (Non DMA transfer mode)
DMA = 1 (DMA transfer mode)

DRC – (DR Control): DRC = 0 (16 bit mode), DRC = 1 (8 bit mode)

SOC – (SO Control): SOC = 0 (16 bit mode), SOC = 1 (8 bit mode)

SIC – (SI Control): SIC = 0 (16 bit mode), SIC = 1 (8 bit mode)

EI – (Enable Interrupt): EI = 0 (interrupts disabled), EI = 1 (interrupts enabled)

P0/P1 (Ports 0 and 1): P0 and P1 directly control the state of output pins P0 and P1

INSTRUCTIONS

The SPI has 3 types of instructions all of which are one word, 23 bits long and execute in 250 ns.

A) Arithmetic/Move-Return (OP = 00/RT = 01)

	22 21	20 19 18 17 16 15	14	13 12	11 10 9	8	7 6 5 4	3 2 1 0
OP	0 0	P-SELECT / ALU	ASL	DP_L	DP_H·M	RPDCR	SRC	DST
RT	0 1	Same as OP instruction						

There are two instructions of this type, both of which are capable of executing all ALU functions listed in Table 2 on the value specified by the ALU input (i.e., P select field see Table 1).

Table 1. OP, RT

Mnemonic	P-Select Field D_{20}	D_{19}	ALU Input
RAM	0	0	RAM
IDB	0	1	*Internal Data Bus
M	1	0	M Register
N	1	1	N Register

*Any value on the on-chip data bus. Value may be selected from any of registers listed in Table 7 source register selections.

Table 2. OP, RT

Mnemonic	ALU Field D_{18}	D_{17}	D_{16}	D_{15}	ALU Function	Flag A / Flag B	Flags Affected SA1 / SB1	SA0 / SB0	CA / CB	ZA / ZB	OVA1 / OVB1	OVA0 / OVB0
NOP	0	0	0	0	No Operation		–	–	–	–	–	–
OR	0	0	0	1	OR		Ø	‡	‡	Ø	Ø	Ø
AND	0	0	1	0	AND		Ø	‡	‡	Ø	Ø	Ø
XOR	0	0	1	1	Exclusive OR		Ø	‡	‡	Ø	Ø	Ø
SUB	0	1	0	0	Subtract		‡	‡	‡	‡	‡	Ø
ADD	0	1	0	1	ADD		‡	‡	‡	‡	‡	‡
SBB	0	1	1	0	Subtract with Borrow		‡	‡	‡	‡	‡	‡
ADC	0	1	1	1	Add with Carry		‡	‡	‡	‡	‡	‡
DEC	1	0	0	0	Decrement A_{CC}		‡	‡	‡	‡	‡	‡
INC	1	0	0	1	Increment A_{CC}		‡	‡	‡	‡	‡	‡
CMP	1	0	1	0	Complement A_{CC} (1's Complement)		‡	‡	‡	Ø	Ø	Ø
SHR1	1	0	1	1	1-bit R-Shift		‡	‡	‡	Ø	Ø	Ø
SHL1	1	1	0	0	1-bit L-Shift		‡	‡	‡	Ø	Ø	Ø
SHL2	1	1	0	1	2-bit L-Shift		Ø	‡	‡	Ø	Ø	Ø
SHL4	1	1	1	0	4-bit L-Shift		Ø	‡	‡	Ø	Ø	Ø
XCHG	1	1	1	1	8-bit Exchange		Ø	‡	‡	Ø	Ø	Ø

‡ Affected by result
– No affect
Ø Reset

Table 3. OP, RT

Mnemonic	ASL Field D_{14}	A_{CC} Selection
ACCA	0	A_{CC} A
ACCB	1	A_{CC} B

Table 4. OP, RT

Mnemonic	DP_L Field D_{13}	D_{12}	DP_3-DP_0
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Table 5. OP, RT

Mnemonic	DP_H-M Field D_{11}	D_{10}	D_9	Exclusive OR
M0	0	0	0	(DP_6 DP_5 DP_4) ¥ (0 0 0)
M1	0	0	1	DP_6 DP_5 DP_4 ¥ (0 0 1)
M2	0	1	0	DP_6 DP_5 DP_4 ¥ (0 1 0)
M3	0	1	1	DP_6 DP_5 DP_4 ¥ (0 1 1)
M4	1	0	0	DP_6 DP_5 DP_4 ¥ (1 0 0)
M5	1	0	1	DP_6 DP_5 DP_4 ¥ (1 0 1)
M6	1	1	0	DP_6 DP_5 DP_4 ¥ (1 1 0)
M7	1	1	1	DP_6 DP_5 DP_4 ¥ (1 1 1

Table 6. OP,RT

Mnemonic	RPDCR D_8	Operation
RPNOP	0	No Operation
RPDEC	1	Decrement RP

Besides the arithmetic functions these instructions can also modify (1) the RAM Data Pointer DP, (2) the Data ROM Pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in Tables 7 and 8 respectively). The difference in the two instructions of this type is that one executes a subroutine or interrupt return at the end of the instruction cycle while the other does not.

Table 7. OP, RT

Mnemonic	SRC Field D_7	D_6	D_5	D_4	Specified Register
NON	0	0	0	0	NO Register
A	0	0	0	1	ACC A (Accumulator A)
B	0	0	1	0	ACC B (Accumulator B)
TR	0	0	1	1	TR Temporary Register
DP	0	1	0	0	DP Data Pointer
RP	0	1	0	1	RP ROM Pointer
RO	0	1	1	0	RO ROM Output Data
SGN	0	1	1	1	SGN Sign Register
DR	1	0	0	0	DR Data Register
DRNF	1	0	0	1	DR Data No Flag ①
SR	1	0	1	0	SR Status
SIM	1	0	1	1	SI Serial in MSB ②
SIL	1	1	0	0	SI Serial in LSB ③
K	1	1	0	1	K Register
L	1	1	1	0	L Register
MEM	1	1	1	1	RAM

① DR to IDB RQM not set. IN DMA DRQ not set.
② First bit in goes to MSB, last bit to LSB.
③ First bit in goes to LSB, last bit to MSB (bit reversed).

Table 7 — List of Registers Specified by the Source Field (SRC)

Table 8. OP, RT, LDI

Mnemonic	DST Field D_3	D_2	D_1	D_0	Specified Register
@NON	0	0	0	0	NO Register
@A	0	0	0	1	ACC A (Accumulator A)
@B	0	0	1	0	ACC B (Accumulator B)
@TR	0	0	1	1	TR Temporary Register
@DP	0	1	0	0	DP Data Pointer
@RP	0	1	0	1	RP ROM Pointer
@DR	0	1	1	0	DR Data Register
@SR	0	1	1	1	SR Status Register
@SOL	1	0	0	0	SO Serial Out LSB ①
@SOM	1	0	0	1	SO Serial Out MSB ②
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB → K ROM → L ③
@KLM	1	1	0	0	Hi RAM → K IDB → L ④
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	NO Register
@MEM	1	1	1	1	RAM

① LSB is first bit out.
② MSB is first bit out.
③ Internal data bus to K and ROM to L register.
④ Contents of RAM address specified by $DP_6 = 1$ (i.e., 1, DP_5, DP_4,-DP_0) is placed in K register. IDB is placed in L.

Table 8 — List of Registers Specified by the Destination Field (DST)

B) Jump/Call/Branch

22 21	20 19 18	17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
10	BRCH	CND	NA

JP Instruction Field Specifications

Three types of execution address modification instructions are accommodated by the processor and are listed in Table 9. All of the instructions, if unconditional or the specified condition is true, take their next program execution address from the Next Address field (NA), otherwise PC = PC + 1.

Table 9. Branch Field Selections (BRCH)

20	19	18	Instruction
1	0	0	Uncondition jump
1	0	1	Subroutine call
0	1	0	Condition jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 10 lists all the instruction mnemonics of the J/C/B OP codes.

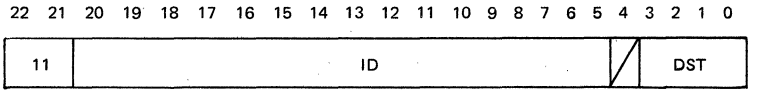
The SPI offers all the execution modification instructions necessary for efficient, data, I/O and arithmetic control.

Table 10. Condition Field Specifications

Mnemonic	BRCH/CND Fields								Conditions
	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	
JMP	1	0	0	0	0	0	0	0	No Condition
CALL	1	0	1	0	0	0	0	0	No Condition
JNCA	0	1	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	CA = 1
JNCB	0	1	0	0	0	0	1	0	CB = 0
JCB	0	1	0	0	0	0	1	1	CB = 1
JNZA	0	1	0	0	0	1	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	ZA = 1
JNZB	0	1	0	0	0	1	1	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	$DP_L = 0$
JDPLF	0	1	0	1	1	0	0	1	DP_L = F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	RQM = 1

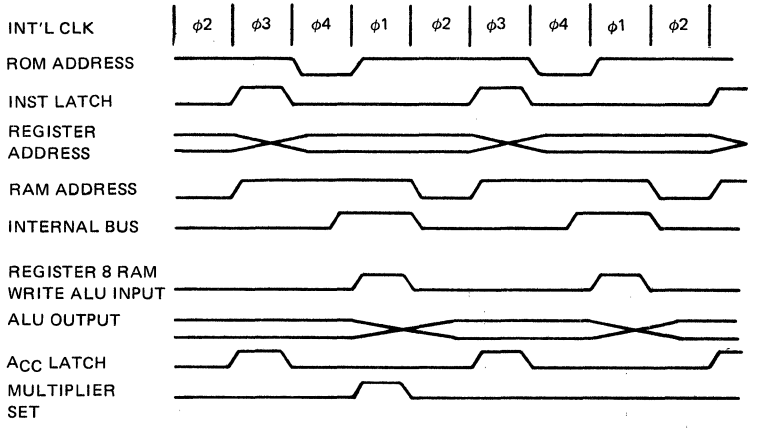
*BRCH or CND values not in this table are prohibited.

C) **Load Data (LDI)**



The Load Data instruction will take the 16-bit value contained in the Immediate Data field (ID) and place it in the location specified by the Destination field (DST) (see Table 8).

Load Data Field Specifications



INSTRUCTION EXECUTION TIMING

ABSOLUTE MAXIMUM RATINGS*

Voltage (V_{CC} Pin) . . . . . −0.5 to +7.0 Volts ①
Voltage, Any Input . . . . . −0.5 to +7.0 Volts ①
Voltage, Any Output . . . . . −0.5 to +7.0 Volts ①
Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C

Note: ① With respect to GND.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 ~ +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.5	V	
CLK Low Voltage	$V_{\phi L}$	−0.5		0.45	V	
CLK High Voltage	$V_{\phi H}$	3.5		V_{CC} +0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{LIL}			−10	μA	V_{IN} = 0V
Input Load Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}			−10	μA	V_{OUT} = V_{CC}
Output Float Leakage	I_{LOH}			10	μA	V_{OUT} = 0.47V
Power Supply Current	I_{CC}		200	280	mA	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK, SCK Input Capacitance	C_ϕ			20	pF	f_c = 1 MHz
Input Pin Capacitance	C_{IN}			10	pF	
Output Pin Capacitance	C_{OUT}			20	pF	

9

AC CHARACTERISTICS

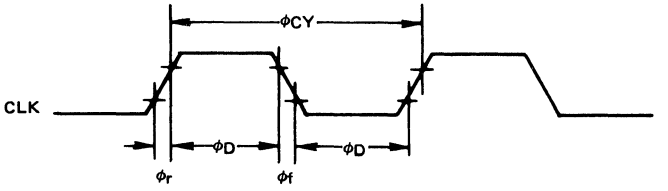
$T_a = -10 \sim +70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK Cycle Time	ϕCY	125		2000	ns	
CLK Pulse Width	ϕD	50			ns	
CLK Rise Time	ϕR			20	ns	
CLK Fall Time	ϕF			20	ns	
Address Setup Time for $\overline{RD}$	t_{AR}	0			ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0			ns	
RD Pulse Width	t_{RR}	200			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	C_L = 100 pF
Read to Data Floating	t_{DF}	20		100	ns	C_L = 100 pF
Address Setup Time for $\overline{WR}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	200			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
DRQ Delay	t_{AM}			150	ns	C_L = 100 pF
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise/Fall Time	t_{RSC}			20	ns	
$\overline{SORQ}$ Delay	t_{DRQ}	30		150	ns	C_L = 100 pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	10			ns	
SO Delay	t_{DCK}			150	ns	
SO Delay from $\overline{SORQ}$	t_{DZRQ}	*				
SO Delay from SCK	t_{DZSC}	*				
SO Delay from $\overline{SOEN}$	t_{DZE}	*				
$\overline{SOEN}$ to SO Floating	t_{HZE}	*				
SCK to SO Floating	t_{HZSC}	*				
$\overline{SORQ}$ to SO Floating	t_{HZRQ}	*				
$\overline{SIEN}$, SI Setup Time	t_{DC}	50			ns	
$\overline{SIEN}$, SI Hold Time	t_{CD}	20			ns	
P_0, P_1 Delay	t_{DP}			300	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

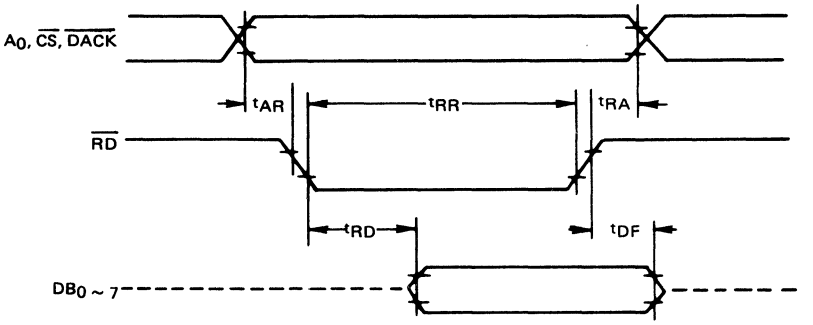
*To be specified

TIMING WAVEFORMS

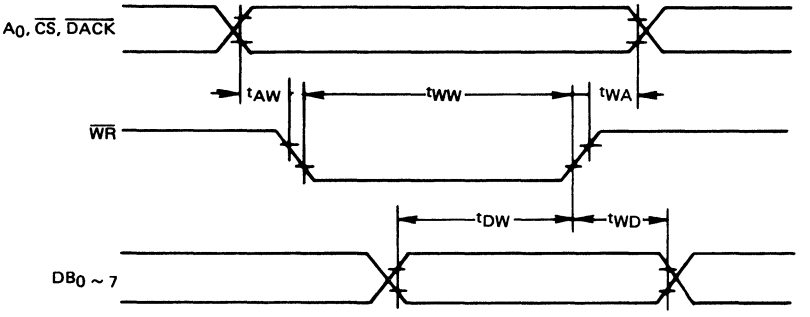
CLOCK



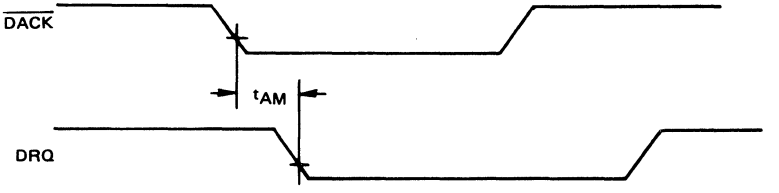
READ OPERATION



WRITE OPERATION



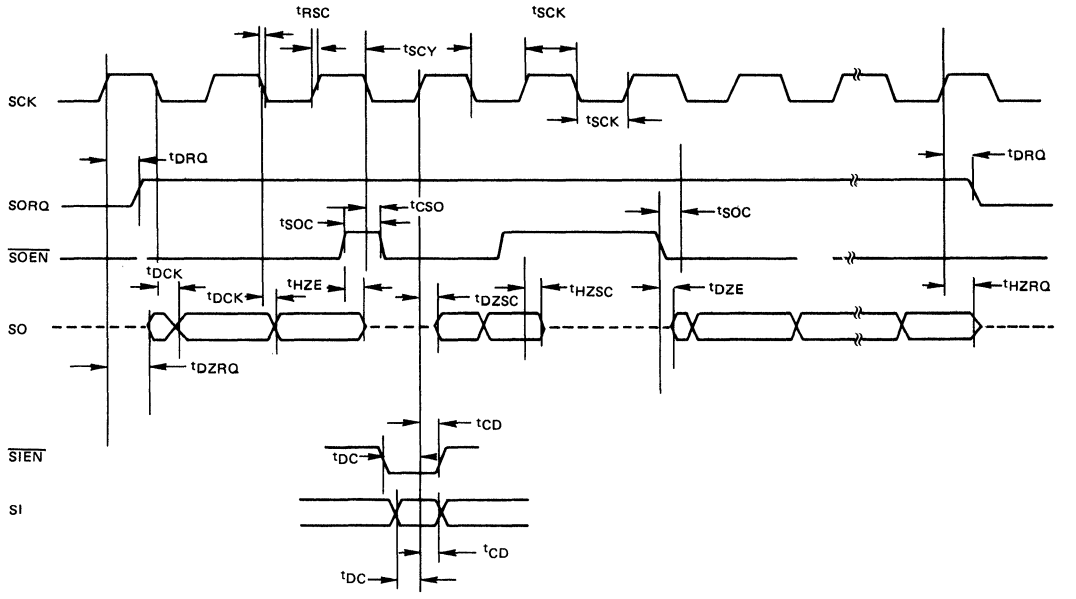
DMA OPERATION



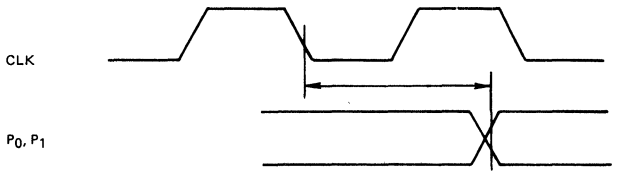
9

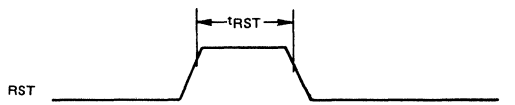
SERIAL TIMING

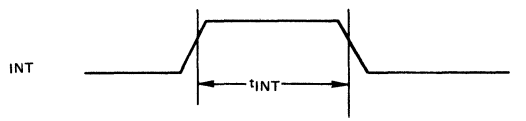
TIMING WAVEFORMS (CON'T.)

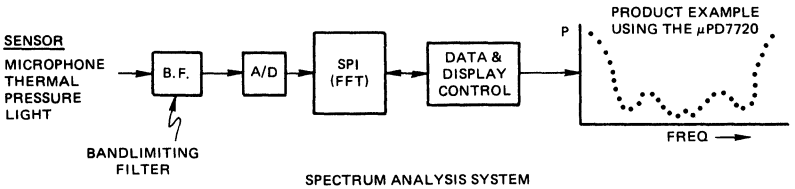


PORT OUTPUT



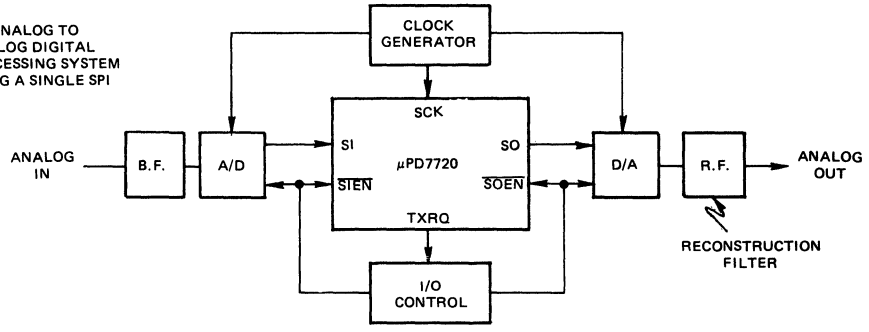


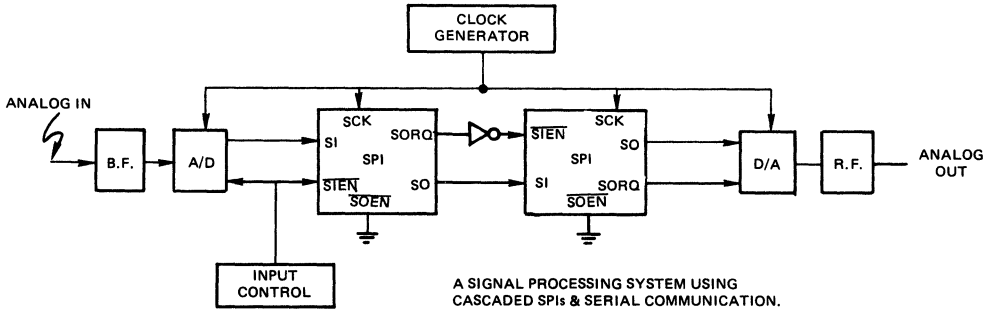




SPECTRUM ANALYSIS SYSTEM

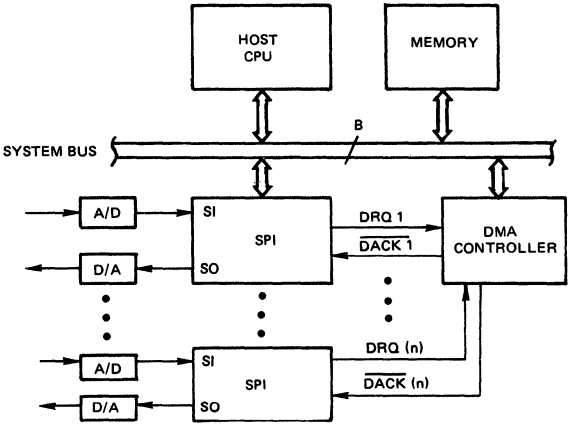
AN ANALOG TO
ANALOG DIGITAL
PROCESSING SYSTEM
USING A SINGLE SPI





A SIGNAL PROCESSING SYSTEM USING
CASCADED SPIs & SERIAL COMMUNICATION.

A SIGNAL PROCESSING
SYSTEM USING SPI(s)
AS A COMPLEX COMPUTER
PERIPHERAL



9