

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 6K ROM

PRODUCT DESCRIPTION

The NEC μPD7802 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

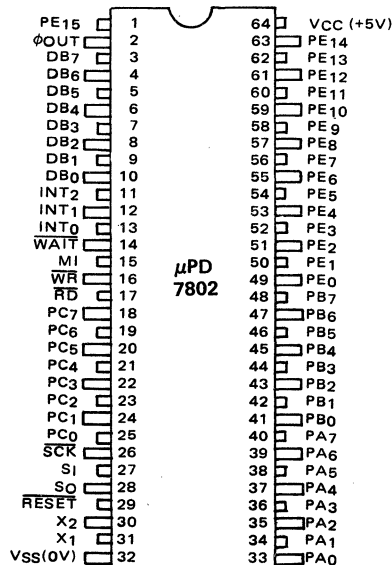
The NEC μPD7802 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks — 6144 x 8 of ROM program memory, 64 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance stand-alone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 6K bytes of ROM program memory and 64 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7802 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

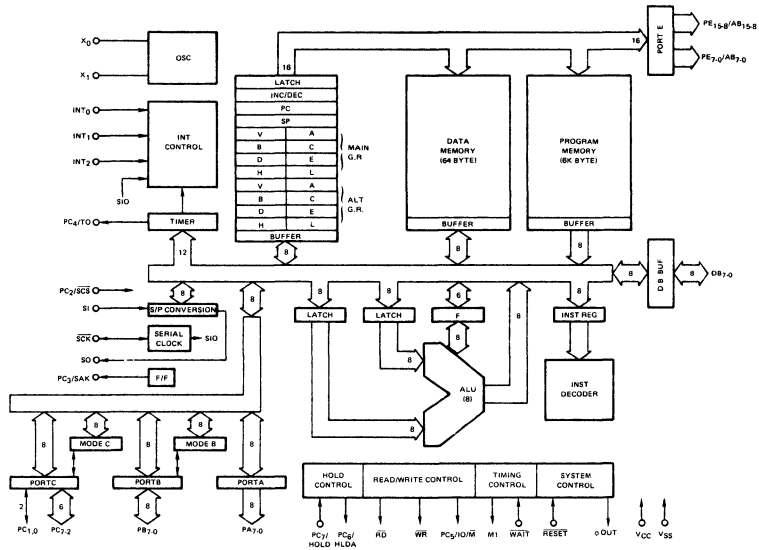
- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
 - 6K Bytes ROM
 - 64 Bytes RAM
 - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
 - Serial Port
 - Timer
 - 3 External Interrupts
- Bus Expansion Capabilities
 - Fully 8080A Bus Compatible
 - 58K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

PIN CONFIGURATION



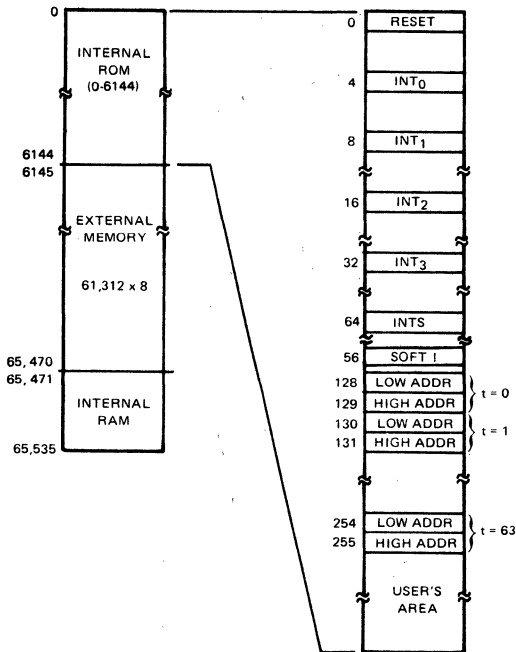
PIN NO.	DESIGNATION	FUNCTION
1, 49-63 2	AB ₀ -AB ₁₅ φOUT	(Tri-State, Output) 16-bit address bus. (Output) φOUT provides a prescaled output clock for use with external I/O devices or memories. φOUT frequency is fXTAL/2.
3-10	DB ₀ -DB ₇	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT ₀	(Input, active high) Level-sensitive interrupt input.
12	INT ₁	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT ₂	(Input) INT ₂ is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT ₂ is rising edge sensitive. When ES is set to 0, INT ₂ is falling edge sensitive.
14	WAIT	(Input, active low) WAIT, when active, extends read or write timing to interface with slower external memory or I/O. WAIT is sampled at the end of T ₂ , if active processor enters a wait state T _W and remains in that state as long as WAIT is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	WR	(Tri-State Output, active low) WR, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. WR goes to the high impedance state during HALT, HOLD, or RESET.
17	RD	(Tri-State Output, active low) RD is used as a strobe to gate data from external devices onto the data bus. RD goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC ₀ -PC ₇	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	SCK	(Input/Output) SCK provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	RESET	(Input, active low) RESET initializes the μPD7801.
30	X ₂	(Output) Oscillator output.
31	X ₁	(Input) Clock Input
33-40	PA ₀ -PA ₇	(Output) 8-bit output port with latch capability.
41-48	PB ₀ -PB ₇	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION **Memory Map**

The μPD7802 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-6144) and RAM (65, 471-65, 535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7802 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



I/O PORTS

FUNCTIONAL DESCRIPTION (CONT.)

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_n = 0$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC ₀	Output	Input
PC ₁	Output	Input
PC ₂	\overline{SCS} Input	Input
PC ₃	SAK Output	Output
PC ₄	To Output	Output
PC ₅	IO/\overline{M} Output	Output
PC ₆	HLDA Output	Output
PC ₇	HOLD Input	Input

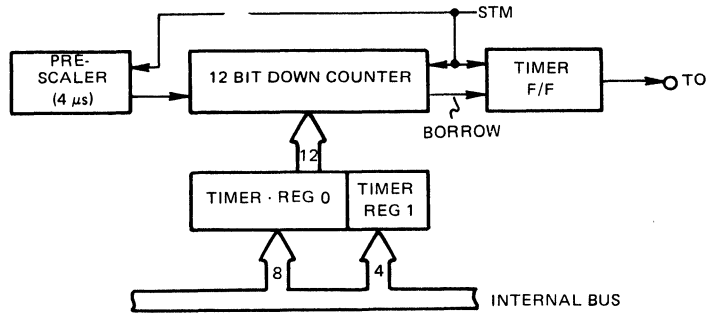
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus — the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus — the PEN instruction sets this mode which allows for memory expansion of an additional 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port — the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE₈₋₁₅ and PE₀₋₇, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



TIMER BLOCK DIAGRAM

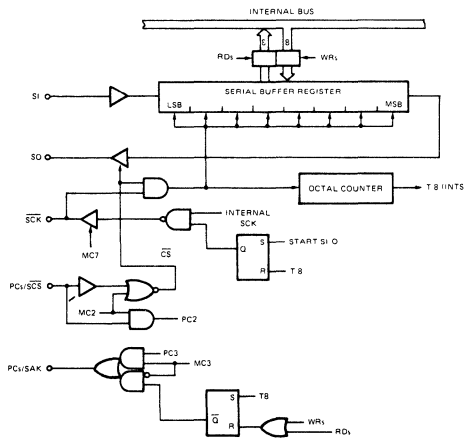
A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 ms in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (TO) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.



SERIAL PORT OPERATION



SERIAL PORT BLOCK DIAGRAM

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7802 to serially interface with external devices.

Serial Transfers are synchronized with either the internal clock or an external clock input (**SCK**). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external **SCK**) is enabled when the Serial Chip Select Signal (**SCS**) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

INTERRUPT STRUCTURE

The μPD7802 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and a non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

FUNCTIONAL DESCRIPTION
(CONT.)

RESET (Reset)

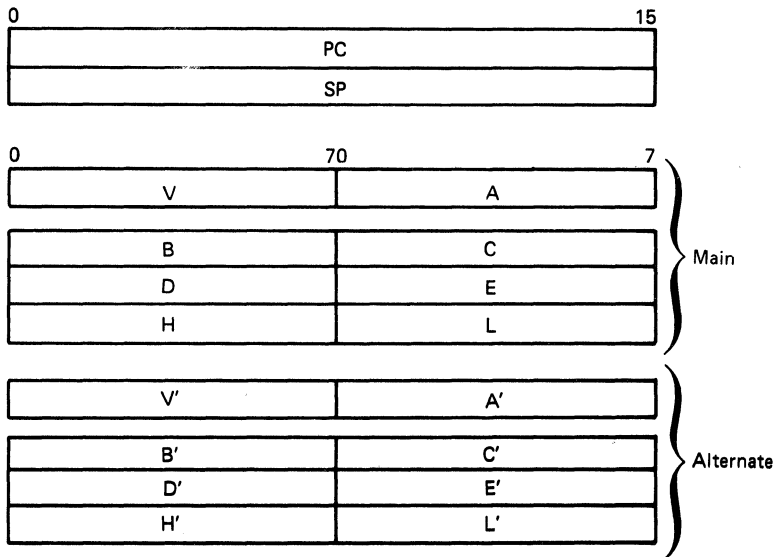
An active low-signal on this input for more than 4 μs forces the μPD7802 into a Reset condition. RESET affects the following internal functions:

- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag is reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus (PE₀₋₁₅), Data Bus (DB₀₋₇), \overline{RD} , and \overline{WR} go to a high impedance state.

Once the RESET input goes high, the program is started at location 0000_H.

REGISTERS

The μPD7802 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L; Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.



μPD7802

FUNCTIONAL DESCRIPTION (CONT.)

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7802 and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000H.

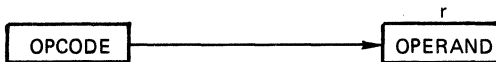
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

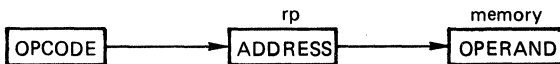
ADDRESS MODES

Register Addressing



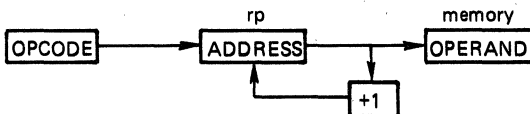
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



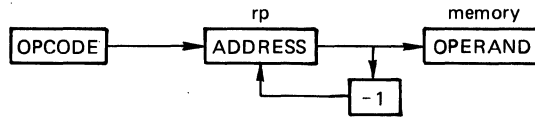
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

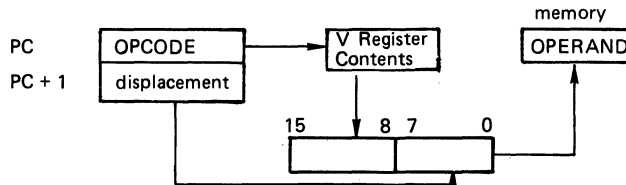


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

ADDRESS MODES (CONT.) Auto-Decrement Addressing

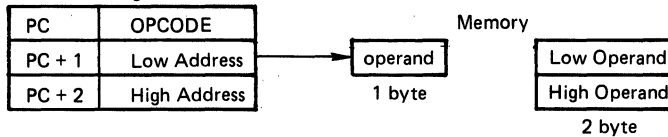


Working Register Addressing



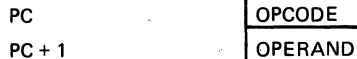
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing



Immediate Extended Addressing



Operand Description

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB, PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D-, H-
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

- Notes:
1. When special register operands sr, sr1, sr2 are used; PA=Port A, PB=Port B, PC=Port C, MK=Mask Register, MB=Mode B Register, MC=Mode C Register, TM0=Timer Register 0, TM1=Timer Register 1, S=Serial Register.
 2. When register pair operands rp, rp1 are used; SP=Stack Pointer, B=BC, D=DE, H=HL, V=VA.
 3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/ auto-decrement addressing modes.
B=(BC), D=(DE), H=(HL)
D+=(DE)⁺, H+=(HL)⁺, D-=(DE)⁻, H-=(HL)⁻.
 4. When the interrupt operand f is used; F0=INTF0, F1=INTF1, F2=INTF2, FT=INTFT, FS=INTFS.

INSTRUCTION GROUPS

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V, A			
BLOCK		1	13 (C+1)	(DE) ⁺ ← (HL) ⁺ , C ← C - 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP _L , (word + 1) ← SP _H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP _L ← (word), SP _H ← (word + 1)			
PUSH	rp1	2	17	(SP - 1) ← rp1 _H , (SP - 2) ← rp1 _L			
POP	rp1	2	15	rp1 _L ← (SP) rp1 _H ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			



INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
ARITHMETIC							
ADD	A, r	2	8	$A \leftarrow A + r$		‡	‡
ADD	r, A	2	8	$r \leftarrow r + A$		‡	‡
ADDX	rpa	2	11	$A \leftarrow A + (rpa)$		‡	‡
ADC	A, r	2	8	$A \leftarrow A + r + CY$		‡	‡
ADC	r, A	2	8	$r \leftarrow r + A + CY$		‡	‡
ADCX	rpa	2	11	$A \leftarrow A + (rpa) + CY$		‡	‡
SUB	A, r	2	8	$A \leftarrow A - r$		‡	‡
SUB	r, A	2	8	$r \leftarrow r - A$		‡	‡
SUBX	rpa	2	11	$A \leftarrow A - (rpa)$		‡	‡
SBB	A, r	2	8	$A \leftarrow A - r - CY$		‡	‡
SBB	r, A	2	8	$r \leftarrow r - A - CY$		‡	‡
SBBX	rpa	2	11	$A \leftarrow A - (rpa) - CY$		‡	‡
ADDNC	A, r	2	8	$A \leftarrow A + r$	No Carry	‡	‡
ADDNC	r, A	2	8	$r \leftarrow r + A$	No Carry	‡	‡
ADDNCX	rpa	2	11	$A \leftarrow A + (rpa)$	No Carry	‡	‡
SUBNB	A, r	2	8	$A \leftarrow A - r$	No Borrow	‡	‡
SUBNB	r, A	2	8	$r \leftarrow r - A$	No Borrow	‡	‡
SUBNBX	rpa	2	11	$A \leftarrow A - (rpa)$	No Borrow	‡	‡
LOGICAL							
ANA	A, r	2	8	$A \leftarrow A \wedge r$			‡
ANA	r, A	2	8	$r \leftarrow r \wedge A$			‡
ANAX	rpa	2	11	$A \leftarrow A \wedge (rpa)$			‡
ORA	A, r	2	8	$A \leftarrow A \vee r$			‡
ORA	r, A	2	8	$r \leftarrow r \vee A$			‡
ORAX	rpa	2	11	$A \leftarrow A \vee (rpa)$			‡
XRA	A, r	2	8	$A \leftarrow A \nabla r$			‡
XRA	r, A	2	8	$A \leftarrow r \nabla A$			‡
XRAX	rpa	2	11	$A \leftarrow A \nabla (rpa)$			‡
GTA	A, r	2	8	$A \leftarrow r - 1$	No Borrow	‡	‡

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	$A - (rpa) - 1$	No Borrow	‡	‡
LTA	A, r	2	8	$A - r$	Borrow	‡	‡
LTA	r, A	2	8	$r - A$	Borrow	‡	‡
LTAX	rpa	2	11	$A - (rpa)$	Borrow	‡	‡
ONA	A, r	2	8	$A \wedge r$	No Zero		‡
ONAX	rpa	2	11	$A \wedge (rpa)$	No Zero		‡
OFFA	A, r	2	8	$A \wedge r$	Zero		‡
OFFAX	rpa	2	11	$A \wedge (rpa)$	Zero		‡
NEA	A, r	2	8	$A - r$	No Zero	‡	‡
NEA	r, A	2	8	$r - A$	No Zero	‡	‡
NEAX	rpa	2	11	$A - (rpa)$	No Zero	‡	‡
EQA	A, r	2	8	$A - r$	Zero	‡	‡
EQA	r, A	2	8	$r - A$	Zero	‡	‡
EQAX	rpa	2	11	$A - (rpa)$	Zero	‡	‡
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	$A \leftarrow A \vee \text{byte}$			‡
ADINC	A, byte	2	7	$A \leftarrow A + \text{byte}$	No Carry	‡	‡
SUINB	A, byte	2	7	$A \leftarrow A - \text{byte}$	No Borrow	‡	‡
ADI	A, byte	2	7	$A \leftarrow A + \text{byte}$			‡
ACI	A, byte	2	7	$A \leftarrow A + \text{byte} + \text{CY}$			‡
SUI	A, byte	2	7	$A \leftarrow A - \text{byte}$			‡
SBI	A, byte	2	7	$A \leftarrow A - \text{byte} - \text{CY}$			‡
ANI	A, byte	2	7	$A \leftarrow A \wedge \text{byte}$			‡
ORI	A, byte	2	7	$A \leftarrow A \vee \text{byte}$			‡
GTI	A, byte	2	7	$A - \text{byte} - 1$	No Borrow	‡	‡
LTI	A, byte	2	7	$A - \text{byte}$	Borrow	‡	‡
ONI	A, byte	2	7	$A \wedge \text{byte}$	No Zero		‡
OFFI	A, byte	2	7	$A \wedge \text{byte}$	Zero		‡
NEI	A, byte	2	7	$A - \text{byte}$	No Zero	‡	‡
EQI	A, byte	2	7	$A - \text{byte}$	Zero	‡	‡

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	$r \leftarrow r \vee \text{byte}$			‡
ADINC	r, byte	3	11	$r \leftarrow r + \text{byte}$	No Carry	‡	‡
SUINB	r, byte	3	11	$r \leftarrow r - \text{byte}$	No Borrow	‡	‡
ADI	r, byte	3	11	$r \leftarrow r + \text{byte}$		‡	‡
ACI	r, byte	3	11	$r \leftarrow r + \text{byte} + \text{CY}$		‡	‡
SUI	r, byte	3	11	$r \leftarrow r - \text{byte}$		‡	‡
SBI	r, byte	3	11	$r \leftarrow r - \text{byte} - \text{CY}$		‡	‡
ANI	r, byte	3	11	$r \leftarrow r \wedge \text{byte}$		‡	‡
ORJ	r, byte	3	11	$r \leftarrow r \vee \text{byte}$			‡
GTI	r, byte	3	11	$r - \text{byte} - 1$	No Borrow	‡	‡
LTI	r, byte	3	11	$r - \text{byte}$	Borrow	‡	‡
ONI	r, byte	3	11	$r \wedge \text{byte}$	No Zero		‡
OFFI	r, byte	3	11	$r \wedge \text{byte}$	Zero		‡
NEI	r, byte	3	11	$r - \text{byte}$	No Zero	‡	‡
EQI	r, byte	3	11	$r - \text{byte}$	Zero	‡	‡
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	$sr2 \leftarrow sr2 \vee \text{byte}$			‡
ADINC	sr2, byte	3	17	$sr2 \leftarrow sr2 + \text{byte}$	No Carry	‡	‡
SUINB	sr2, byte	3	17	$sr2 \leftarrow sr2 - \text{byte}$	No Borrow	‡	‡
ADI	sr2, byte	3	17	$sr2 \leftarrow sr2 + \text{byte}$		‡	‡
ACI	sr2, byte	3	17	$sr2 \leftarrow sr2 + \text{byte} + \text{CY}$		‡	‡
SUI	sr2, byte	3	17	$sr2 \leftarrow sr2 - \text{byte}$		‡	‡
SBI	sr2, byte	3	17	$sr2 \leftarrow sr2 - \text{byte} - \text{CY}$		‡	‡
ANI	sr2, byte	3	17	$sr2 \leftarrow sr2 \wedge \text{byte}$			‡
ORI	sr2, byte	3	17	$sr2 \leftarrow sr2 \vee \text{byte}$			‡
GTI	sr2, byte	3	14	$sr2 - \text{byte} - 1$	No Borrow	‡	‡
LTI	sr2, byte	3	14	$sr2 - \text{byte}$	Borrow	‡	‡
ONI	sr2, byte	3	14	$sr2 \wedge \text{byte}$	No Zero		‡

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		‡
NEI	sr2, byte	3	14	sr2 - byte	No Zero	‡	‡
EQI	sr2, byte	3	14	sr2 - byte	Zero	‡	‡
WORKING REGISTER							
XRAW	wa	3	14	A ← A ∨ (V, wa)			‡
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	‡	‡
SUBNBW	wa	3	14	A ← A - (V, wa)	No Borrow	‡	‡
ADDW	wa	3	14	A ← A + (V, wa)		‡	‡
ADCW	wa	3	14	A ← A + (V, wa) + CY		‡	‡
SUBW	wa	3	14	A ← A - (V, wa)		‡	‡
SBBW	wa	3	14	A ← A - (V, wa) - CW		‡	‡
ANAW	wa	3	14	A ← A ∧ (V, wa)			‡
ORAW	wa	3	14	A ← A ∨ (V, wa)			‡
GTAW	wa	3	14	A - (V, wa) - 1	No Borrow	‡	‡
LTAW	wa	3	14	A - (V, wa)	Borrow	‡	‡
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		‡
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		‡
NEAW	wa	3	14	A - (V, wa)	No Zero	‡	‡
EQAW	wa	3	14	A - (V, wa)	Zero	‡	‡
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			‡
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			‡
GTIW	wa, byte	3	13	(V, wa) - byte - 1	No Borrow	‡	‡
LTIW	wa, byte	3	13	(V, wa) - byte	Borrow	‡	‡
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		‡
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		‡
NEIW	wa, byte	3	13	(V, wa) - byte	No Zero	‡	‡
EQIW	wa, byte	3	13	(V, wa) - byte	Zero	‡	‡
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		‡
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		‡



INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	$r2 \leftarrow r2 - 1$	Borrow		↑
DCRW	wa	2	13	$(V, wa) \leftarrow (V, wa) - 1$	Borrow		↑
INX	rp	1	7	$rp \leftarrow rp + 1$			
DCX	rp	1	7	$rp \leftarrow rp - 1$			
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	$A_m + 1 \leftarrow A_m, A_0 \leftarrow CY, CY \leftarrow A_7$			↑
RCL		2	8	$C_m + 1 \leftarrow C_m, C_0 \leftarrow CY, CY \leftarrow C_7$			↑
RAR		2	8	$A_m - 1 \leftarrow A_m, A_7 \leftarrow CY, CY \leftarrow A_0$			↑
RCR		2	8	$C_m - 1 \leftarrow C_m, C_7 \leftarrow CY, CY \leftarrow C_0$			↑
SHAL		2	8	$A_m + 1 \leftarrow A_m, A_0 \leftarrow 0, CY \leftarrow A_7$			↑
SHCL		2	8	$C_m + 1 \leftarrow C_m, C_0 \leftarrow 0, CY \leftarrow C_7$			↑
SHAR		2	8	$A_m - 1 \leftarrow A_m, A_7 \leftarrow 0, CY \leftarrow A_0$			↑
SHCR		2	8	$C_m - 1 \leftarrow C_m, C_7 \leftarrow 0, CY \leftarrow C_0$			↑
JUMP							
JMP	word	3	10	$PC \leftarrow \text{word}$			
JB		1	4	$PC_H \leftarrow B, PC_L \leftarrow C$			
JR	word	1	13	$PC \leftarrow PC + 1 + \text{jdisp1}$			
JRE	word	2	13	$PC \leftarrow PC + 2 + \text{jdisp}$			
CALL							
CALL	word	3	16	$(SP - 1) \leftarrow (PC - 3)_H, (SP - 2) \leftarrow (PC - 3)_L, PC \leftarrow \text{word}$			
CALB		1	13	$(SP - 1) \leftarrow (PC - 1)_H, (SP - 2) \leftarrow (PC - 1)_L, PC_H \leftarrow B, PC_L \leftarrow C$			
CALF	word	2	16	$(SP - 1) \leftarrow (PC - 2)_H, (SP - 2) \leftarrow (PC - 2)_L, PC_{15 \sim 11} \leftarrow 00001, PC_{10 \sim 0} \leftarrow \text{fa}$			
CALT	word	1	19	$(SP - 1) \leftarrow (PC - 1)_H, (SP - 2) \leftarrow (PC - 1)_L, PC_L \leftarrow (128 - 2\text{ta}), PC_H \leftarrow (129 + 2\text{ta})$			
SOFTI		1	19	$(SP - 1) \leftarrow PSW, SP - 2, (SP - 3) \leftarrow PC, PC \leftarrow 0060_H, SIRQ \leftarrow 1$			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS	
						CY	Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $SP \leftarrow SP - 2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1),$ $SP \leftarrow SP + 2, PC \leftarrow PC + n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1$		
SKC		2	8	Skip if Carry	$CY = 1$		
SKNC		2	8	Skip if No Carry	$CY = 0$		
SKZ		2	8	Skip if Zero	$Z = 1$		
SKNZ		2	8	Skip if No Zero	$Z = 0$		
SKIT	f	2	8	Skip if $INT X = 1$, then reset $INT X$	$f = 1$		
SKNIT	f	2	8	Skip if No $INT X$ otherwise reset $INT X$	$f = 0$		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow \text{byte}$ $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow \text{byte}$ $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

Program Status Word (PSW) Operation

OPERATION					D6	D5	D4	D3	D2	D0	
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD	ADDW	ADDX	ADI			‡	0	‡	0	0	‡
ADC	ADCW	ADCX	ACI								
SUB	SUBW	SUBX	SUI								
SBB	SBBW	SBBX	SBI								
ANA	ANAW	ANAX	ANI	ANIW		‡	0	•	0	0	•
ORA	ORAW	ORAX	ORI	ORIW							
XRA	XRAW	XRAX	XRI								
ADDNC	ADDNCW	ADDNCX	ADINC			‡	‡	‡	0	0	‡
SUBNB	SUBNBW	SUBNBX	SUINB								
GTA	GTAW	GTAX	GTI	GTIW							
LTA	LTAW	LTAX	LTI	LTIW							
ONAW	ONAW	ONAX	ONI	ONIW		‡	‡	•	0	0	•
OFFA	OFFAW	OFFAX	OFFI	OFFIW							
NEAW	NEAW	NEAX	NEI	NEIW		‡	‡	‡	0	0	‡
EQA	EQAW	EQAX	EQI	EQIW							
INRW	INRW					‡	‡	‡	0	0	•
DCR	DCRW										
DAA						‡	0	‡	0	0	‡
RAL, RAR, RCL, RCR						•	0	•	0	0	‡
SHAL, SHAR, SHCL, SHCR											
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
			BIT								
			SKC								
			SKNC								
			SKZ			•	‡	•	0	0	•
			SKNZ								
			SKIT								
			SKNIT								
			RETS			•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

- ‡ Flag affected according to result of operation
- 1 Flag set
- 0 Flag reset
- Flag not affected

ABSOLUTE MAXIMUM RATINGS*	Operating Temperature	-10°C to +70°C
	Storage Temperature	-65°C to +125°C
	Voltage On Any Pin	-0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS -10 to +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V _{IL}	0		0.8	V	
Input High Voltage	V _{IH1}	2.0		V _{CC}	V	Except \overline{SCK} , X1
	V _{IH2}	3.8		V _{CC}	V	\overline{SCK} , X1
Output Low Voltage	V _{OL}			0.45	V	I _{OL} = 2.0 mA
Output High Voltage	V _{OH1}	2.4			V	I _{OH} = -100 μA
	V _{OH2}	2.0			V	I _{OH} = -500 μA
Low Level Input Leakage Current	I _{LIL}			-10	μA	V _{IN} = 0V
High Level Input Leakage Current	I _{LIH}			10	μA	V _{IN} = V _{CC}
Low Level Output Leakage Current	I _{LOL}			-10	μA	V _{OUT} = 0.45V
High Level Output Leakage Current	I _{LOH}			10	μA	V _{OUT} = V _{CC}
V _{CC} Power Supply Current	I _{CC}		110	200	mA	



CAPACITANCE T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C _I			10	pF	f _c = 1 MHz All pins not under test at 0V
Output Capacitance	C _O			20	pF	
Input/Output Capacitance	C _{IO}			20	pF	

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
X1 Input Cycle Time	t _{CYX}	227	1000	ns	
X1 Input Low Level Width	t _{XXL}	106		ns	
X1 Input High Level Width	t _{XXH}	106		ns	
φ _{OUT} Cycle Time	t _{CYφ}	454	2000	ns	
φ _{OUT} Low Level Width	t _{φL}	150		ns	
φ _{OUT} High Level Width	t _{φH}	150		ns	
φ _{OUT} Rise/Fall Time	t _{r,tf}		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
RD L.E. → φ _{OUT} L.E.	t _{Rφ}	100		ns	t _{CYφ} = 500 ns
Address (PE ₀₋₁₅) → Data Input	t _{AD1}		550 + 500 x N	ns	
RD T.E. → Address	t _{RA}	200(T3); 700(T4)		ns	
RD L.E. → Data Input	t _{RD}		350 + 500 x N	ns	
RD T.E. → Data Hold Time	t _{RDH}	0		ns	
RD Low Level Width	t _{RR}	850 + 500 x N		ns	
RD L.E. → WAIT L.E.	t _{RWT}		450	ns	
Address (PE ₀₋₁₅) → WAIT L.E.	t _{AWT1}		650	ns	
WAIT Set Up Time (Referenced from φ _{OUT} L.E.)	t _{WTS}	290		ns	
WAIT Hold Time (Referenced from φ _{OUT} L.E.)	t _{WTH}	0		ns	
M1 → RD L.E.	t _{MR}	200		ns	
RD T.E. → M1	t _{RM}	200		ns	
IO/M → RD L.E.	t _{IR}	200		ns	
RD T.E. → IO/M	t _{RI}	200		ns	
φ _{OUT} L.E. → WR L.E.	t _{φW}	40	125	ns	
Address (PE ₀₋₁₅) → φ _{OUT} T.E.	t _{Aφ}	100	300	ns	
Address (PE ₀₋₁₅) → Data Output	t _{AD2}	450		ns	
Data Output → WR T.E.	t _{DW}	600 + 500 x N		ns	
WR T.E. → Data Stabilization Time	t _{WD}	150		ns	
Address (PE ₀₋₁₅) → WR L.E.	t _{AW}	400		ns	
WR T.E. → Address Stabilization Time	t _{WA}	200		ns	
WR Low Level Width	t _{WW}	600 + 500 x N		ns	
IO/M → WR L.E.	t _{IW}	500		ns	
WR T.E. → IO/M	t _{WI}	250		ns	

SERIAL I/O OPERATION

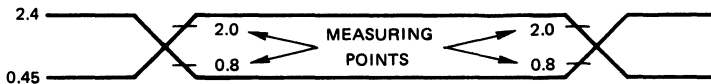
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{\text{SCK}}$ Cycle Time	t_{CYK}	800		ns	$\overline{\text{SCK}}$ Input
		900	4000	ns	$\overline{\text{SCK}}$ Output
$\overline{\text{SCK}}$ Low Level Width	t_{KLL}	350		ns	$\overline{\text{SCK}}$ Input
		400		ns	$\overline{\text{SCK}}$ Output
$\overline{\text{SCK}}$ High Level Width	t_{KHH}	350		ns	$\overline{\text{SCK}}$ Input
		400		ns	$\overline{\text{SCK}}$ Output
SI Set-Up Time (referenced from $\overline{\text{SCK}}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{\text{SCK}}$ T.E.)	t_{SIH}	260		ns	
$\overline{\text{SCK}}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{\text{SCS}}$ High → $\overline{\text{SCK}}$ L.E.	t_{CSK}	100		ns	
$\overline{\text{SCK}}$ T.E. → $\overline{\text{SCS}}$ Low	t_{KCS}	100		ns	
$\overline{\text{SCK}}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from $\emptyset\text{OUT}$ L.E.)	t_{HDS_1}	200		ns	$t_{\text{CY}\phi} = 500 \text{ ns}$
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from $\emptyset\text{OUT}$ L.E.)	t_{HDH}	0		ns	
$\emptyset\text{OUT}$ L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	-150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

- ① AC Signal waveform (unless otherwise specified)



- ② Output Timing is measured with 1 TTL + 200 pF measuring points are $V_{\text{OH}} = 2.0\text{V}$
 $V_{\text{OL}} = 0.8\text{V}$
- ③ L.E. = Leading Edge, T.E. = Trailing Edge

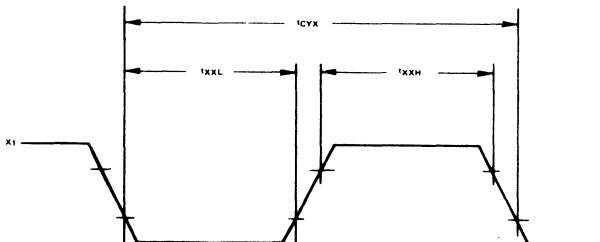
t_{CYφ} DEPENDENT AC PARAMETERS

**AC CHARACTERISTICS
(CONT.)**

PARAMETER	EQUATION	MIN/MAX	UNIT
t _{Rφ}	(1/5) T	MIN	ns
t _{AD1}	(3/2 + N) T - 200	MAX	ns
t _{RA} (T ₃)	(1/2) T - 50	MIN	ns
t _{RA} (T ₄)	(3/2) T - 50	MIN	ns
t _{RD}	(1 + N) T - 150	MAX	ns
t _{RR}	(2 + N) T - 150	MIN	ns
t _{RWT}	(3/2) T - 300	MAX	ns
t _{AWT1}	(2) T - 350	MAX	ns
t _{MR}	(1/2) T - 50	MIN	ns
t _{RM}	(1/2) T - 50	MIN	ns
t _{IR}	(1/2) T - 50	MIN	ns
t _{RI}	(1/2) T - 50	MIN	ns
t _{φW}	(1/4) T	MAX	ns
t _{Aφ}	(1/5) T	MIN	ns
t _{AD2}	T - 50	MIN	ns
t _{DW}	(3/2 + N) T - 150	MIN	ns
t _{WD}	(1/2) T - 100	MIN	ns
t _{AW}	T - 100	MIN	ns
t _{WA}	(1/2) T - 50	MIN	ns
t _{WW}	(3/2 + N) T - 150	MIN	ns
t _{IW}	T	MIN	ns
t _{WI}	(1/2) T	MIN	ns
t _{HABE}	(1/2) T - 150	MAX	ns

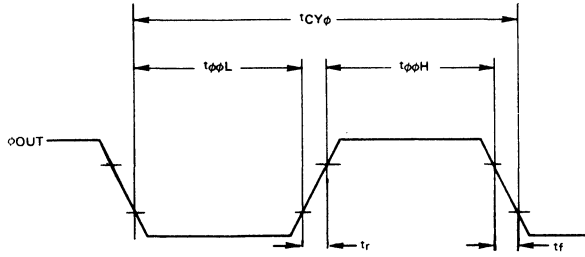
- Notes: ① N = Number of Wait States
 ② T = t_{CYφ}
 ③ Only above parameters are t_{CYφ} dependent
 ④ When a crystal frequency other than 4 MHz is used (t_{CYφ} = 500 ns) the above equations can be used to calculate AC parameter values.

CLOCK TIMING

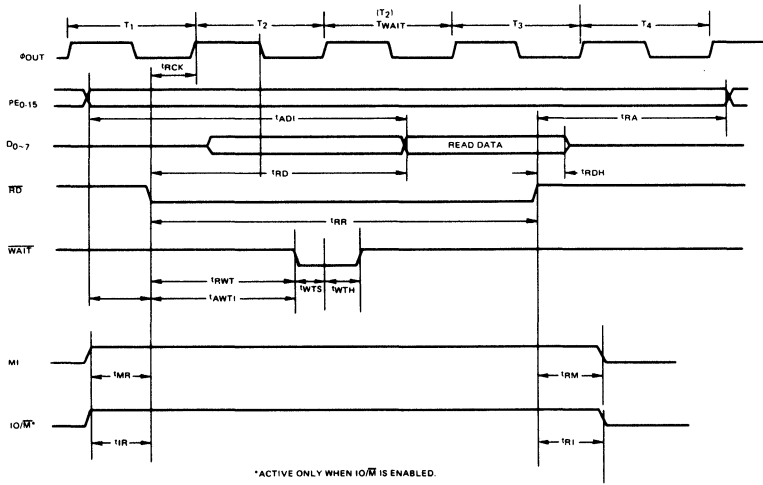


TIMING WAVEFORMS

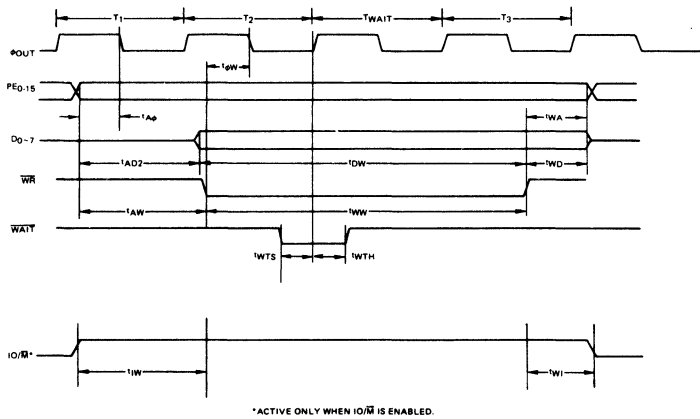
**TIMING WAVEFORMS
(CONT.)**



READ OPERATION

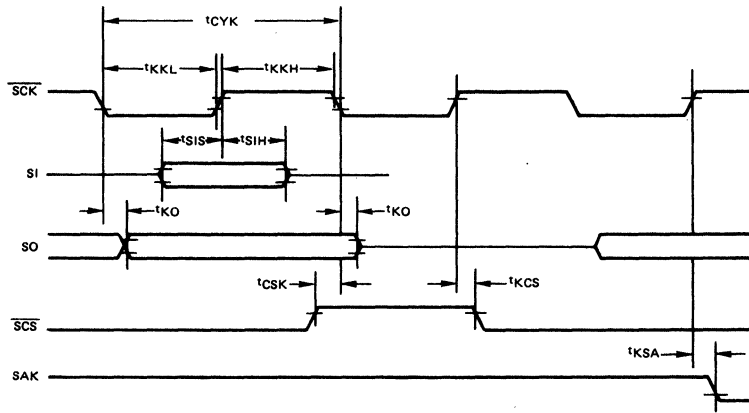


WRITE OPERATION

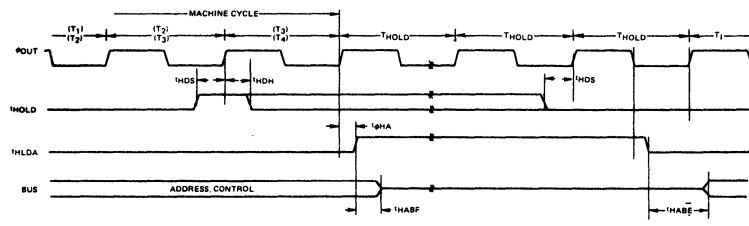


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SERIAL I/O OPERATION

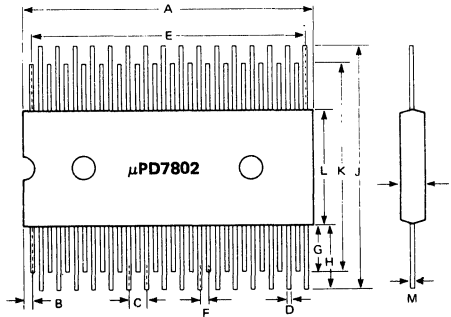


HOLD OPERATION



PACKAGE INFORMATION

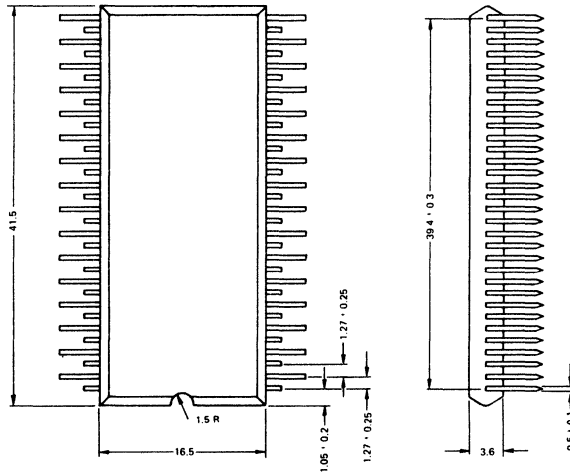
STRAIGHT LEADS



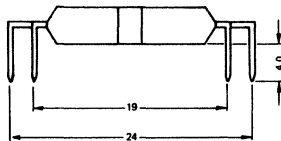
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	38.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit:mm)



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