

8-BIT SINGLE-CHIP MICROCONTROLLER**DESCRIPTION**

The μ PD780232 is a member of the μ PD780232 Subseries in the 78K/0 Series.

The μ PD780232 Subseries consists of products that incorporate a VFD controller/driver for panel control.

A flash memory version, the μ PD78F0233, that can operate within the same power supply voltage range as the mask ROM version, and various development tools are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD780232 Subseries User's Manual: U13364E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- I/O ports: 40
- Internal ROM and RAM
 - Internal ROM: 16 KB
 - Internal high-speed RAM: 768 bytes
 - Internal buffer RAM: 32 bytes
 - VFD display RAM: 112 bytes
- Minimum instruction execution time can be changed from high speed (0.4 μ s) to low speed (6.4 μ s)
- VFD controller/driver: 53 display outputs (Universal grid supported)
- 8-bit resolution A/D converter: 4 channels
- Serial interface: 2 channels
- Timer: 4 channels
- Power supply voltage: $V_{DD} = 4.5$ to 5.5 V

APPLICATIONS

Monolithic mini components, separated mini components, tuners, cassette tape decks, CD/MD players, audio amplifiers, etc.

ORDERING INFORMATION

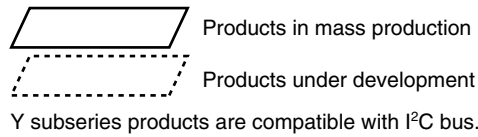
| Part Number | Package |
|--------------------------|------------------------------|
| μ PD780232GC-xxx-8BT | 80-pin plastic QFP (14 × 14) |

Remark xxx indicates ROM code suffix.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



| | | | |
|--------------------------------|----------------|---|--|
| 78K/0 Series | Control | | |
| | 100-pin | μPD78075B | EMI-noise reduced version of the μPD78078 |
| | 100-pin | μPD78078 | μPD78054 with added timer and enhanced external interface |
| | | μPD78078Y | |
| | 100-pin | μPD78070A | ROMless version of the μPD78078 |
| | 100-pin | μPD780018AY | μPD78078Y with enhanced serial I/O and limited function |
| | 80-pin | μPD780058 | μPD78054 with enhanced serial I/O |
| | | μPD780058Y | |
| | 80-pin | μPD78058F | EMI-noise reduced version of the μPD78054 |
| | 80-pin | μPD78054 | μPD78018F with added UART and D/A converter and enhanced I/O |
| | | μPD78054Y | |
| | 80-pin | μPD780065 | μPD780024A with expanded RAM capacity |
| | 64-pin | μPD780078 | μPD780034A with added timer and enhanced serial I/O |
| | | μPD780078Y | |
| | 64-pin | μPD780034A | μPD780024A with enhanced A/D converter |
| | 64-pin | μPD780024A | μPD78018F with enhanced serial I/O |
| | | μPD780024AY | |
| | 64-pin | μPD78014H | EMI-noise reduced version of the μPD78018F |
| | 64-pin | μPD78018F | Basic subseries for control |
| | | μPD78018FY | |
| 42-/44-pin | μPD78083 | On-chip UART, capable of operating at low voltage (1.8 V) | |
| Inverter control | | | |
| 64-pin | μPD780988 | On-chip inverter controller and UART. EMI-noise reduced. | |
| VFD drive | | | |
| 100-pin | μPD780208 | μPD78044F with enhanced I/O and VFD C/D. Display output total: 53 | |
| 80-pin | μPD780232 | | |
| 80-pin | μPD78044H | For panel control. On-chip VFD C/D. Display output total: 53 | |
| 80-pin | μPD78044F | μPD78044F with added N-ch open-drain I/O. Display output total: 34 | |
| LCD drive | | | |
| 120-pin | μPD780338 | μPD780308 with enhanced display capacity and timer. Segment signal output: 40 pins max. | |
| 120-pin | μPD780328 | | |
| 120-pin | μPD780318 | | |
| 100-pin | μPD780308 | μPD78064 with enhanced SIO, and expanded ROM, RAM capacity | |
| | μPD780308Y | | |
| 100-pin | μPD78064B | EMI-noise reduced version of the μPD78064 | |
| 100-pin | μPD78064 | Basic subseries for LCD drive, on-chip UART | |
| | μPD78064Y | | |
| Bus interface supported | | | |
| 100-pin | μPD780948 | On-chip DCAN controller | |
| 80-pin | μPD78098B | μPD78054 with added IEBus™ controller. EMI-noise reduced. | |
| 80-pin | μPD780701Y | | |
| 80-pin | μPD780833Y | On-chip controller compliant with J1850 (Class 2) | |
| Meter control | | | |
| 100-pin | μPD780958 | For industrial meter control | |
| 80-pin | μPD780852 | On-chip automobile meter controller/driver | |
| 80-pin | μPD780824 | For automobile meter driver. On-chip DCAN controller | |

Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

| Subseries Name | Function | ROM Capacity | Timer | | | | 8-Bit A/D | 10-Bit A/D | 8-Bit D/A | Serial Interface | I/O | V _{DD} MIN. Value | External Expansion | |
|-------------------------|-------------|--------------|-------|-------------|-------|------|-----------|------------|-----------|---------------------------------|-------------------|----------------------------|--------------------|------|
| | | | 8-Bit | 16-Bit | Watch | WDT | | | | | | | | |
| Control | μPD78075B | 32 K to 40 K | 4 ch | 1 ch | 1 ch | 1 ch | 8 ch | - | 2 ch | 3 ch (UART: 1 ch) | 88 | 1.8 V | √ | |
| | μPD78078 | 48 K to 60 K | | | | | | | | | 61 | 2.7 V | | |
| | μPD78070A | - | 2 ch | - | - | - | - | - | - | 3 ch (time-division UART: 1 ch) | 68 | 1.8 V | - | |
| | μPD780058 | 24 K to 60 K | | | | | | | | | 69 | 2.7 V | | |
| | μPD78058F | 48 K to 60 K | - | - | - | - | - | - | - | 3 ch (UART: 1 ch) | 69 | 2.7 V | - | |
| | μPD78054 | 16 K to 60 K | | | | | | | | | 2.0 V | | | |
| | μPD780065 | 40 K to 48 K | 2 ch | - | - | - | - | - | - | - | 4 ch (UART: 1 ch) | 60 | 2.7 V | - |
| | μPD780078 | 48 K to 60 K | | | | | | | | | | 52 | 1.8 V | |
| | μPD780034A | 8 K to 32 K | 1 ch | - | - | - | 8 ch | - | - | - | 3 ch (UART: 1 ch) | 51 | - | - |
| | μPD780024A | 8 K to 32 K | | | | | | | | | | | | |
| | μPD78014H | 8 K to 32 K | - | - | - | - | - | - | - | - | 2 ch | 53 | - | - |
| | μPD78018F | 8 K to 60 K | | | | | | | | | | | | |
| μPD78083 | 8 K to 16 K | - | - | - | - | - | - | - | - | 1 ch (UART: 1 ch) | 33 | - | - | |
| Inverter control | μPD780988 | 16 K to 60 K | 3 ch | Note | - | 1 ch | - | 8 ch | - | 3 ch (UART: 2 ch) | 47 | 4.0 V | √ | |
| VFD drive | μPD780208 | 32 K to 60 K | 2 ch | 1 ch | 1 ch | 1 ch | 8 ch | - | - | 2 ch | 74 | 2.7 V | - | |
| | μPD780232 | 16 K to 24 K | | | | | 3 ch | | | | - | - | | 4 ch |
| | μPD78044H | 32 K to 48 K | 2 ch | 1 ch | 1 ch | - | 8 ch | - | - | 1 ch | 68 | 2.7 V | - | |
| | μPD78044F | 16 K to 40 K | | | | | | | | | 2 ch | | | |
| LCD drive | μPD780338 | 48 K to 60 K | 3 ch | 2 ch | 1 ch | 1 ch | - | 10 ch | 1 ch | 2 ch (UART: 1 ch) | 54 | 1.8 V | - | |
| | μPD780328 | | | | | | | | | | 62 | | | |
| | μPD780318 | | | | | | | | | | 70 | | | |
| | μPD780308 | 48 K to 60 K | 2 ch | 1 ch | - | - | 8 ch | - | - | 3 ch (time-division UART: 1 ch) | 57 | 2.0 V | - | |
| | μPD78064B | 32 K | | | | | | | | | 2 ch (UART: 1 ch) | | | |
| | μPD78064 | 16 K to 32 K | | | | | | | | | | | | |
| Bus interface supported | μPD780948 | 60 K | 2 ch | 2 ch | 1 ch | 1 ch | 8 ch | - | - | 3 ch (UART: 1 ch) | 79 | 4.0 V | √ | |
| | μPD78098B | 40 K to 60 K | | 1 ch | | | | | | | 2 ch | 69 | 2.7 V | - |
| Meter control | μPD780958 | 48 K to 60 K | 4 ch | 2 ch | - | 1 ch | - | - | - | 2 ch (UART: 1 ch) | 69 | 2.2 V | - | |
| Dash-board control | μPD780852 | 32 K to 40 K | 3 ch | 1 ch | 1 ch | 1 ch | 5 ch | - | - | 3 ch (UART: 1 ch) | 56 | 4.0 V | - | |
| | μPD780824 | 32 K to 60 K | | | | | | | | | 2 ch (UART: 1 ch) | | | 59 |

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

FUNCTION OVERVIEW

| Item | | Function |
|--|-----------------|--|
| Internal memory | ROM | 16 KB |
| | High-speed RAM | 768 bytes |
| | Buffer RAM | 32 bytes |
| | VFD display RAM | 112 bytes |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) |
| Minimum instruction execution time | | <ul style="list-style-type: none"> • On-chip minimum instruction execution time variable function • 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0 MHz operation with system clock) |
| Instruction set | | <ul style="list-style-type: none"> • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) |
| I/O ports (including alternate-function pins for VFD) | | Total: 40 <ul style="list-style-type: none"> • CMOS I/Os: 11 • P-ch open-drain I/Os: 13 • P-ch open-drain outputs: 16 |
| VFD controller/driver | | Total of display outputs: 53 <ul style="list-style-type: none"> • 15 mA display current: 20 • 5 mA display current: 33 |
| A/D converter | | <ul style="list-style-type: none"> • 8-bit resolution × 4 channels • Power supply voltage: AV_{DD} = 4.5 to 5.5 V |
| Serial interface | | <ul style="list-style-type: none"> • 3-wire serial mode (automatic transmit/receive function): 1 channel • 2-wire serial mode (transmit only): 1 channel |
| Timer | | <ul style="list-style-type: none"> • 8-bit remote control timer: 1 channel • 8-bit timer: 2 channels • Watchdog timer: 1 channel |
| Vectored interrupt sources | Maskable | Internal: 10, external: 2 |
| | Non-maskable | Internal: 1 |
| | Software | 1 |
| Power supply voltage | | V _{DD} = 4.5 to 5.5 V |
| Package | | 80-pin plastic QFP (14 × 14) |

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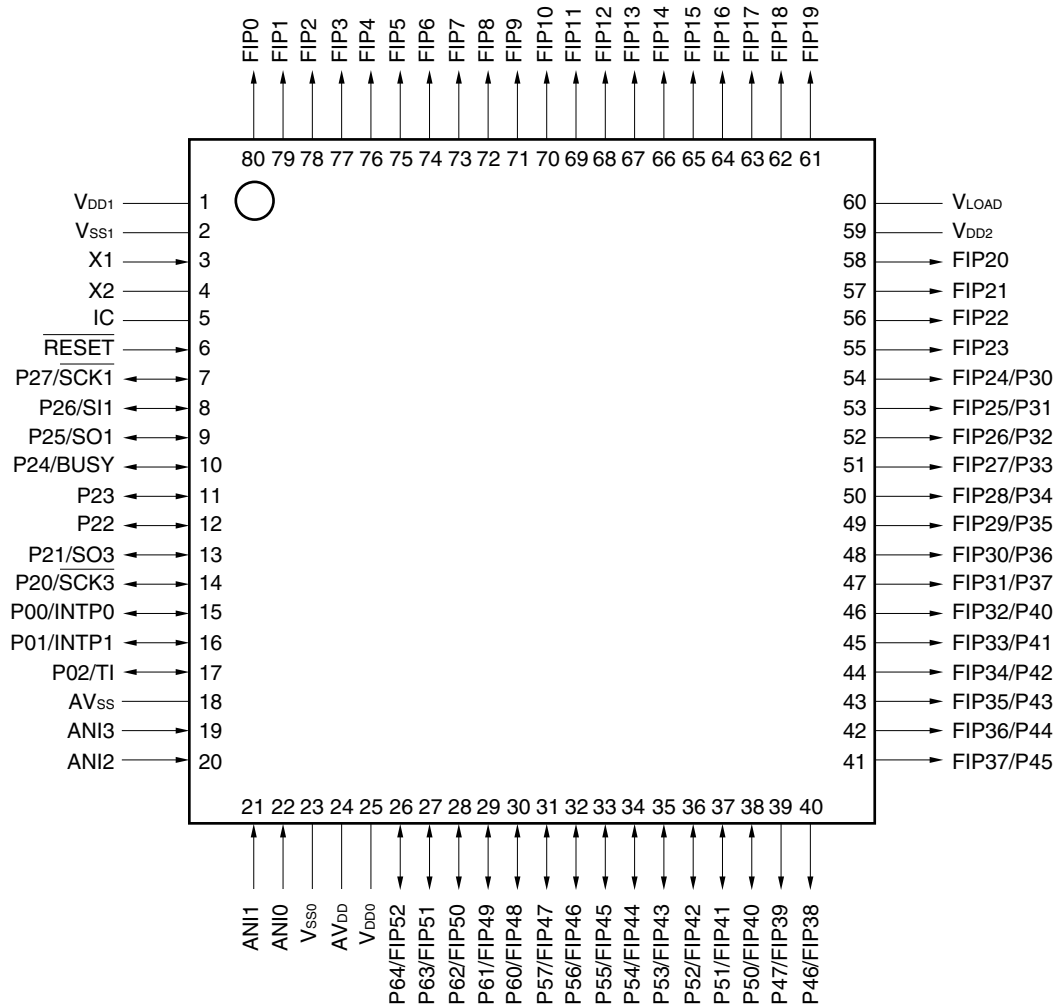
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1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14)
μPD780232GC-xxx-8BT

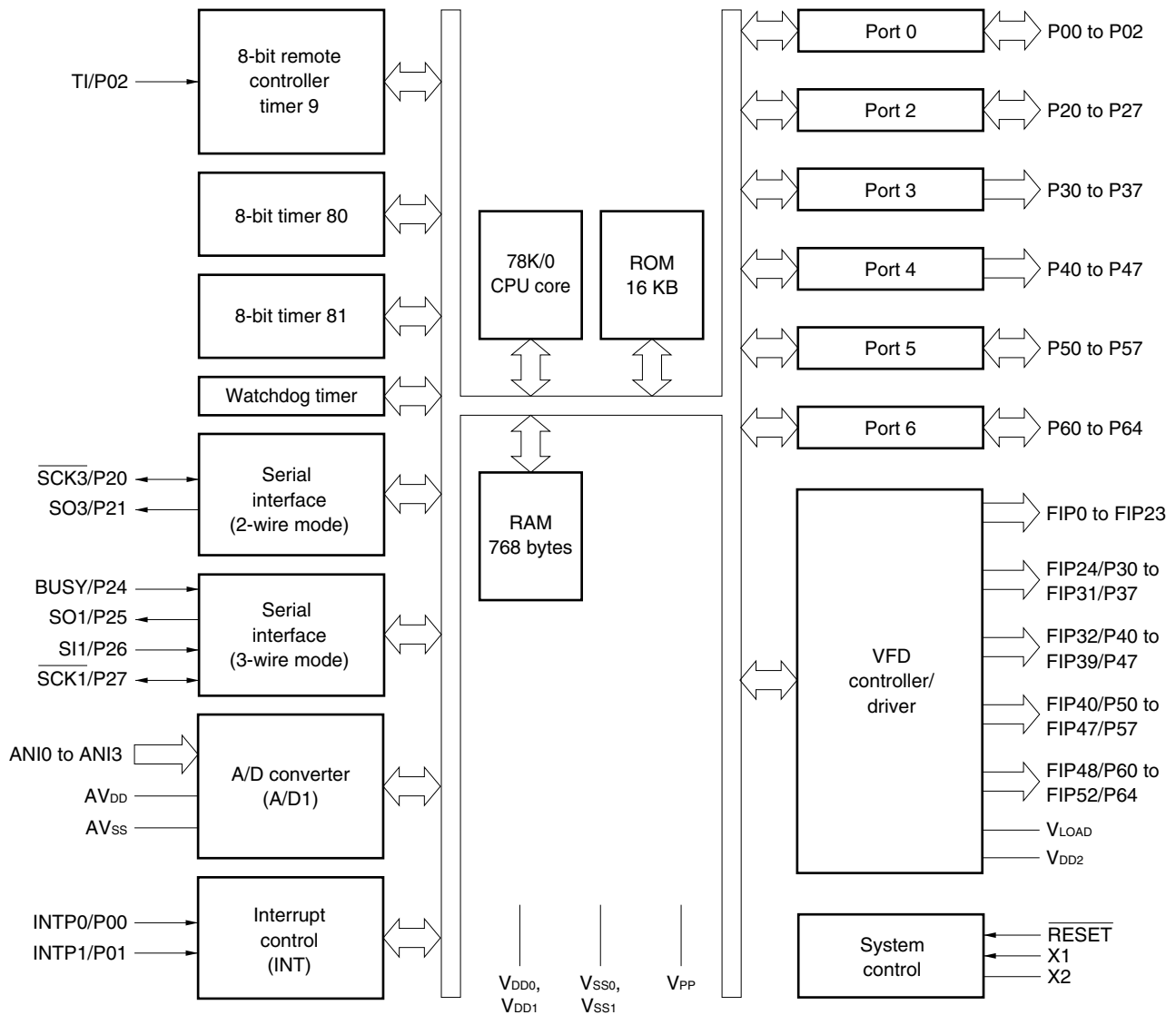


- Cautions**
1. Connect directly the IC (Internally Connected) pin to V_{SS1}.
 2. Connect the AV_{DD} pin to V_{DD1}.
 3. Connect the AV_{SS} pin to V_{SS1}.

Remark When the μPD780232 is used in application fields that require reduction of the noise from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

| | | | |
|--------------------|-----------------------------|--|-----------------------|
| ANI0 to ANI3: | Analog input | P50 to P57: | Port 5 |
| AV _{DD} : | Analog power supply | P60 to P64: | Port 6 |
| AV _{SS} : | Analog ground | $\overline{\text{RESET}}$: | Reset |
| BUSY: | Busy | $\overline{\text{SCK1}}, \overline{\text{SCK3}}$: | Serial clock |
| FIP0 to FIP52: | Fluorescent indicator panel | SI1: | Serial input |
| IC: | Internally connected | SO1, SO3: | Serial output |
| INTP0, INTP1 | External interrupt input | TI: | Timer input |
| P00 to P02: | Port 0 | V _{DD0} to V _{DD2} : | Power supply |
| P20 to P27: | Port 2 | V _{LOAD} : | Negative power supply |
| P30 to P37: | Port 3 | V _{SS0} , V _{SS1} : | Ground |
| P40 to P47: | Port 4 | X1, X2: | Crystal |

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

| Pin Name | I/O | Function | After Reset | Alternate Function |
|------------|--------|---|-------------|--------------------------|
| P00 | I/O | Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software. | Input | INTP0 |
| P01 | | | | INTP1 |
| P02 | | | | TI |
| P20 | I/O | Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software. | Input | $\overline{\text{SCK3}}$ |
| P21 | | | | SO3 |
| P22, P23 | | | | — |
| P24 | | | | BUSY |
| P25 | | | | SO1 |
| P26 | | | | SI1 |
| P27 | | | | $\overline{\text{SCK1}}$ |
| P30 to P37 | Output | Port 3. P-ch open-drain 8-bit high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by mask option. | Output | FIP24 to FIP31 |
| P40 to P47 | Output | Port 4. P-ch open-drain 8-bit high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by mask option. | Output | FIP32 to FIP39 |
| P50 to P57 | I/O | Port 5. P-ch open-drain 8-bit high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units). | Input | FIP40 to FIP47 |
| P60 to P64 | I/O | Port 6. P-ch open-drain 5-bit high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units). | Input | FIP48 to FIP52 |

3.2 Non-Port Pins

| Pin Name | I/O | Function | After Reset | Alternate Function |
|---------------------------|--------|--|-------------|--------------------|
| INTP0 | Input | External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified. | Input | P00 |
| INTP1 | | | | P01 |
| TI | Input | 8-bit remote control timer 9 (TM9) timer input | Input | P02 |
| $\overline{\text{SCK3}}$ | I/O | Serial interface serial clock input/output | Input | P20 |
| SO3 | Output | Serial interface serial data output | Input | P21 |
| BUSY | Input | Serial interface automatic transmit/receive busy signal input | Input | P24 |
| SO1 | Output | Serial interface serial data output | Input | P25 |
| SI1 | Input | Serial interface serial data input | Input | P26 |
| $\overline{\text{SCK1}}$ | I/O | Serial interface serial clock input/output | Input | P27 |
| FIP0 to FIP23 | Output | VFD controller/driver high-tolerance large current output. A pull-down resistor can be incorporated to V_{LOAD} in 1-bit units by a mask option. | Output | — |
| FIP24 to FIP31 | | | | P30 to P37 |
| FIP32 to FIP39 | | | | P40 to P47 |
| FIP40 to FIP47 | | VFD controller/driver high-tolerance large current output. A pull-down resistor can be incorporated in 1-bit units by a mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units). | Input | P50 to P57 |
| FIP48 to FIP52 | | | | P60 to P64 |
| V_{LOAD} | — | Connecting pull-down resistor for VFD controller/driver | — | — |
| $\overline{\text{RESET}}$ | Input | System reset input | — | — |
| X1 | Input | Connecting crystal resonator for system clock oscillation | — | — |
| X2 | — | | — | — |
| ANI0 to ANI3 | Input | A/D converter analog input | Input | — |
| AV_{DD} | — | A/D converter analog power supply/reference voltage input. Make the same potential as V_{DD1} . | — | — |
| AV_{SS} | — | A/D converter ground potential. Make the same potential as V_{SS1} . | — | — |
| V_{DD0} | — | Positive power supply for ports | — | — |
| V_{DD1} | — | Positive power supply except for ports, analog block, and VFD controller/driver | — | — |
| V_{DD2} | — | Positive power supply for VFD controller/driver | — | — |
| V_{SS0} | — | Ground potential for ports | — | — |
| V_{SS1} | — | Ground potential except for ports and analog block | — | — |
| IC | — | Internally connected. Connect directly to V_{SS1} . | — | — |

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and the recommended connection of unused pins are shown in Table 3-1.

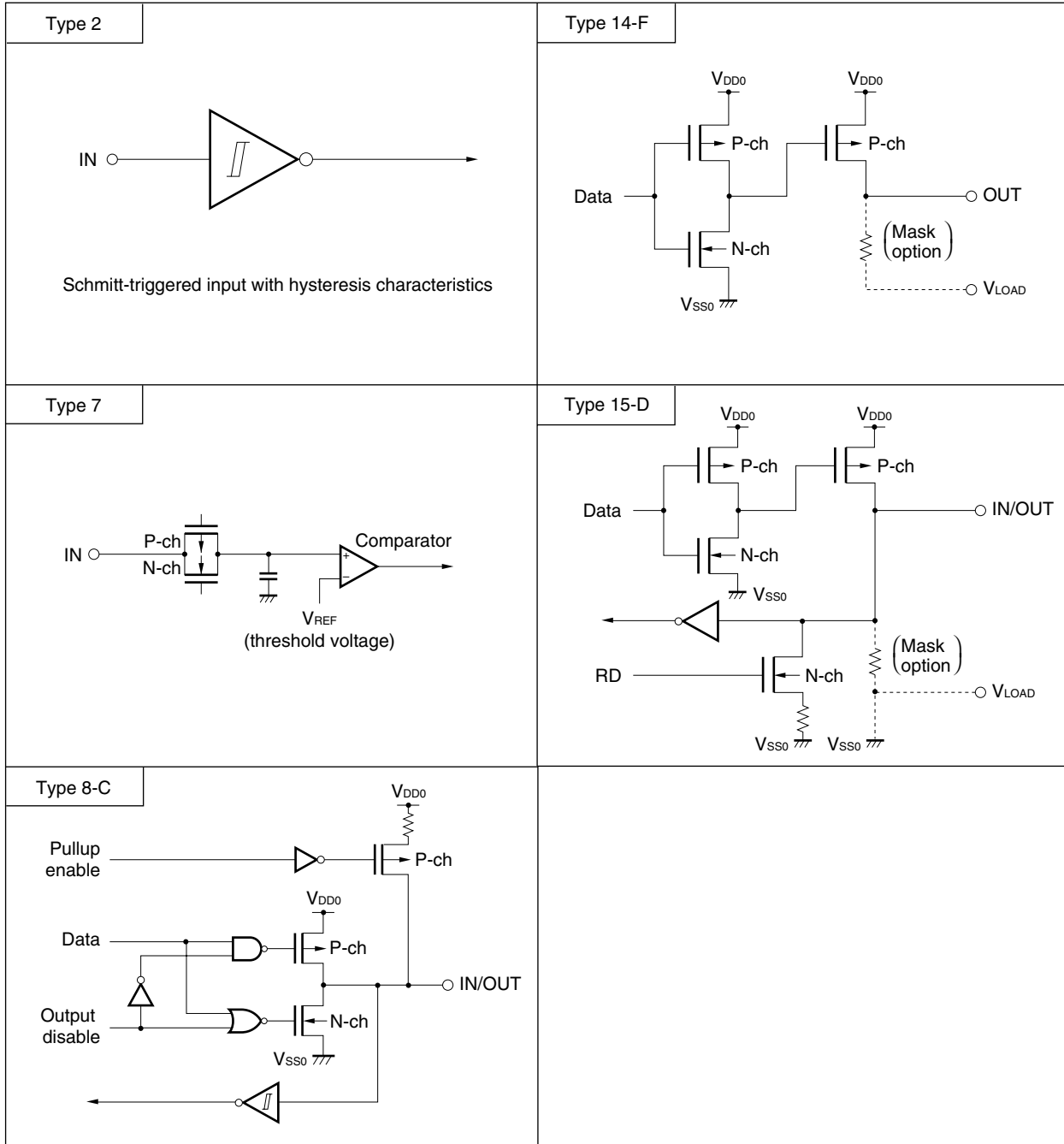
For the I/O circuit configuration of each type, see **Figure 3-1**.

★

Table 3-1. Types of Pin I/O Circuits

| Pin Name | I/O Circuit Type | I/O | Recommended Connection of Unused Pins | |
|------------------------|------------------|--------|--|---------------------|
| P00/INTP0 | 8-C | I/O | Input: Independently connect to V _{SS0} via a resistor. | |
| P01/INTP1 | | | Output: Leave open. | |
| P02/TI | | | Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. | |
| P20/SCK3 | | | | Output: Leave open. |
| P21/SO3 | | | | |
| P22, P23 | | | | |
| P24/BUSY | | | | |
| P25/SO1 | | | | |
| P26/SI1 | | | | |
| P27/SCK1 | | | | |
| P30/FIP24 to P37/FIP31 | 14-F | Output | Leave open. | |
| P40/FIP32 to P47/FIP39 | 15-D | I/O | Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. | |
| P50/FIP40 to P57/FIP47 | | | Output: Leave open. | |
| P60/FIP48 to P64/FIP52 | 14-F | Output | Leave open. | |
| FIP0 to FIP23 | | | — | |
| RESET | 2 | Input | — | |
| ANI0 to ANI3 | 7 | | Connect to V _{DD0} or V _{SS0} . | |
| AV _{DD} | — | — | Connect to V _{DD1} . | |
| AV _{SS} | | | Connect to V _{SS1} . | |
| V _{LOAD} | | | Connect directly to V _{SS1} . | |
| IC | | | | |

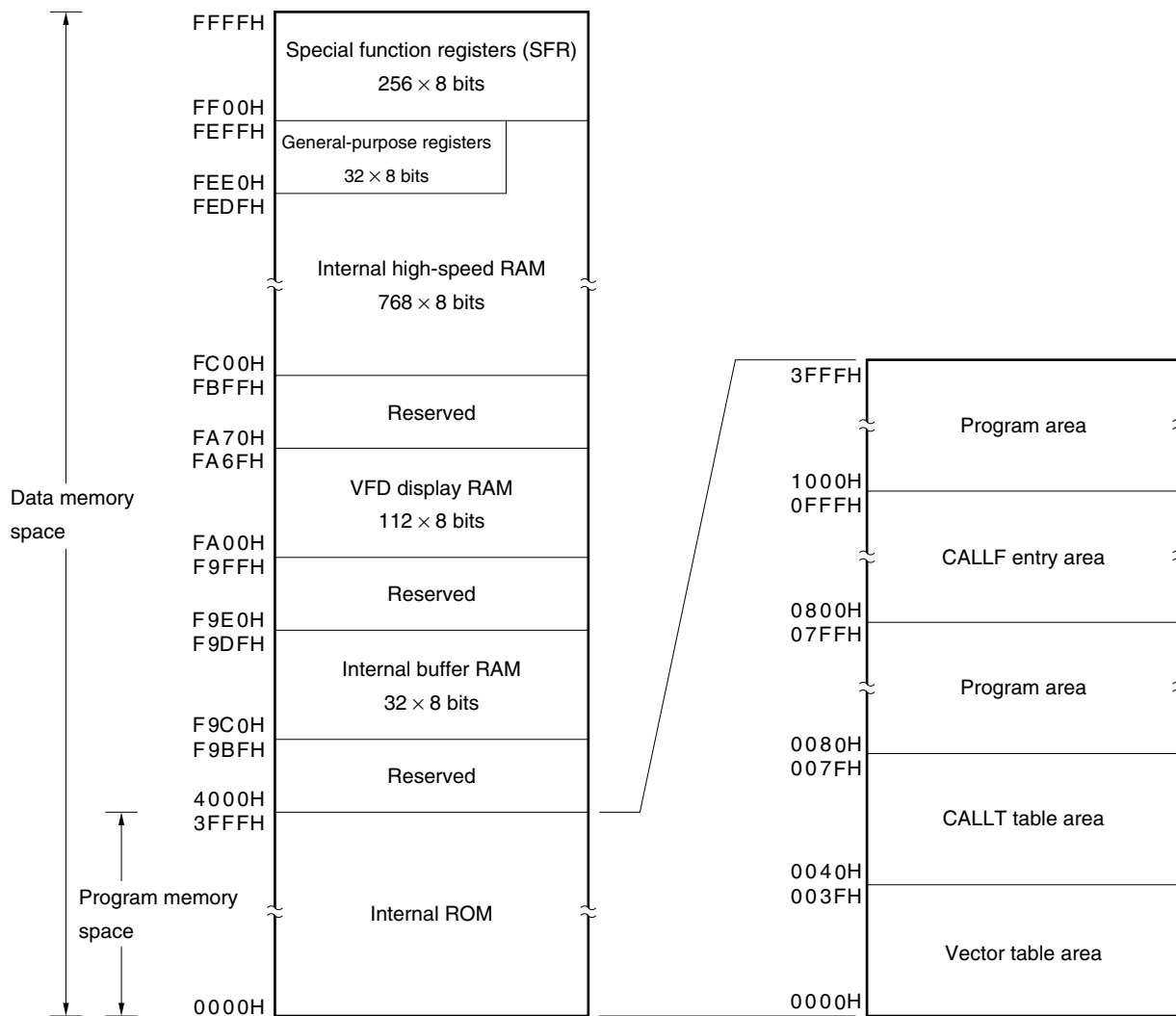
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

The memory map of the μPD780232 is shown in Figure 4-1.

Figure 4-1. Memory Map



5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Port

There are three kinds of I/O ports.

| | |
|--|----|
| • CMOS I/O (ports 0, 2): | 11 |
| • P-ch open-drain output (ports 3, 4): | 16 |
| • P-ch open-drain I/O (ports 5, 6): | 13 |
| Total: | 40 |

Table 5-1. Port Functions

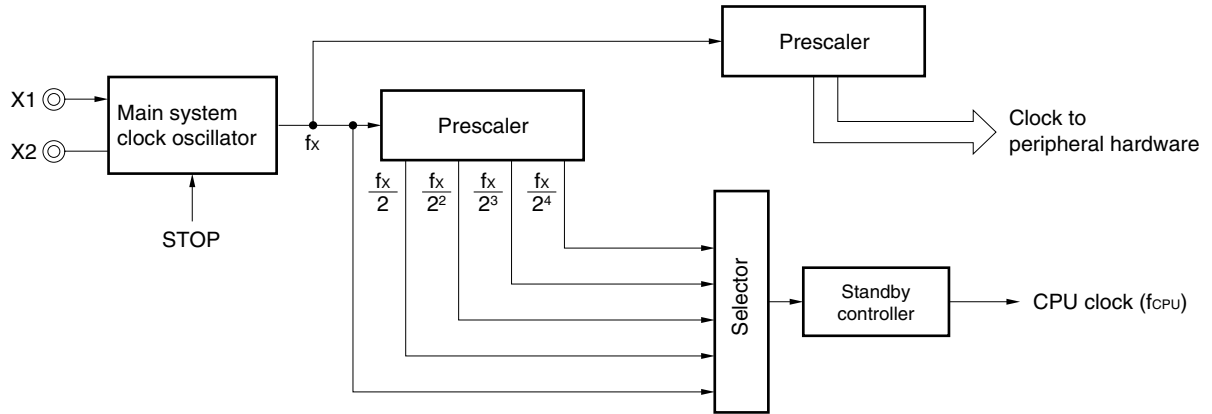
| Name | Pin Name | Function |
|--------|------------|---|
| Port 0 | P00 to P02 | I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip resistor can be specified by software. |
| Port 2 | P20 to P27 | I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip resistor can be specified by software. |
| Port 3 | P30 to P37 | P-ch open-drain high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by a mask option. |
| Port 4 | P40 to P47 | P-ch open-drain high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by a mask option. |
| Port 5 | P50 to P57 | P-ch open-drain high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by a mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units). |
| Port 6 | P60 to P64 | P-ch open-drain high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by a mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units). |

5.2 Clock Generator

The minimum instruction execution time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0 MHz operation with main system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

Four timer/event counter channels are incorporated.

- 8-bit remote control timer: 1 channel
- 8-bit timer: 2 channels
- Watchdog timer: 1 channel

Table 5-2. Timer/Event Counter Operations

| | | 8-Bit Remote Control Timer | 8-Bit Timer | Watchdog Timer |
|----------------|-------------------------|----------------------------|-------------|----------------|
| Operation mode | Interval timer | — | 2 channels | 1 channel |
| Function | Pulse width measurement | 1 input | — | — |
| | Interrupt source | 3 | 2 | 1 |

Figure 5-2. Block Diagram of 8-Bit Remote Control Timer (TM9)

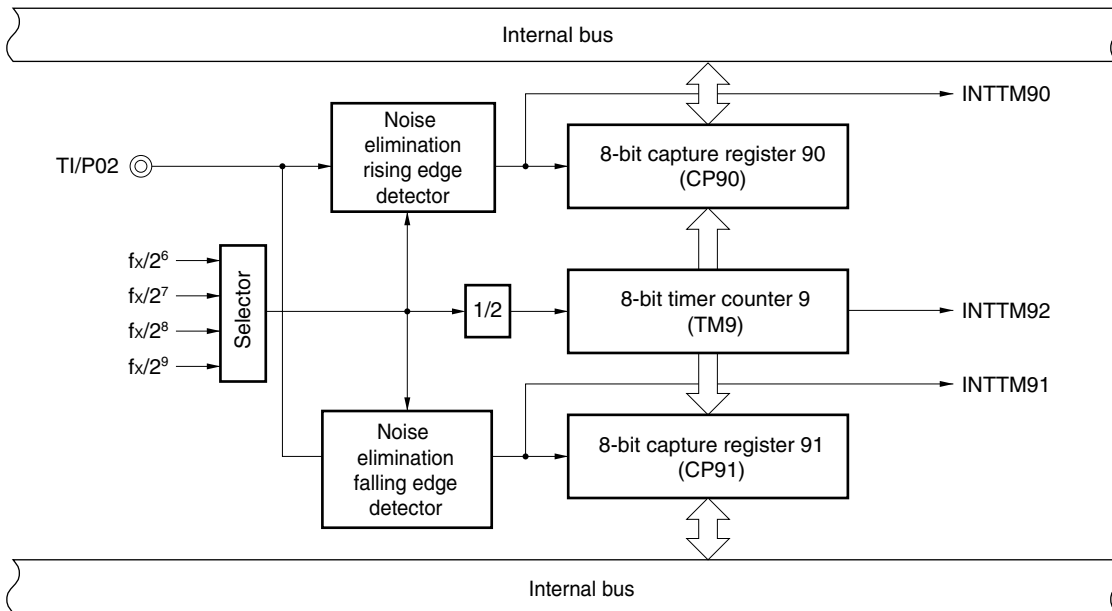


Figure 5-3. Block Diagram of 8-Bit Timer (TM80)

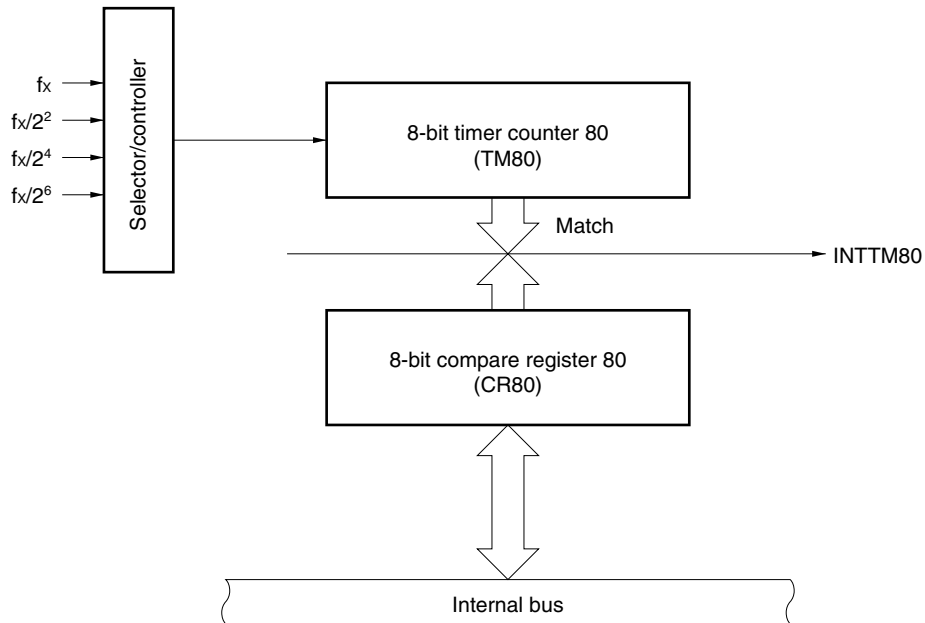
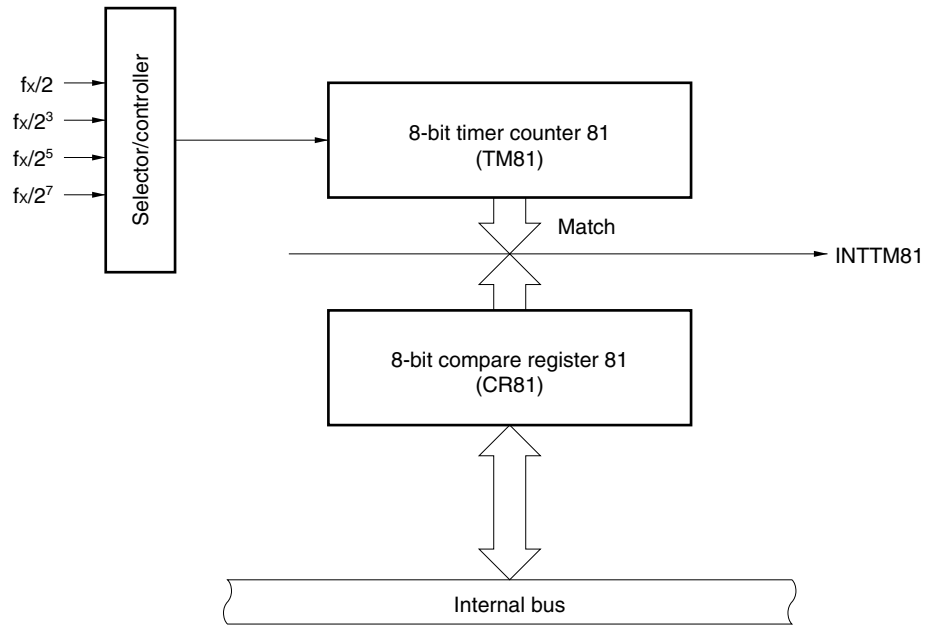
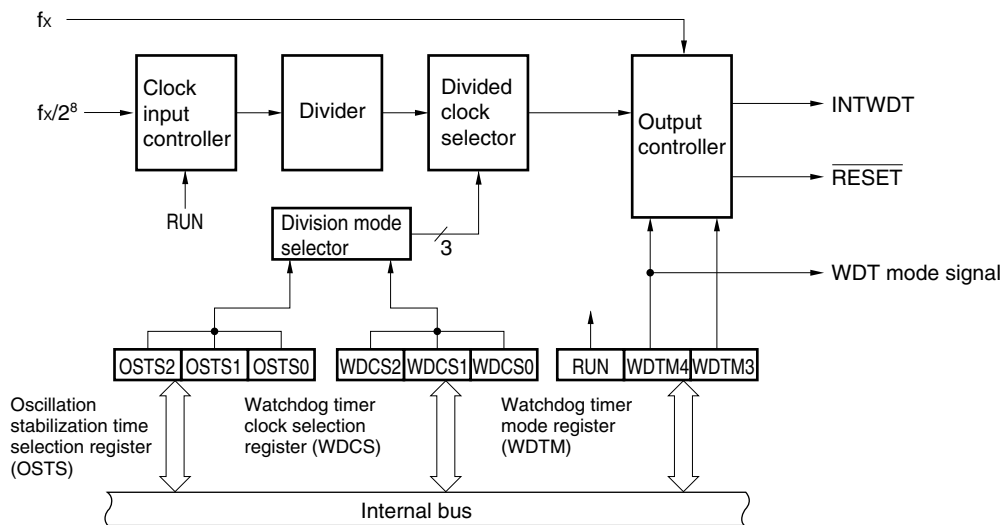


Figure 5-4. Block Diagram of 8-Bit Timer (TM81)



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Figure 5-5. Watchdog Timer Block Diagram

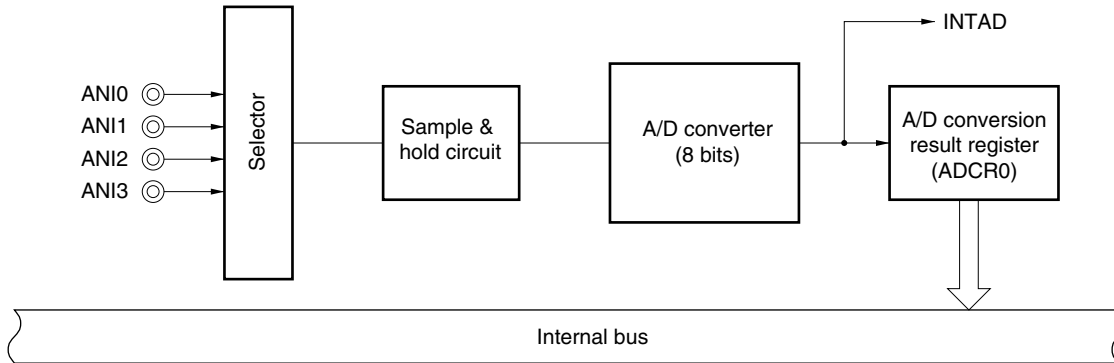


5.4 A/D Converter

An 8-bit resolution 4-channel A/D converter is incorporated.

A/D conversion can be started by software only.

Figure 5-6. A/D Converter Block Diagram



5.5 Serial Interface

Two clocked serial interface channels are incorporated.

Serial interface SIO1 operates in the 3-wire serial mode (with automatic transmit/receive function), in which MSB first/LSB first switching is possible.

Serial interface SIO3 operates in the 2-wire serial mode (transmit only) in which the first bit is fixed to MSB.

Figure 5-7. Serial Interface SIO1 Block Diagram

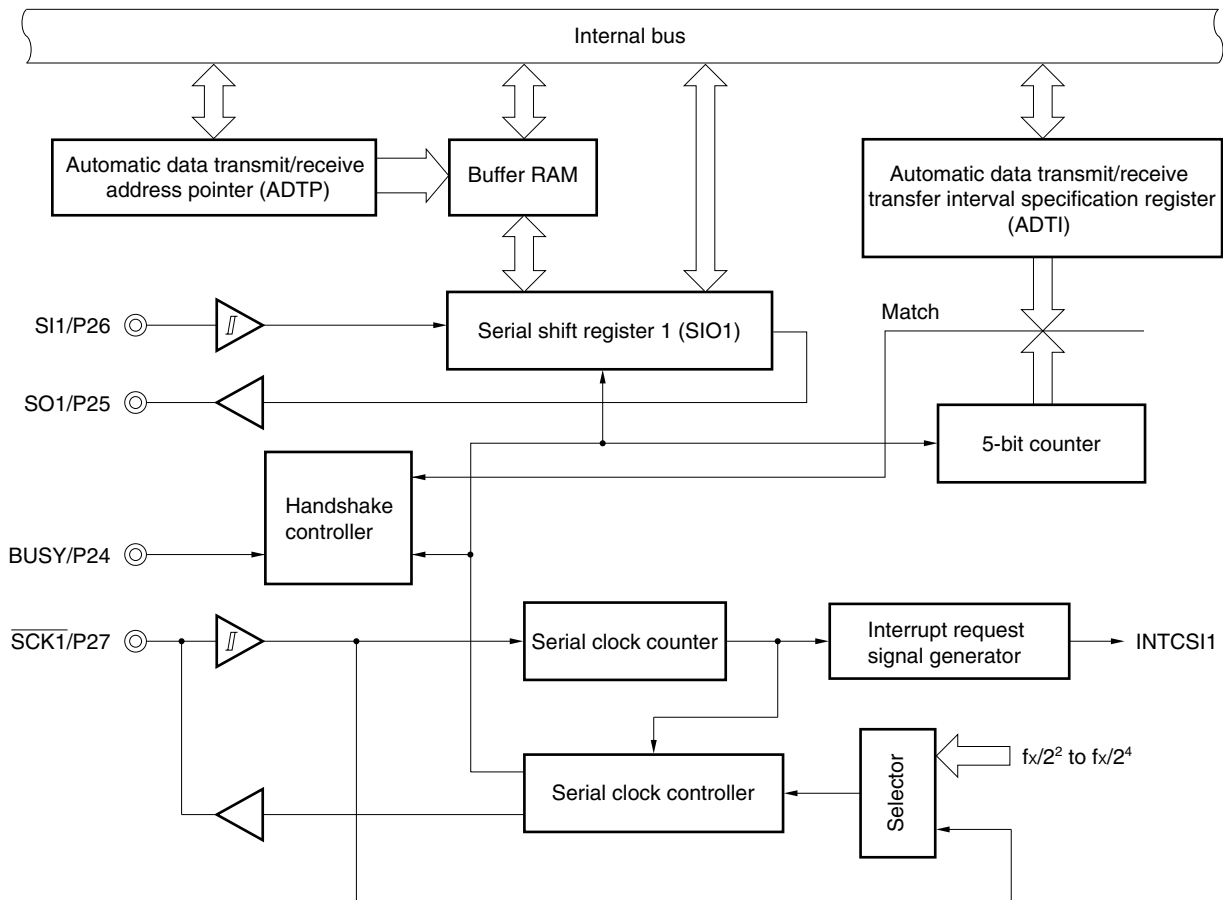
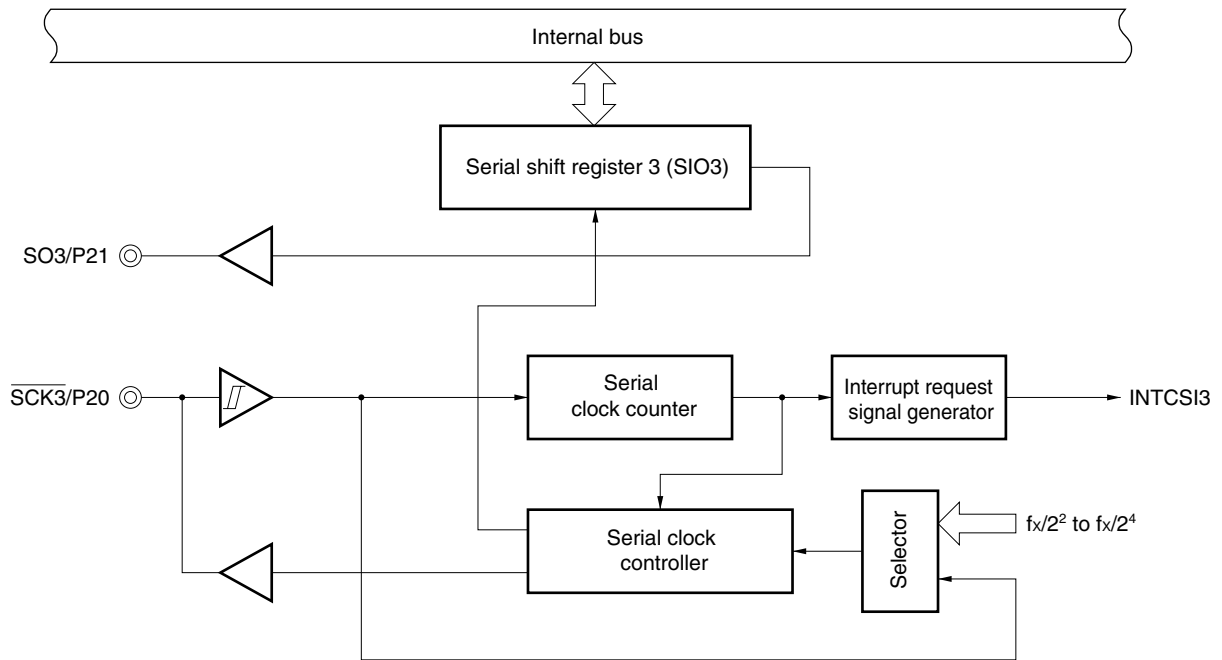


Figure 5-8. Serial Interface SIO3 Block Diagram

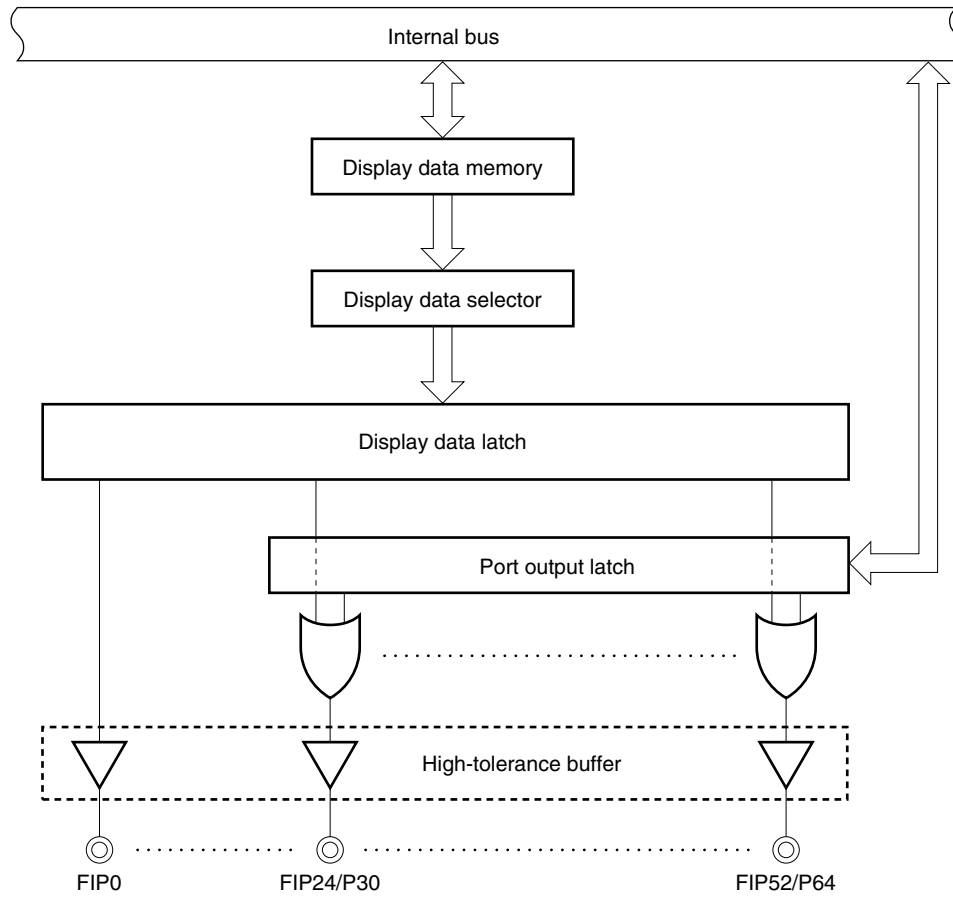


5.6 VFD Controller/Driver

A VFD controller/driver with the following functions is incorporated.

- Total number of display outputs: 53. Output of 16 patterns is enabled.
- 112-byte display RAM is provided to enable display signal output by reading display data automatically (direct memory access (DMA)).
- A port pin that is not used for VFD display can be used as an output port or an I/O port (except for FIP0 to FIP23, which are VFD output-only pins).
- The luminance can be adjusted in 8 levels using display mode register 1 (DSPM1).
- Hardware taking into consideration the key scan application is incorporated.
- Whether the key scan timing is inserted or not is selectable.
- A high-tolerance output buffer (VFD driver) that can drive the VFD directly is incorporated.
- VFD output pins can incorporate a pull-down resistor, set by a mask option.

Figure 5-9. VFD Controller/Driver Block Diagram



6. INTERRUPT FUNCTIONS

There are 3 types of interrupt functions.

- Non-maskable: 1
- Maskable: 12
- Software: 1

Table 6-1. Interrupt Source List

| Interrupt Type | Default Priority ^{Note 1} | Interrupt Source | | Internal/External | Vector Table Address | Basic Configuration Type ^{Note 2} | | |
|----------------|------------------------------------|------------------|--|-------------------|----------------------|--|-------|-----|
| | | Name | Trigger | | | | | |
| Non-maskable | — | INTWDT | Watchdog timer overflow (when watchdog timer mode 1 is selected) | Internal | 0004H | (A) | | |
| Maskable | 0 | INTWDT | Watchdog timer overflow (when interval timer mode is selected) | | | External | 0006H | (B) |
| | 1 | INTP0 | Pin input edge detection | 0008H | (C) | | | |
| | 2 | INTP1 | | | | | | |
| | 3 | INTTM90 | Remote control timer input rising edge detection | Internal | 000AH | (B) | | |
| | 4 | INTTM91 | Remote control timer input falling edge detection | | 000CH | | | |
| | 5 | INTTM92 | Remote control timer overflow | | 000EH | | | |
| | 6 | INTKS | Key scan timing from VFD controller/driver | | 0010H | | | |
| | 7 | INTCSI1 | Serial interface SIO1 transfer end | | 0012H | | | |
| | 8 | INTCSI3 | Serial interface SIO3 transfer end | | 0014H | | | |
| | 9 | INTTM80 | TM80 and CR80 match | | 0016H | | | |
| | 10 | INTTM81 | TM81 and CR81 match | | 0018H | | | |
| | 11 | INTAD | A/D conversion end | | 001AH | | | |
| Software | — | BRK | BRK instruction execution | | — | | 003EH | (D) |

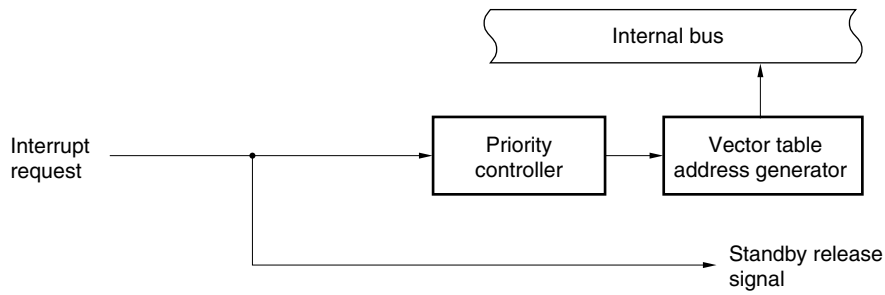
Notes 1. Default Priority is the priority order when more than one maskable interrupt request is generated simultaneously. 0 is the highest priority and 11 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

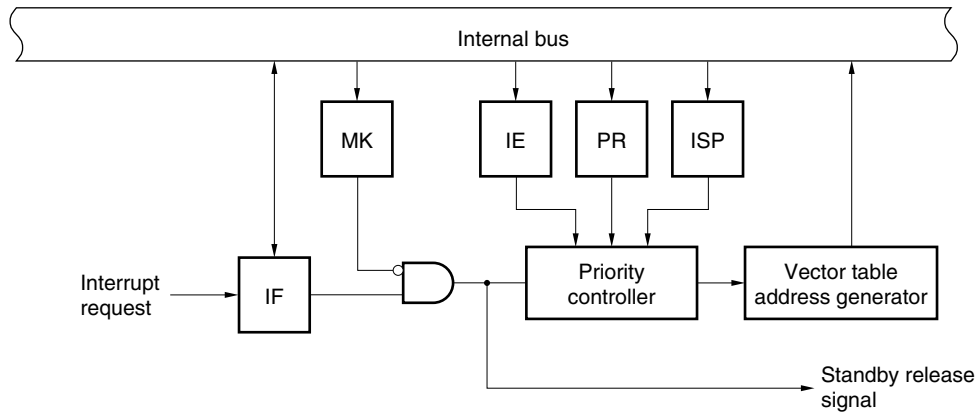
★ **Remark** Two watchdog timer interrupt sources (INTWDT) are available: a non-maskable interrupt and a maskable interrupt (internal), either of which can be selected.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0, INTP1)

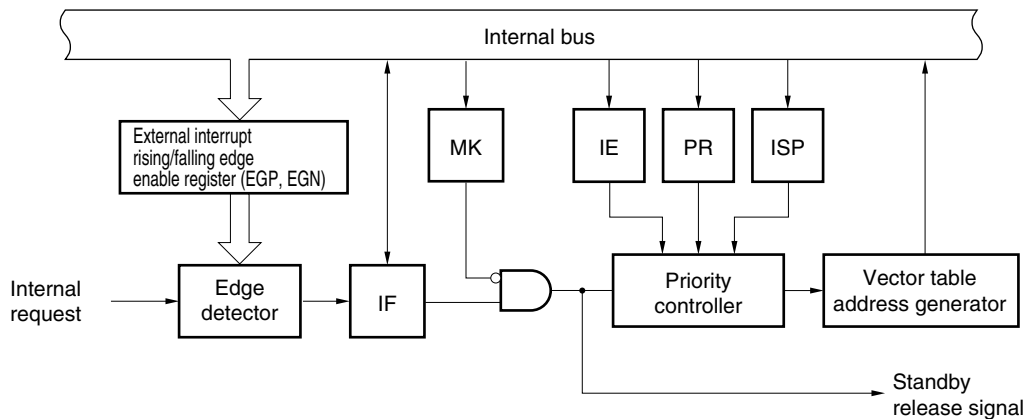
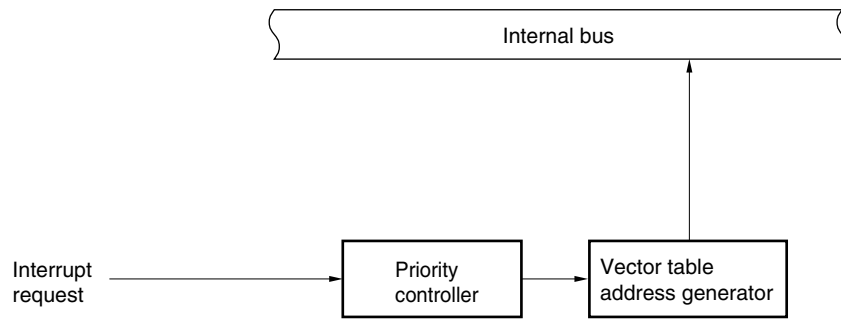


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) Software interrupt

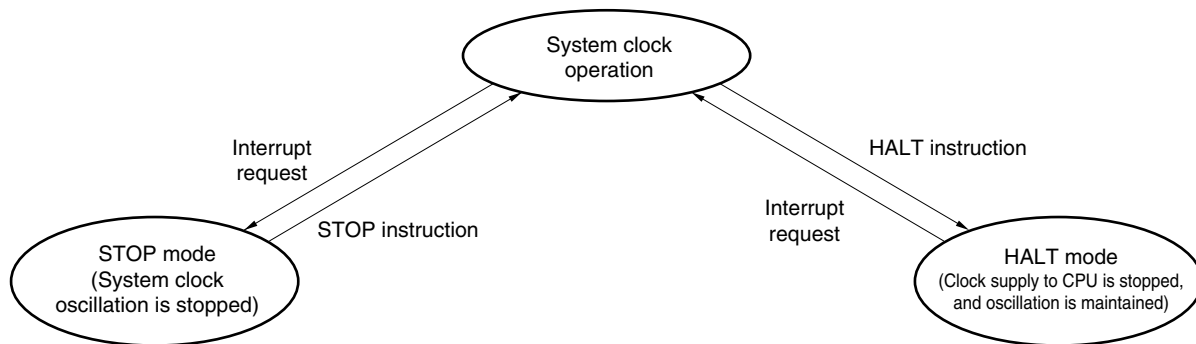


7. STANDBY FUNCTION

The standby function is a function to reduce the current consumption. The following two types of standby functions are available.

- HALT mode: Halts the CPU operating clock and enables a reduction in the average current consumption by intermittent operation with normal operation.
- STOP mode: Halts the system clock oscillation. Halts all operations with the system clock and sets an ultra-low power consumption state.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two types of resetting methods are available.

- External reset by the $\overline{\text{RESET}}$ input
- Internal reset by watchdog timer loop detection

★ 9. MASK OPTION

The mask options for the μPD780232 are shown in Table 9-1.

Table 9-1. Pin Mask Option Selection

| Pin Name | Mask Option |
|--|--|
| FIP 0 to FIP23, P30/FIP24 to P37/FIP31, P40/FIP32 to P47/FIP39 | An on-chip pull-down resistor can be specified for V_{LOAD} in 1-bit units. |
| P50/FIP40 to P57/FIP47, P60/FIP48 to P64/FIP52 | An on-chip pull-down resistor can be specified for V_{LOAD} or V_{SS0} in 1-bit units. |

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

| 2nd Operand 1st Operand | #byte | A | r>Note | sfr | saddr | !addr16 | PSW | [DE] | [HL] | [HL+byte] [HL+B] [HL+C] | \$addr16 | 1 | None |
|-------------------------------|--|--|---|------------|---|---|-----|------------|---|---|----------|----------------------------|--------------|
| A | ADD ADDC SUB SUBC AND OR XOR CMP | | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV | MOV XCH | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | | ROR ROL RORC ROLC | |
| r | MOV | MOV ADD ADDC SUB SUBC AND OR XOR CMP | | | | | | | | | | | INC DEC |
| B, C | | | | | | | | | | | DBNZ | | |
| sfr | MOV | MOV | | | | | | | | | | | |
| saddr | MOV ADD ADDC SUB SUBC AND OR XOR CMP | MOV | | | | | | | | | DBNZ | | INC DEC |
| !addr16 | | MOV | | | | | | | | | | | |
| PSW | MOV | MOV | | | | | | | | | | | PUSH POP |
| [DE] | | MOV | | | | | | | | | | | |
| [HL] | | MOV | | | | | | | | | | | ROR4 ROL4 |
| [HL+byte] [HL+B] [HL+C] | | MOV | | | | | | | | | | | |
| X | | | | | | | | | | | | | MULU |
| C | | | | | | | | | | | | | DIVUW |

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

| 2nd Operand 1st Operand | #word | AX | rp ^{Note} | sfrp | saddrp | !addr16 | SP | None |
|----------------------------|----------------------|----------------------|--------------------|------|--------|---------|------|-----------------------------|
| AX | ADDW SUBW CMPW | | MOVW XCHW | MOVW | MOVW | MOVW | MOVW | |
| rp | MOVW | MOVW ^{Note} | | | | | | INCW DECW PUSH POP |
| sfrp | MOVW | MOVW | | | | | | |
| saddrp | MOVW | MOVW | | | | | | |
| !addr16 | | MOVW | | | | | | |
| SP | MOVW | MOVW | | | | | | |

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

| 2nd Operand 1st Operand | A.bit | sfr.bit | saddr.bit | PSW.bit | [HL].bit | CY | \$addr16 | None |
|----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------|-------------------|----------------------|
| A.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| sfr.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| saddr.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| PSW.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| [HL].bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| CY | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | | | SET1 CLR1 NOT1 |

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

| 2nd Operand 1st Operand | AX | !addr16 | !addr11 | [addr5] | \$addr16 |
|----------------------------|----|------------|---------|---------|------------------------------|
| Basic instruction | BR | CALL BR | CALLF | CALLT | BR BC BNC BZ BNZ |
| Compound instruction | | | | | BT BF BTCLR DBNZ |

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

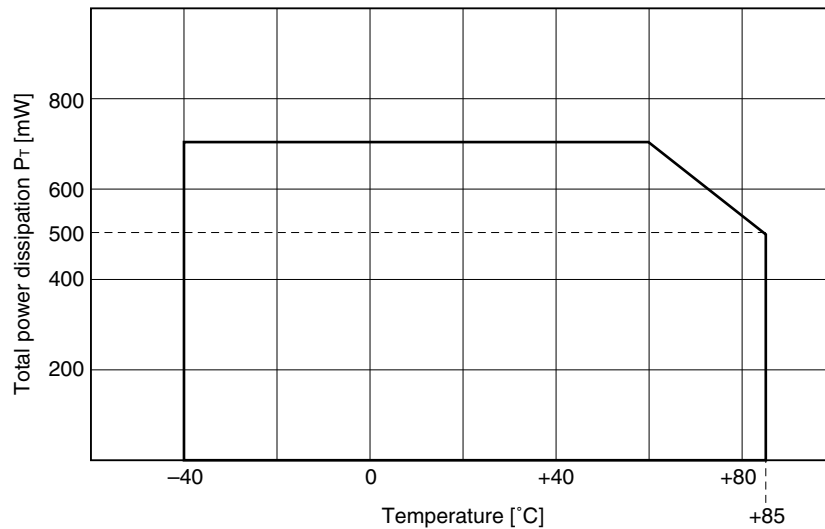
| Parameter | Symbol | Conditions | Rating | Unit | |
|-------------------------------|-------------------------------|---|---|------|----|
| Supply voltage | V _{DD} | | -0.3 to +6.5 | V | |
| | V _{LOAD} | | V _{DD} - 45 to V _{DD} + 0.3 | V | |
| | AV _{DD} | | -0.3 to V _{DD} + 0.3 | V | |
| | AV _{SS} | | -0.3 to +0.3 | V | |
| Input voltage | V _{I1} | P00 to P02, P20 to P27, X1, X2, RESET | -0.3 to V _{DD} + 0.3 | V | |
| | V _{I2} | P50 to P57, P60 to P64 P-ch open drain | V _{DD} - 45 to V _{DD} + 0.3 | V | |
| Output voltage | V _{O1} | | -0.3 to V _{DD} + 0.3 | V | |
| | V _{O2} | | V _{DD} - 45 to V _{DD} + 0.3 | V | |
| Analog input voltage | V _{AN} | ANI0 to ANI3 Analog input pins | AV _{SS} to AV _{DD} | V | |
| Output current, high | I _{OH} | Per pin for P00 to P02 and P20 to P27 | -10 | mA | |
| | | Total for P00 to P02 and P20 to P27 | -30 | mA | |
| | | Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64 | -30 | mA | |
| | | Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64 | Peak value | -300 | mA |
| | | | rms value | -120 | mA |
| Output current, low | I _{OL} Note 1 | Per pin for P00 to P02 and P20 to P27 | Peak value | 10 | mA |
| | | | rms value | 5 | mA |
| | | Total for P00 to P02 and P20 to P27 | Peak value | 20 | mA |
| | | | rms value | 10 | mA |
| Total power dissipation | P _T Note 2 | T _A = -40 to +60°C | 700 | mW | |
| | | T _A = +60 to +85°C | 500 | mW | |
| Operating ambient temperature | T _A | | -40 to +85 | °C | |
| Storage temperature | T _{stg} | | -40 to +150 | °C | |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Notes 1. The rms value should be calculated as follows: [rms value] = [Peak value] × √Duty

Notes 2. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780232 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

- <1> CPU power consumption: Calculate V_{DD} (MAX.) × I_{DD} (MAX.).
- <2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.
- <3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

The following shows how to calculate total power consumption for the example in Figure 11-1.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids × 10 segments (blanking width = 1/16)

The maximum current at the grid pin is 15 mA.

The maximum current at the segment pin is 5 mA.

At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids V_{OD} = V_{DD} - 2 V (voltage drop of 2 V)

Segments V_{OD} = V_{DD} - 0.5 V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = -35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: $5.5 \text{ V} \times 21.0 \text{ mA} = 115.5 \text{ mW}$

<2> Output pin power consumption:

$$\begin{aligned} \text{Grid} & (V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width}) \\ & = 2 \text{ V} \times \frac{15 \text{ mA} \times 11 \text{ grids}}{11 \text{ grids} + 1} \times \left(1 - \frac{1}{16}\right) = 25.8 \text{ mW} \end{aligned}$$

$$\begin{aligned} \text{Segment} & (V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width}) \\ & = 0.5 \text{ V} \times \frac{5 \text{ mA} \times 31 \text{ dots}}{11 \text{ grids} + 1} \times \left(1 - \frac{1}{16}\right) = 6.1 \text{ mW} \end{aligned}$$

<3> Pull-down resistor power consumption:

$$\begin{aligned} \text{Grid} & \frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width}) \\ & = \frac{(5.5 \text{ V} - 2 \text{ V} - (-35 \text{ V}))^2}{35 \text{ k}\Omega} \times \frac{11 \text{ grids}}{11 \text{ grids} + 1} \times \left(1 - \frac{1}{16}\right) = 36.4 \text{ mW} \end{aligned}$$

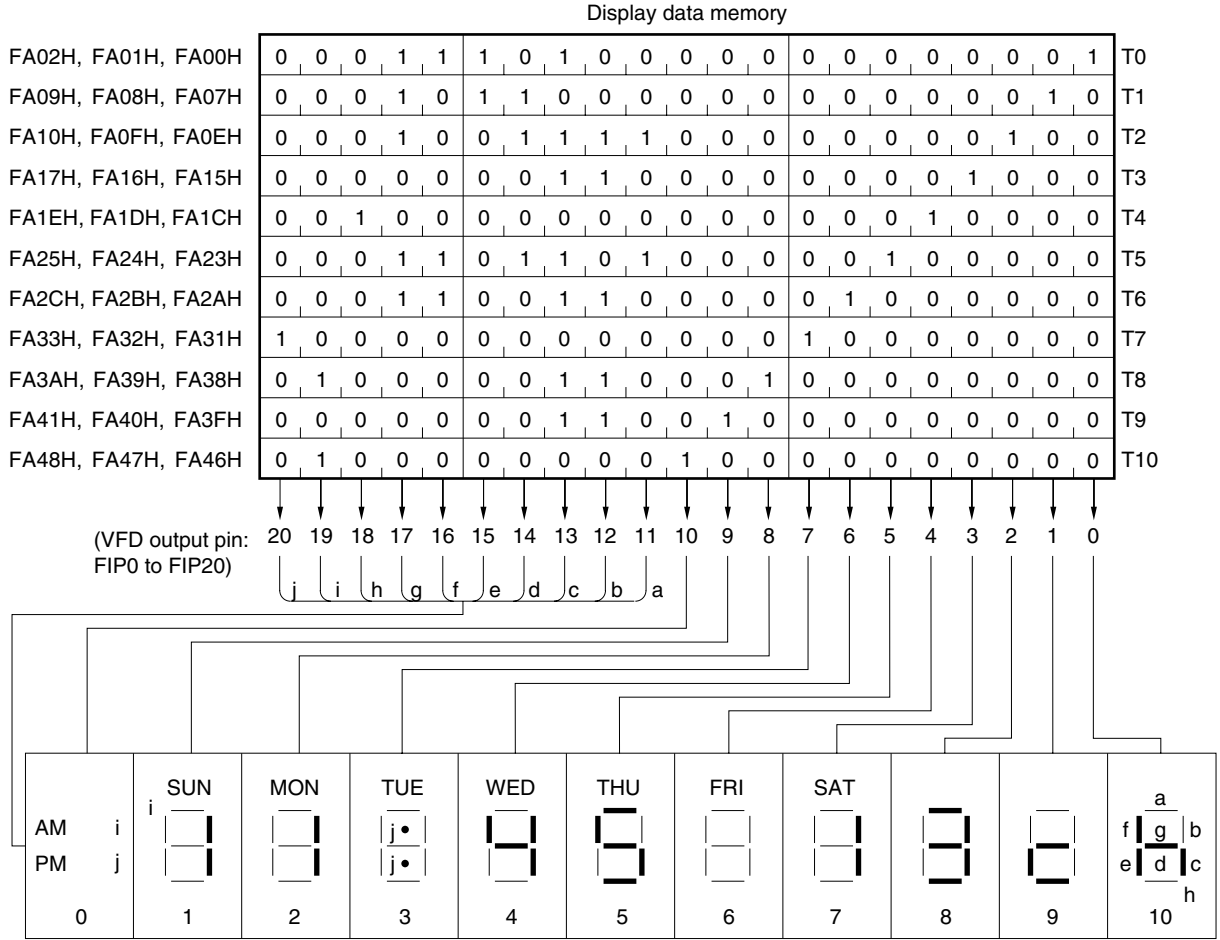
$$\begin{aligned} \text{Segment} & \frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width}) \\ & = \frac{(5.5 \text{ V} - 0.5 \text{ V} - (-35 \text{ V}))^2}{35 \text{ k}\Omega} \times \frac{31 \text{ dots}}{11 \text{ grids} + 1} \times \left(1 - \frac{1}{16}\right) = 110.7 \text{ mW} \end{aligned}$$

$$\text{Total power consumption} = \text{<1>} + \text{<2>} + \text{<3>} = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 \text{ mW}$$

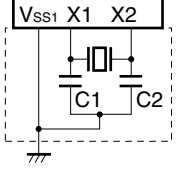
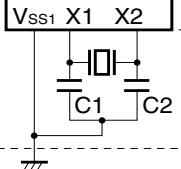
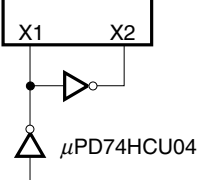
In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption.

However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

Figure 11-1. Display Example of 10 Segments-11 Digits



System Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---|--|--|------|------|------|------|
| Ceramic resonator |  | Oscillation frequency (f _x) ^{Note 1} | V _{DD} = Oscillation voltage range | 1 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After V _{DD} reaches the minimum value of oscillation voltage range | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency (f _x) ^{Note 1} | | 1 | | 5 | MHz |
| | | Oscillation stabilization time ^{Note 2} | | | | 10 | ms |
| External clock |  | X1 input frequency (f _x) ^{Note 1} | | 1 | | 5 | MHz |
| | | X1 input high-/low-level width (t _{xH} /t _{xL}) | | 85 | | 450 | ns |

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

Recommended Oscillator Constant

System Clock: Ceramic Resonator (T_A = -40 to +85°C)

| Manufacturer | Part Number | Frequency (MHz) | Recommended Circuit Constant | | Oscillation Voltage Range | |
|-----------------------|--------------|-----------------|------------------------------|---------|---------------------------|----------|
| | | | C1 (pF) | C2 (pF) | MIN. (V) | MAX. (V) |
| Murata Mfg. Co., Ltd. | CSB 1000J | 1.00 | 150 | 150 | 4.5 | 5.5 |
| | CSA2.00MG040 | 2.00 | 100 | 100 | | |
| | CST2.00MG040 | | On-chip | On-chip | | |
| | CSA3.58MG | 3.58 | 30 | 30 | | |
| | CST3.58MGW | | On-chip | On-chip | | |
| | CSTS0358MG06 | | | | | |
| | CSA4.19MG | 4.19 | 30 | 30 | | |
| | CST4.19MGW | | On-chip | On-chip | | |
| | CSTS0419MG06 | | | | | |
| | CSA5.00MG | 5.00 | 30 | 30 | | |
| | CST5.00MGW | | On-chip | On-chip | | |
| | CSTS0500MG03 | | | | | |

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--------------------|------------------|--|---|------|------|------|----|
| Input capacitance | C _{IN} | f = 1 MHz Unmeasured pins returned to 0 V | P00 to P02, P20 to P27 | | | 15 | pF |
| | | | P50 to P57, P60 to P64 | | | 35 | pF |
| Output capacitance | C _{OUT} | f = 1 MHz Unmeasured pins returned to 0 V | P00 to P02, P20 to P27 | | | 15 | pF |
| | | | P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23 | | | 35 | pF |
| I/O capacitance | C _{IO} | f = 1 MHz Unmeasured pins returned to 0 V | P00 to P02, P20 to P27 | | | 15 | pF |
| | | | P50 to P57, P60 to P64 | | | 35 | pF |

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|-------------------|---|--|------|--------------------|------|----|
| Input voltage, high | V _{IH1} | P00 to P02, P20 to P27, $\overline{\text{RESET}}$ | 0.7V _{DD} | | V _{DD} | V | |
| | V _{IH2} | P50 to P57, P60 to P64 | 0.7V _{DD} | | V _{DD} | V | |
| | V _{IH3} | X1, X2 | V _{DD} - 0.5 | | V _{DD} | V | |
| Input voltage, low | V _{IL1} | P00 to P02, P20 to P27, $\overline{\text{RESET}}$ | 0 | | 0.2V _{DD} | V | |
| | V _{IL2} | X1, X2 | 0 | | 0.4 | V | |
| Output voltage, high | V _{OH} | I _{OH} = -1 mA | V _{DD} - 1.0 | | V _{DD} | V | |
| | | I _{OH} = -100 μA | V _{DD} - 0.5 | | V _{DD} | V | |
| Output voltage, low | V _{OL} | P00 to P02, P20 to P27 | | | 0.5 | V | |
| Input leakage current, high | I _{LIH1} | P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$ | | | 3 | μA | |
| | I _{LIH2} | X1, X2 | | | 20 | μA | |
| Input leakage current, low | I _{LIL1} | P00 to P02, P20 to P27, $\overline{\text{RESET}}$ | | | -3 | μA | |
| | I _{LIL2} | X1, X2 | | | -20 | μA | |
| | I _{LIH3} | P50 to P57, P60 to P64 | V _{IN} = V _{LOAD} = V _{DD} - 40 V | | -10 | μA | |
| Output leakage current, high | I _{LOH} | P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64 | | | 3 | μA | |
| Output leakage current, low | I _{LOL1} | P00 to P02, P20 to P27 | | | -3 | μA | |
| | I _{LOL2} | P30 to P37, P40 to P47, P50 to P57, P60 to P64 | | | -10 | μA | |
| VFD output current | I _{OD} | FIP0 to FIP19 | | | -15 | mA | |
| | | FIP20 to FIP52 | | | -5 | mA | |
| Software pull-up resistance | R ₁ | P00 to P02, P20 to P27 | | 10 | 30 | 100 | kΩ |
| On-chip mask option pull-down resistance (V _{SS0} connection) | R ₂ | P50 to P57, P60 to P64 | | 15 | 35 | 90 | kΩ |
| On-chip mask option pull-down resistance (V _{LOAD} connection) | R ₃ | FIP0 to FIP52 | V _{OD} - V _{LOAD} = 40 V | 30 | 60 | 135 | kΩ |
| Power supply current ^{Note} | I _{DD1} | 5 MHz crystal oscillation operation mode | PCC = 00H | | 7 | 14 | mA |
| | I _{DD2} | 5 MHz crystal oscillation HALT mode | | | 1.5 | 4.5 | mA |
| | I _{DD3} | STOP mode | | | 1 | 30 | μA |

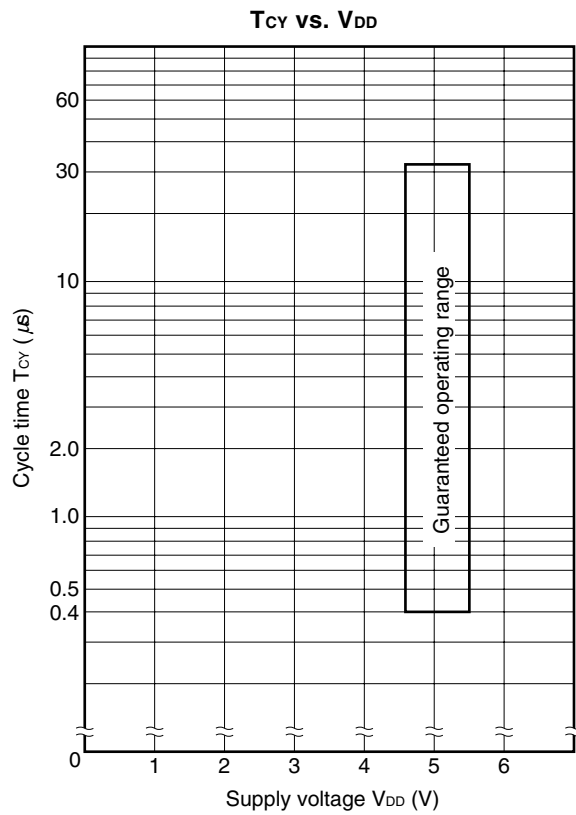
Note Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.
2. PCC: Processor clock control register

AC Characteristics

(1) Basic operation (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--|---------------------------------|------|------|------|------|
| Cycle time (minimum instruction execution time) | T _{CY} | Operated with main system clock | 0.4 | | 32 | μs |
| Interrupt request input high-/low-level width | t _{INTH} t _{INTL} | INTP0, INTP1 | 10 | | | μs |
| RESET low-level width | t _{RSL} | | 10 | | | μs |



(2) Timer/counter (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------------------------|--------------------------------------|------------|--|------|------|------|
| T1 input high-/ low-level width | t _{TIH} t _{TIL} | | 2/F _{count} + 0.2 ^{Note} | | | μs |

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from f_x/2⁶, f_x/2⁷, f_x/2⁸, and f_x/2⁹).

(3) Serial interface (T_A = -40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{\text{SCK1}}$: Internal clock output)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--------------------------------------|----------------------------|---------------------------|------|------|------|
| $\overline{\text{SCK1}}$ cycle time | t _{KCY1} | | 800 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | t _{KH1} t _{KL1} | | t _{KCY1} /2 - 50 | | | ns |
| S11 setup time (to $\overline{\text{SCK1}}\uparrow$) | t _{SIK1} | | 100 | | | ns |
| S11 hold time (from $\overline{\text{SCK1}}\uparrow$) | t _{KSI1} | | 400 | | | ns |
| Delay time from $\overline{\text{SCK1}}\downarrow$ to SO1 output | t _{KSO1} | C = 100 pF ^{Note} | | | 300 | ns |

Note C is the load capacitance of the $\overline{\text{SCK1}}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{\text{SCK1}}$: External clock input)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--------------------------------------|----------------------------|------|------|------|------|
| $\overline{\text{SCK1}}$ cycle time | t _{KCY2} | | 800 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | t _{KH2} t _{KL2} | | 400 | | | ns |
| S11 setup time (to $\overline{\text{SCK1}}\uparrow$) | t _{SIK2} | | 100 | | | ns |
| S11 hold time (from $\overline{\text{SCK1}}\uparrow$) | t _{KSI2} | | 400 | | | ns |
| Delay time from $\overline{\text{SCK1}}\downarrow$ to SO1 output | t _{KSO2} | C = 100 pF ^{Note} | | | 300 | ns |
| $\overline{\text{SCK1}}$ rise/fall time | t _{R2} t _{F2} | | | | 1 | μs |

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{\text{SCK3}}$...Internal clock output)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------------------------|----------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK3}}$ cycle time | t_{CY3} | | 800 | | | ns |
| $\overline{\text{SCK3}}$ high-/low-level width | t_{H3} t_{L3} | | $t_{\text{CY3}}/2 - 50$ | | | ns |
| Delay time from $\overline{\text{SCK3}}\downarrow$ to SO3 output | t_{SO3} | C = 100 pF ^{Note} | | | 300 | ns |

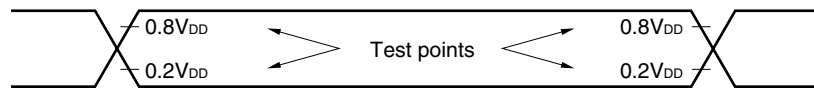
Note C is the load capacitance of the $\overline{\text{SCK3}}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{\text{SCK3}}$...External clock input)

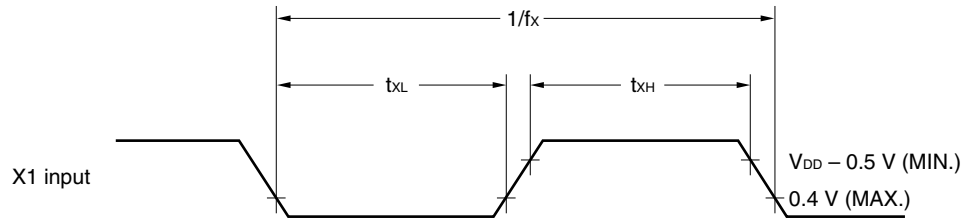
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------------------------|----------------------------|------|------|------|------|
| $\overline{\text{SCK3}}$ cycle time | t_{CY4} | | 800 | | | ns |
| $\overline{\text{SCK3}}$ high-/low-level width | t_{H4} t_{L4} | | 400 | | | ns |
| Delay time from $\overline{\text{SCK3}}\downarrow$ to SO3 output | t_{SO4} | C = 100 pF ^{Note} | | | 300 | ns |
| $\overline{\text{SCK3}}$ rise/fall time | t_{R4} t_{F4} | | | | 1 | μs |

Note C is the load capacitance of the SO3 output line.

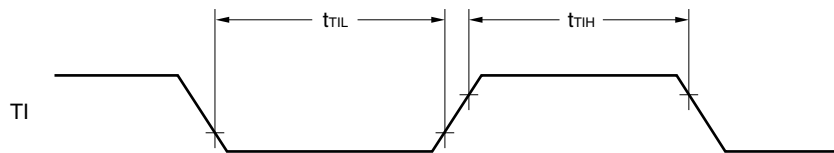
AC Timing Test Points (Excluding X1 Input)



Clock Timing

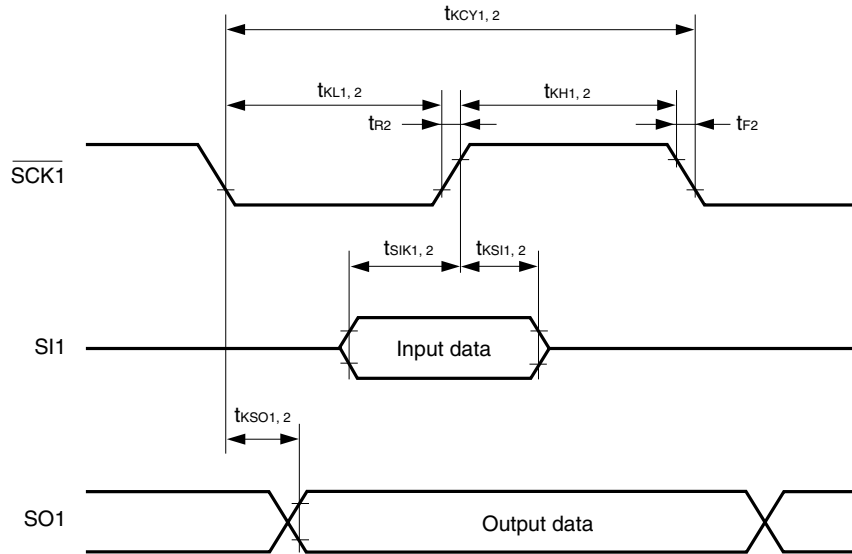


TI Timing

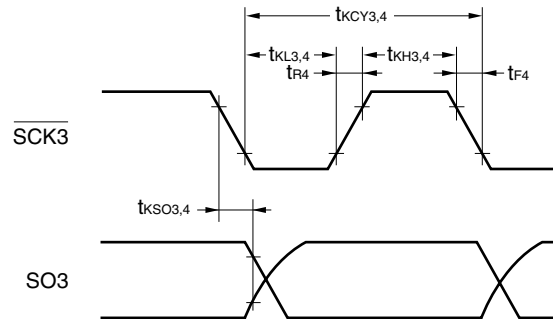


Serial Transfer Timing

3-wire serial mode:



2-wire serial mode:



A/D Converter Characteristics (T_A = -40 to +85°C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|-------------------|------------|------------------|------|------------------|------|
| Resolution | | | | | 8 | bit |
| Overall error ^{Note 1} | | | | | ±1.0 | % |
| Conversion time ^{Note 2} | t _{CONV} | | 14 | | | μs |
| Analog input voltage | V _{IAN} | | AV _{SS} | | AV _{DD} | V |

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

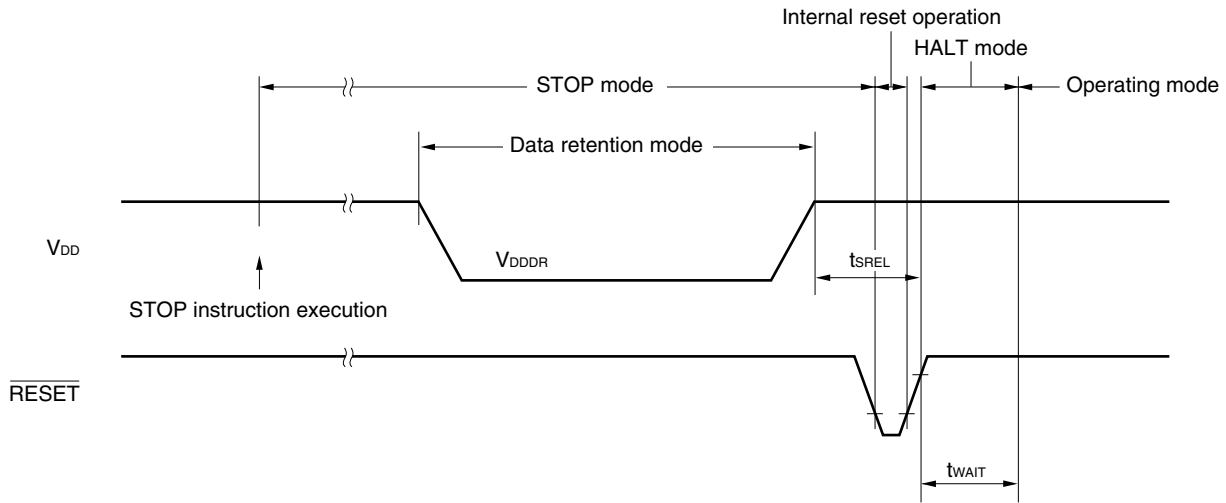
2. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85°C)

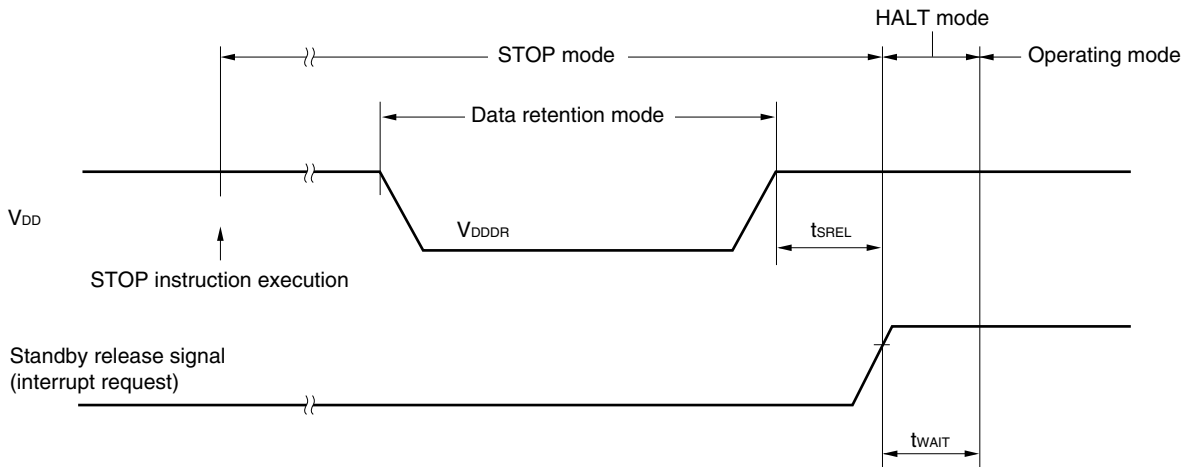
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-------------------|--------------------------------------|------|---------------------------------|------|------|
| Data retention supply voltage | V _{DDDR} | | 2.0 | | 5.5 | V |
| Data retention supply current | I _{DDDR} | | | 0.1 | 30 | μA |
| Release signal set time | t _{SREL} | | 0 | | | μs |
| Oscillation stabilization wait time | t _{WAIT} | Release by $\overline{\text{RESET}}$ | | 2 ¹⁷ /f _x | | ms |
| | | Release by interrupt request | | Note | | ms |

Note 2¹²/f_x, 2¹⁴/f_x to 2¹⁷/f_x can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

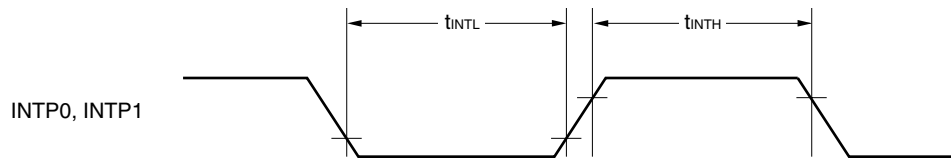
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



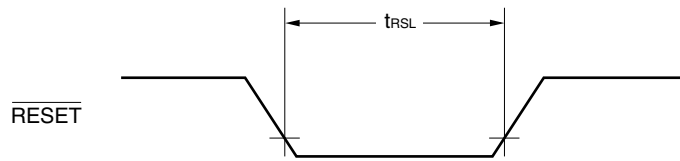
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

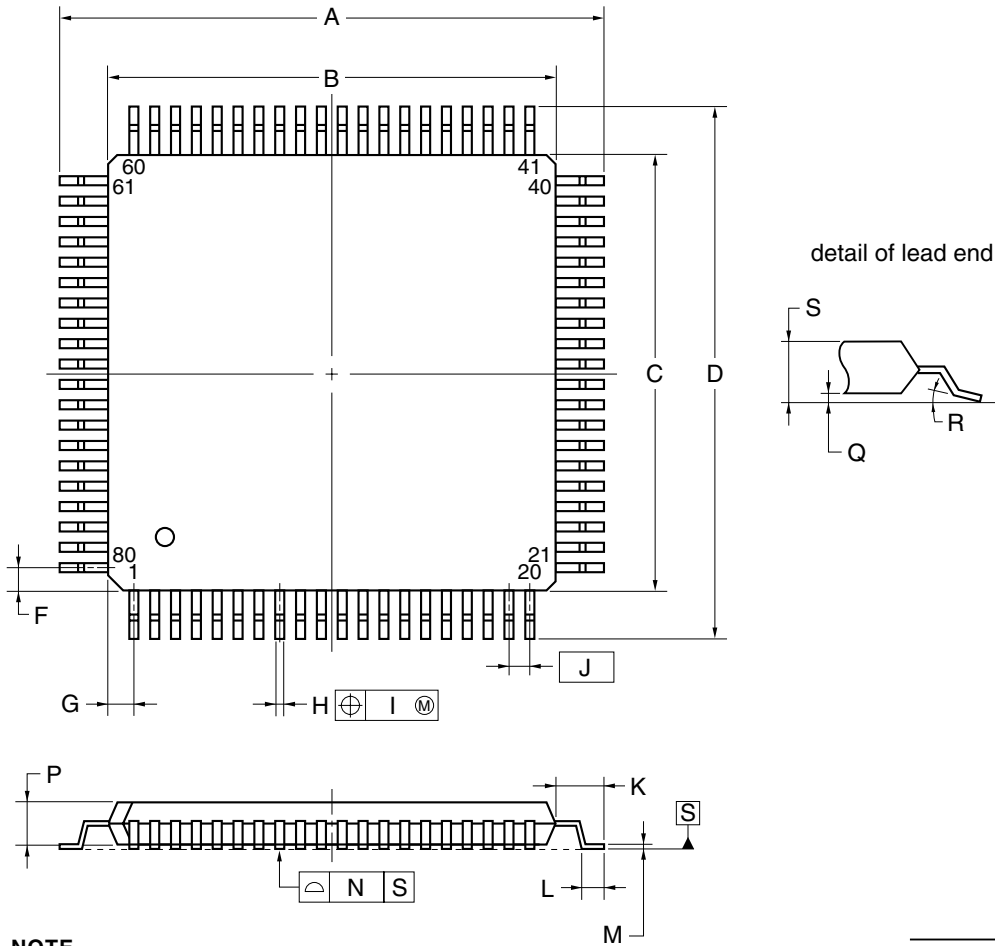


RESET Input Timing



12. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 17.20±0.20 |
| B | 14.00±0.20 |
| C | 14.00±0.20 |
| D | 17.20±0.20 |
| F | 0.825 |
| G | 0.825 |
| H | 0.32±0.06 |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.60±0.20 |
| L | 0.80±0.20 |
| M | 0.17 ^{+0.03} _{-0.07} |
| N | 0.10 |
| P | 1.40±0.10 |
| Q | 0.125±0.075 |
| R | 3° ^{+7°} _{-3°} |
| S | 1.70 MAX. |

P80GC-65-8BT-1

★ 13. RECOMMENDED SOLDERING CONDITIONS

The μPD780232 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions

μPD780232GC-xxx-8BT: 80-pin plastic QFP (14 × 14)

| Soldering | Soldering Conditions | Recommended Method Condition Symbol |
|-----------------|---|-------------------------------------|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less | IR35-00-2 |
| VPS | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less | VP15-00-2 |
| Wave soldering | Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | — |

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780232.

Also refer to **(6) Notes on using development tools**.

(1) Software Package

| | |
|--------|---|
| SP78K0 | Software package common to 78K/0 Series |
|--------|---|

(2) Language Processing Software

| | |
|----------|---|
| RA78K0 | Assembler package common to 78K/0 Series |
| CC78K0 | C compiler package common to 78K/0 Series |
| DF780233 | Device file for μPD780232 Subseries |
| CC78K0-L | C compiler library source file common to 78K/0 Series |

(3) Flash Memory Writing Tools

| | | |
|---|----------------------------------|---|
| ★ | Flashpro III (FL-PR3, PG-FP3) | Dedicated flash programmer for on-chip flash memory microcontrollers |
| | FA-80GC | Adapter for flash memory writing. Used by connecting to Flashpro III. • For 80-pin plastic QFP (GC-8BT type) |

(4) Debugging Tools

- **When in-circuit emulator IE-78K0-NS(-A) is used**

| | | |
|---|-------------------------------------|--|
| | IE-78K0-NS(-A) | In-circuit emulator common to 78K/0 Series |
| | IE-70000-MC-PS-B | Power supply unit for IE-78K0-NS |
| ★ | IE-78K0-NS-PA | Performance board to enhance/extend the functions of the IE-78K0-NS |
| | IE-70000-98-IF-C | Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported) |
| ★ | IE-70000-CD-IF-A | PC card and interface cable required when notebook-type PC is used as host machine (PCMCIA socket supported) |
| | IE-70000-PC-IF-C | Adapter required when IBM PC/AT™ compatible is used as host machine (ISA bus supported) |
| ★ | IE-70000-PCI-IF-A | Adapter required when PC incorporating PCI bus is used as host machine |
| ★ | IE-780233-NS-EM4, IE-78K0-NS-P01 | Emulation board and I/O board to emulate the μPD780232 Subseries |
| ★ | NP-80GC | Emulation probe for 80-pin plastic QFP (GC-8BT type) |
| ★ | NP-80GC-TQ | |
| ★ | NP-H80GC-TQ | |
| | EV-9200GC-80 | Conversion socket to connect the NP-80GC and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted |
| ★ | TGC-080SBP | Conversion adapter to connect the NP-80GC-TQ or NP-H80GC-TQ and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted |
| | ID78K0-NS | Integrated debugger for IE-78K0-NS |
| | SM78K0 | System simulator common to 78K/0 Series |
| | DF780233 | Device file for μPD780232 Subseries |

• When in-circuit emulator IE-78001-R-A is used

| | | |
|---|-------------------------------------|--|
| | IE-78001-R-A | In-circuit emulator common to 78K/0 Series |
| ★ | IE-70000-98-IF-C | Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported) |
| ★ | IE-70000-PC-IF-C | Adapter required when IBM PC/AT compatible is used as host machine (ISA bus supported) |
| ★ | IE-70000-PCI-IF-A | Adapter required when PC incorporating PCI bus is used as host machine |
| | IE-70000-R-SV3 | Interface adapter and cable required when EWS is used as host machine |
| ★ | IE-780233-NS-EM4, IE-78K0-NS-P01 | Emulation board and I/O board to emulate the μPD780232 Subseries |
| | IE-78K0-R-EX1 | Emulation probe conversion board required when using IE-780232-NS-EM1 on IE-78001-R-A |
| | EP-78230GC-R | Emulation probe for 80-pin plastic QFP (GC-8BT type) |
| | EV-9200GC-80 | Conversion socket to connect the EP-78230GC-R and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted |
| | ID78K0 | Integrated debugger for IE-78001-R-A |
| | SM78K0 | System simulator common to 78K/0 Series |
| | DF780233 | Device file for μPD780232 Subseries |

(5) Real-Time OSs

| | | |
|--|--------|-------------------------------|
| | RX78K0 | Real-time OS for 78K/0 Series |
| | MX78K0 | OS for 78K/0 Series |

★ (6) Notes on using development tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780233.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780233.
- The FL-PR3, FA-80GC, NP-80GC, NP-80GC-TQ, and NP-H80GC-TQ are products of Naito Densai Machida Mfg. Co., Ltd (+81-45-475-4191).
- The TGK-080SBP is a product made by TOKYO ELETECH CORPORATION.
For further information, contact: Daimaru Kogyo, Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OS suitable for each software are as follows:

| Host Machine [OS] Software | PC | EWS |
|----------------------------------|---|---|
| | PC-9800 series [Japanese Windows™] IBM PC/AT compatibles [Japanese/English Windows] | HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] |
| RA78K0 | √ Note | √ |
| CC78K0 | √ Note | √ |
| ID78K0-NS | √ | — |
| ID78K0 | √ | — |
| SM78K0 | √ | — |
| RX78K0 | √ Note | √ |
| MX78K0 | √ Note | √ |

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

| Document Name | Document No. |
|--|--------------|
| μPD780232 Subseries User's Manual | U13364E |
| μPD780232 Data Sheet | This manual |
| μPD78F0233 Data Sheet | U13322E |
| 78K/0 Series Instructions User's Manual | U12326E |
| ★ 78K/0, 78K/0S Series Flash Memory Write Application Note | U14458E |

★ **Documents Related to Development Tools (User's Manuals)**

| Document Name | Document No. | |
|--|---|---------|
| RA78K0 Assembler Package | Operation | U14445E |
| | Language | U14446E |
| | Structured Assembly Language | U11789E |
| CC78K0 C Compiler | Operation | U14297E |
| | Language | U14298E |
| PG-FP3 Flash Memory Programmer | U13502E | |
| IE-78K0-NS In-Circuit Emulator | U13731E | |
| IE-78K0-NS-A In-Circuit Emulator | U14889E | |
| IE-78001-R-A In-Circuit Emulator | U14142E | |
| IE-78K0-R-EX1 In-Circuit Emulator | To be prepared | |
| IE-780233-NS-EM4 Emulation Board | U14666E | |
| EP-78230 Emulation Probe | EEU-1515 | |
| SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based | Operation | U14611E |
| SM78K Series System Simulator Ver. 2.10 or Later | External Parts User Open Interface Specifications | U15006E |
| ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based | Operation | U14379E |
| ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based | Operation | U14910E |
| ID78K0 Integrated Debugger Windows Based | Guide | U11649E |
| | Reference | U11539E |

Documents Related to Embedded Software (User's Manuals)

| Document Name | | Document No. |
|---------------------------|--------------|--------------|
| 78K/0 Series Real-time OS | Fundamentals | U11537E |
| | Installation | U11536E |
| 78K/0 Series OS MX78K0 | Fundamentals | U12257E |

Other Documents

| Document Name | Document No. |
|--|--------------|
| SEMICONDUCTOR SELECTION GUIDE - Products & Package - (CD-ROM) | X13769E |
| Semiconductor Device Mounting Technology Manual | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892E |

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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