NEC

MOS INTEGRATED CIRCUIT

μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), 780988(A)

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), and 780988(A) are members of the μPD780988 Subseries of the 78K/0 Series. These microcontrollers are suitable for general-purpose inverter control.

The μPD780988 Subseries provides expanded internal ROM and RAM capacities as well as inverter control, timers, and serial interfaces.

The μPD780982(A), 780983(A), 780984(A), 780986(A), and 780988(A) are applied a stricter quality assurance program than the μPD780982, 780983, 780984, 780986, and 780988 (standard grade) (NEC classifies these products as special grade in its quality grade classification).

A flash memory version, the μPD78F0988, which can operate within the same power supply voltage range as the mask ROM version, and various development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780988 Subseries User's Manual: U13029E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- On-chip ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	Internal Expansion RAM	
μPD780982, 780982(A)	16 KB	1024 bytes	None	• 64-pin plastic SDIP (19.05 mm (750))[Note] • 64-pin plastic QFP (14 × 14)
μPD780983, 780983(A)	24 KB			
μPD780984, 780984(A)	32 KB			
μPD780986, 780986(A)	48 KB		1024 bytes	
μPD780988, 780988(A)	60 KB			

Note Only for standard-grade products

- External memory expansion space: 256 bytes (except μPD780988 and 780988(A))
- Minimum instruction execution time: 0.24 μs (@ f_X = 8.38 MHz operation)
- I/O ports: 47
- Timer outputs for 10-bit inverter control: 6
- 8-bit real-time output ports: 8
- 10-bit resolution A/D converter: 8 channels
- Serial interface: 3 channels
- Timer: 7 channels
- Power supply voltage: V_{DD} = 4.0 to 5.5 V

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Printed in Japan

The mark ★ shows major revised points.

APPLICATIONS

Motor control for inverter-type air conditioners, washing machines, refrigerators, etc.

ORDERING INFORMATION

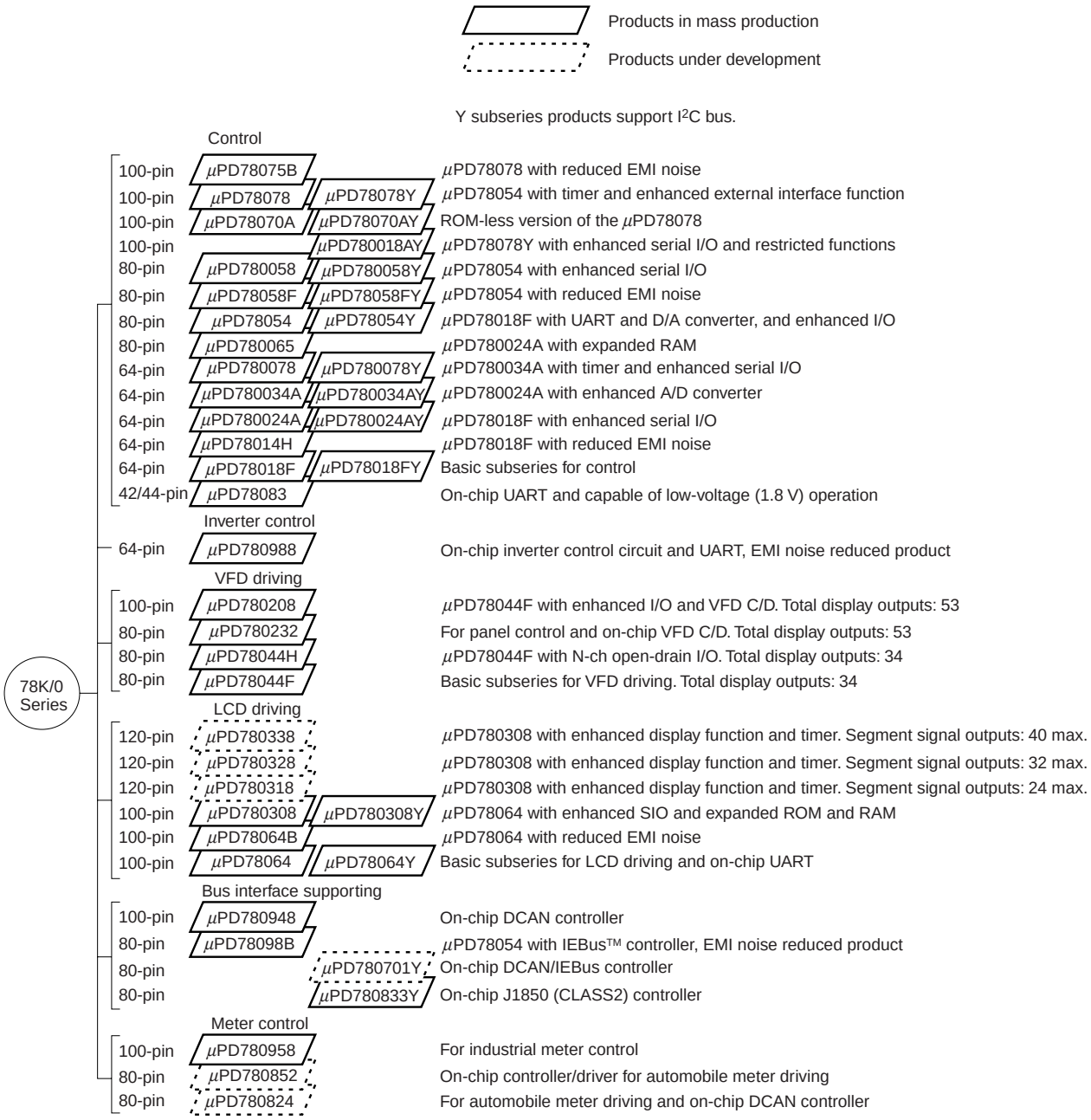
Part Number	Package	Quality Grade
μPD780982CW-×××	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electronic equipment)
μPD780983CW-×××	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electronic equipment)
μPD780984CW-×××	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electronic equipment)
μPD780986CW-×××	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electronic equipment)
μPD780988CW-×××	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electronic equipment)
μPD780982GC-×××-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electronic equipment)
μPD780983GC-×××-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electronic equipment)
μPD780984GC-×××-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electronic equipment)
μPD780986GC-×××-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electronic equipment)
μPD780988GC-×××-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electronic equipment)
μPD780982GC(A)-×××-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical machinery and apparatus)
μPD780983GC(A)-×××-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical machinery and apparatus)
μPD780984GC(A)-×××-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical machinery and apparatus)
μPD780986GC(A)-×××-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical machinery and apparatus)
μPD780988GC(A)-×××-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical machinery and apparatus)

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Yes
	μPD78078	48 K to 60 K											
	μPD78070A	—									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							—	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			—	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	—					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		—	—					1 ch (UART: 1 ch)	33		—
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	—	1 ch	—	8 ch	—	3 ch (UART: 2 ch)	47	4.0 V	Yes
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780232	16 K to 24 K	3 ch	—	—		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	—	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	—
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	—	—	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	—	—	3 ch (UART: 1 ch)	79	4.0 V	Yes
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	—
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	—	1 ch	—	—	—	2 ch (UART: 1 ch)	69	2.2 V	—
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	—	—	3 ch (UART: 1 ch)	56	4.0 V	—
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD780982 μPD780982(A)	μPD780983 μPD780983(A)	μPD780984 μPD780984(A)	μPD780986 μPD780986(A)	μPD780988 μPD780988(A)
Internal memory	ROM	16 KB	24 KB	32 KB	48 KB	60 KB
	High-speed RAM	1024 bytes				
	Expansion RAM	None			1024 bytes	
Memory space		64 KB				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		On-chip minimum instruction execution time variable function 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38 MHz operation with system clock)				
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.				
I/O ports		Total: 47 • CMOS inputs: 8 • CMOS I/O: 39				
Real-time output ports		• 8 bits × 1 or 4 bits × 2 • 6 bits × 1 or 4 bits × 1				
A/D converter		• 10-bit resolution × 8 channels • Power supply voltage: AV_{DD} = 4.0 to 5.5 V				
Serial interfaces		• UART mode: 2 channels • 3-wire serial I/O mode: 1 channel				
Timers		• 16-bit timer/event counter: 2 channels • 8-bit timer/event counter: 3 channels • 10-bit inverter control timer: 1 channel • Watchdog timer: 1 channel				
Timer output		11 (General-purpose output: 5, inverter control output: 6)				
Vectored interrupt sources	Maskable	Internal: 16, external: 8				
	Non-maskable	Internal: 1				
	Software	1				
Power supply voltage		V_{DD} = 4.0 to 5.5 V				
Operating ambient temperature		T_A = –40 to +85°C				
Package		• 64-pin plastic SDIP (19.05 mm (750))[Note] • 64-pin plastic QFP (14 × 14)				

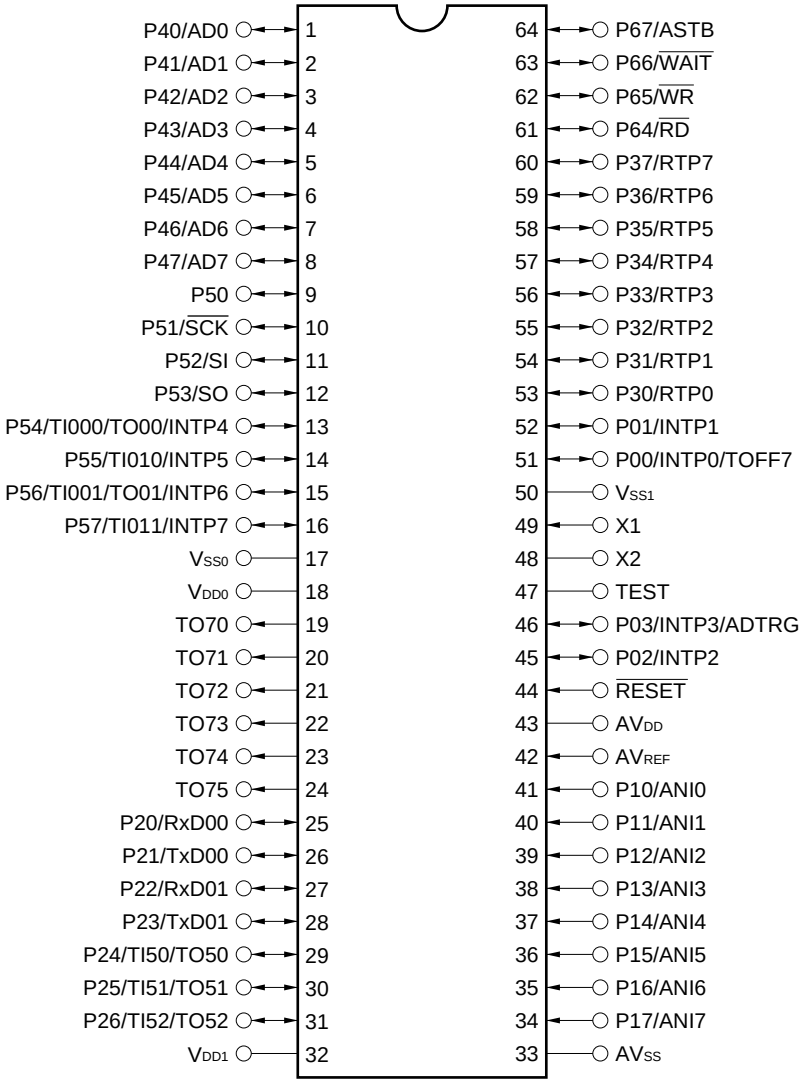
Note Only for standard-grade products

CONTENTS

1. PIN CONFIGURATION (Top View)

- **64-Pin Plastic SDIP (19.05 mm (750))**

  μPD780982CW-×××, 780983CW-×××, 780984CW-×××, 780986CW-×××, 780988CW-×××

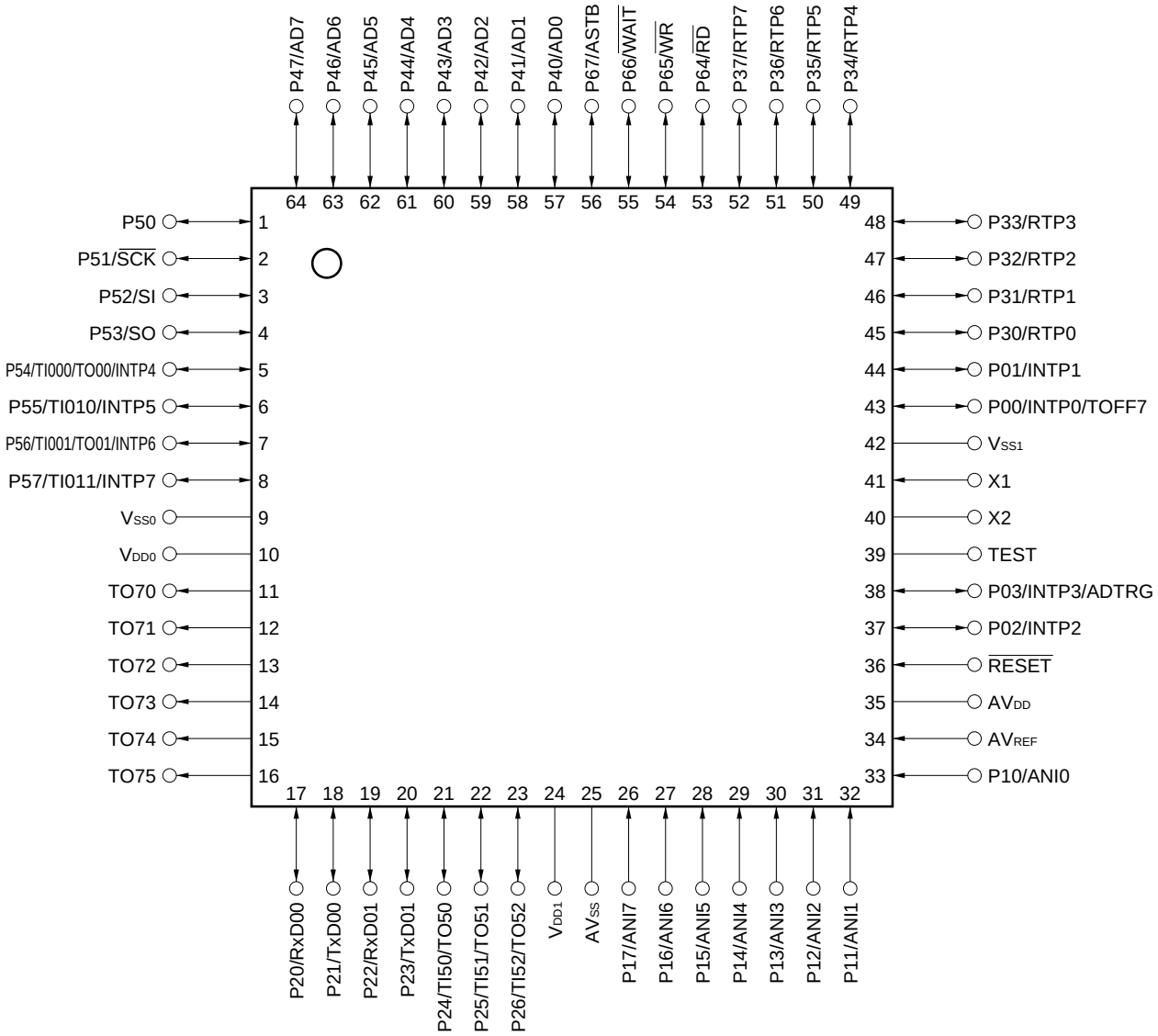


Cautions 1. Connect the TEST pin directly to V_{SS0}.

★ **2. The 64-pin plastic SDIP (19.05 mm (750)) package is not supported for special quality grade products.**

Remark When the μPD780982, 780983, 780984, 780986, and 780988 are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-Pin Plastic QFP (14 × 14 mm)**
  μPD780982GC-×××-AB8, 780983GC-×××-AB8, 780984GC-×××-AB8, 780986GC-×××-AB8, 780988GC-×××-AB8
  μPD780982GC(A)-×××-AB8, 780983GC(A)-×××-AB8, 780984GC(A)-×××-AB8, 780986GC(A)-×××-AB8,
  μPD780988GC(A)-×××-AB8

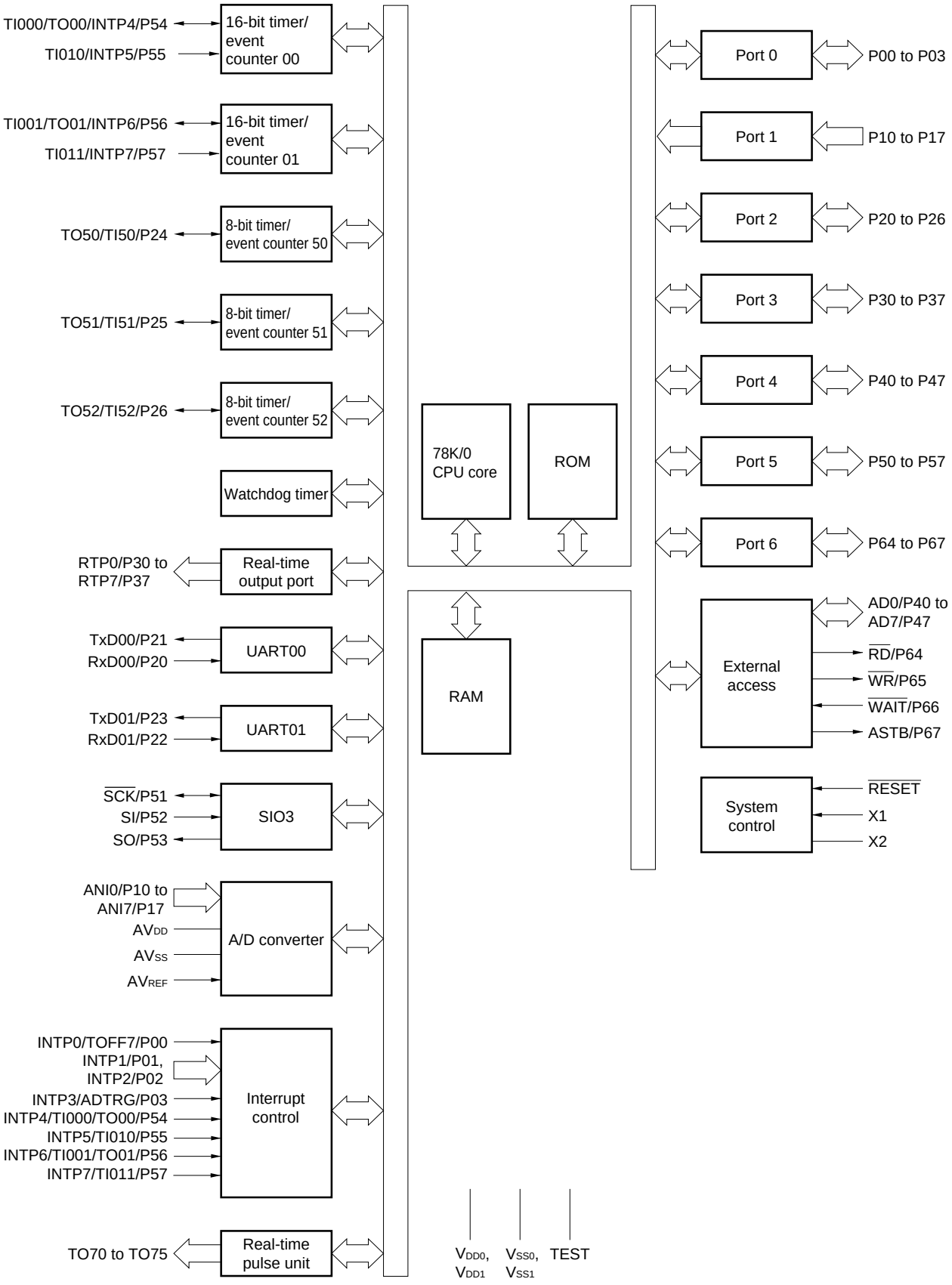


Caution Connect the TEST pin directly to V_{SS0}.

Remark When the μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), and 780988(A) are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

AD0 to AD7:	Address/data bus	RxD00, RxD01:	Receive data
ADTRG:	AD trigger input	$\overline{SCK}$:	Serial clock
ANI0 to ANI7:	Analog input	SI:	Serial input
ASTB:	Address strobe	SO:	Serial output
AV_{DD}:	Analog power supply	TEST:	Test
AV_{REF}:	Analog reference voltage	TI000, TI001,	
AV_{SS}:	Analog ground	TI010, TI011,	
INTP0 to INTP7:	External interrupt input	TI50 to TI52:	Timer input
P00 to P03:	Port 0	TO00, TO01,	
P10 to P17:	Port 1	TO50 to TO52,	
P20 to P26:	Port 2	TO70 to TO75:	Timer output
P30 to P37:	Port 3	TOFF7:	Timer output off
P40 to P47:	Port 4	TxD00, TxD01:	Transmit data
P50 to P57:	Port 5	V_{DD0}, V_{DD1}:	Power supply
P64 to P67:	Port 6	V_{SS0}, V_{SS1}:	Ground
$\overline{RD}$:	Read strobe	$\overline{WAIT}$:	Wait
$\overline{RESET}$:	Reset	$\overline{WR}$:	Write strobe
RTP0 to RTP7:	Real-time port	X1, X2:	Crystal

2. BLOCK DIAGRAM



Remark Internal ROM and RAM capacities vary depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	INTP0/TOFF7
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1. 8-bit input-only port.	Input	ANI0 to ANI7
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	RxD00
P21				TxD00
P22				RxD01
P23				TxD01
P24				TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	AD0 to AD7
P50	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. LEDs can be driven directly. An on-chip pull-up resistor can be specified by means of software.	Input	—
P51				$\overline{SCK}$
P52				SI
P53				SO
P54				INTP4/TI000/TO00
P55				INTP5/TI010
P56				INTP6/TI001/TO01
P57				INTP7/TI011
P64	I/O	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
INTP4			Input	P54/TI000/TO00
INTP5			Input	P55/TI010
INTP6			Input	P56/TI001/TO01
INTP7			Input	P57/TI011
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P24/TO50
TI51		External count clock input to 8-bit timer/event counter 51	Input	P25/TO51
TI52		External count clock input to 8-bit timer/event counter 52	Input	P26/TO52
TI000		External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture register (CR000, CR010) of 16-bit timer/event counter 00	Input	P54/INTP4/TO00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00	Input	P55/INTP5
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture register (CR001, CR011) of 16-bit timer/event counter 01	Input	P56/INTP6/TO01
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01	Input	P57/INTP7
TO50	Output	8-bit timer/event counter 50 output	Input	P24/TI50
TO51		8-bit timer/event counter 51 output	Input	P25/TI51
TO52		8-bit timer/event counter 52 output	Input	P26/TI52
TO00		16-bit timer/event counter 00 output	Input	P54/INTP4/TI000
TO01		16-bit timer/event counter 01 output	Input	P56/INTP6/TI001
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals from the real-time pulse unit	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input	Input	P20
RxD01			Input	P22
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P51
SI	Input	Serial interface serial data input	Input	P52
SO	Output	Serial interface serial data output	Input	P53
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control	Hi-Z	—
TOFF7	Input	Timer output (TO70 to TO75) stop external input	Input	P00/INTP0
AD0 to AD7	I/O	Address/data bus for expanding memory externally	Input	P40 to P47
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory	Input	P65

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67
AV_{REF}	Input	A/D converter reference voltage input	—	—
AV_{DD}	–	A/D converter analog power supply	—	—
AV_{SS}	–	A/D converter ground potential	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for system clock oscillation	—	—
X2	–		—	—
V_{DD0}	–	Positive power supply for ports	—	—
V_{SS0}	–	Ground potential for ports	—	—
V_{DD1}	–	Positive power supply (except ports)	—	—
V_{SS1}	–	Ground potential (except ports)	—	—
TEST	–	Test mode set pin. Connect directly to V_{SS0}.	—	—

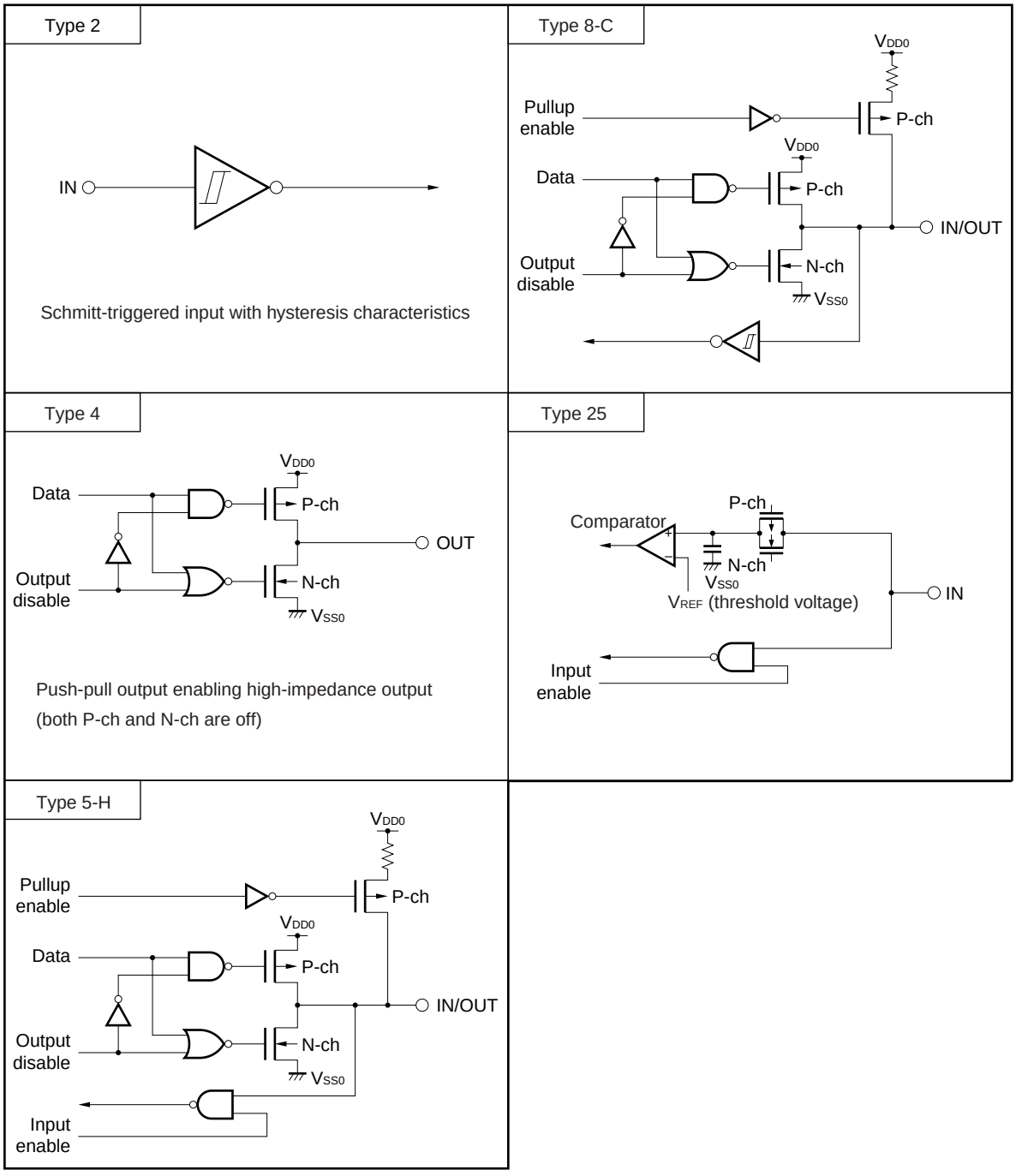
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0/TOFF7	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
P01/INTP1			
P02/INTP2			
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/RxD00	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/TxD00	5-H		
P22/RxD01	8-C		
P23/TxD01	5-H		
P24/TI50/TO50	8-C		
P25/TI51/TO51			
P26/TI52/TO52			
P30/RTP0 to P37/RTP7	5-H		
P40/AD0 to P47/AD7			
P50			
P51/$\overline{SCK}$	8-C		
P52/SI	5-H		
P53/SO			
P54/INTP4/TI000/TO00			
P55/INTP5/TI010			
P56/INTP6/TI001/TO01			
P57/INTP7/TI011			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
TO70 to TO75	4	Output	Leave open.
$\overline{RESET}$	2	Input	—
AV_{DD}	—	—	Connect to V_{DD0}.
AV_{REF}			Connect to V_{SS0}.
AV_{SS}			
TEST			Connect directly to V_{SS0}.

Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), and 780988(A) is shown in Figures 4-1 through 4-5.

Figure 4-1. Memory Map (μPD780982, 780982(A))

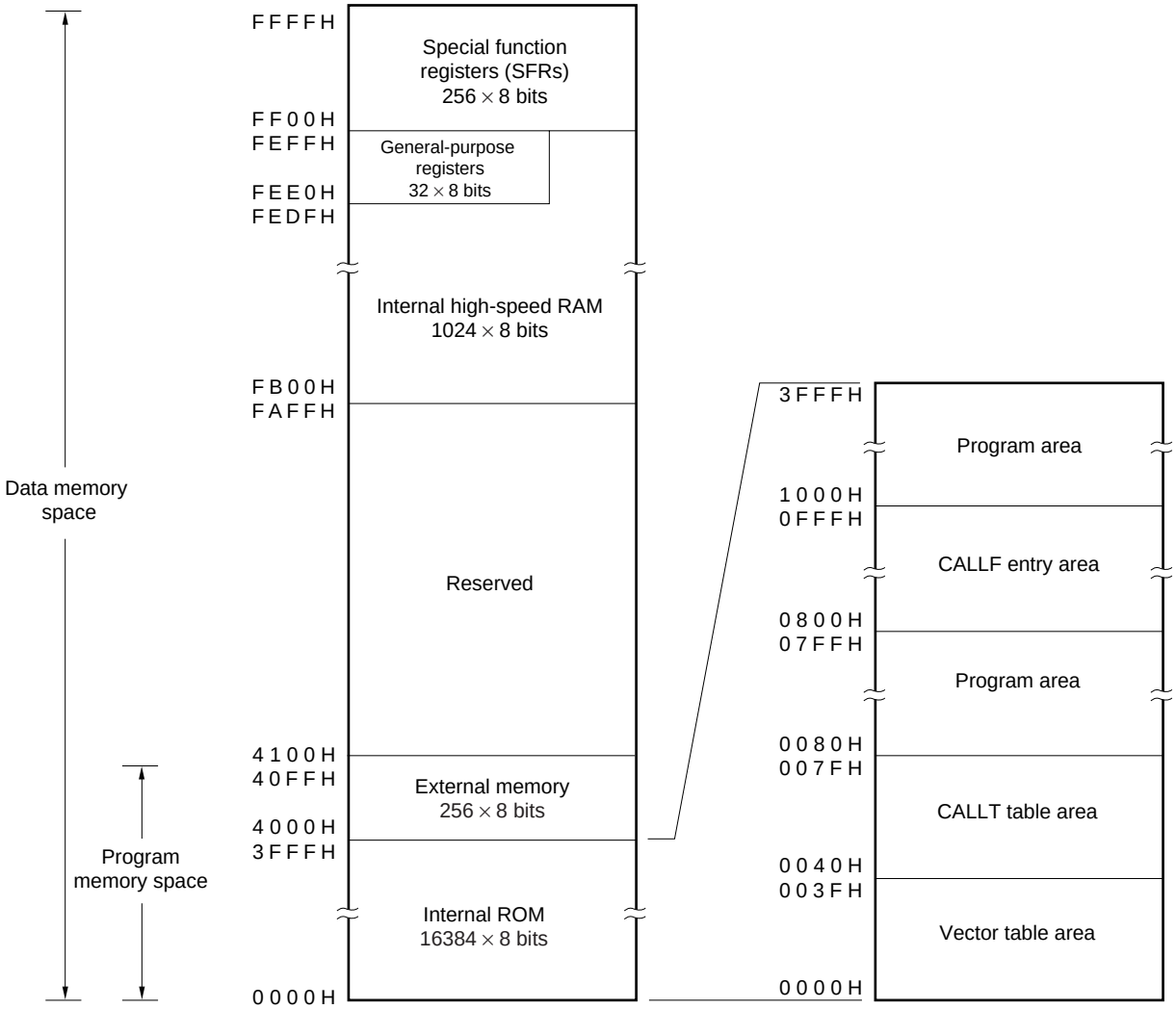


Figure 4-2. Memory Map (μPD780983, 780983(A))

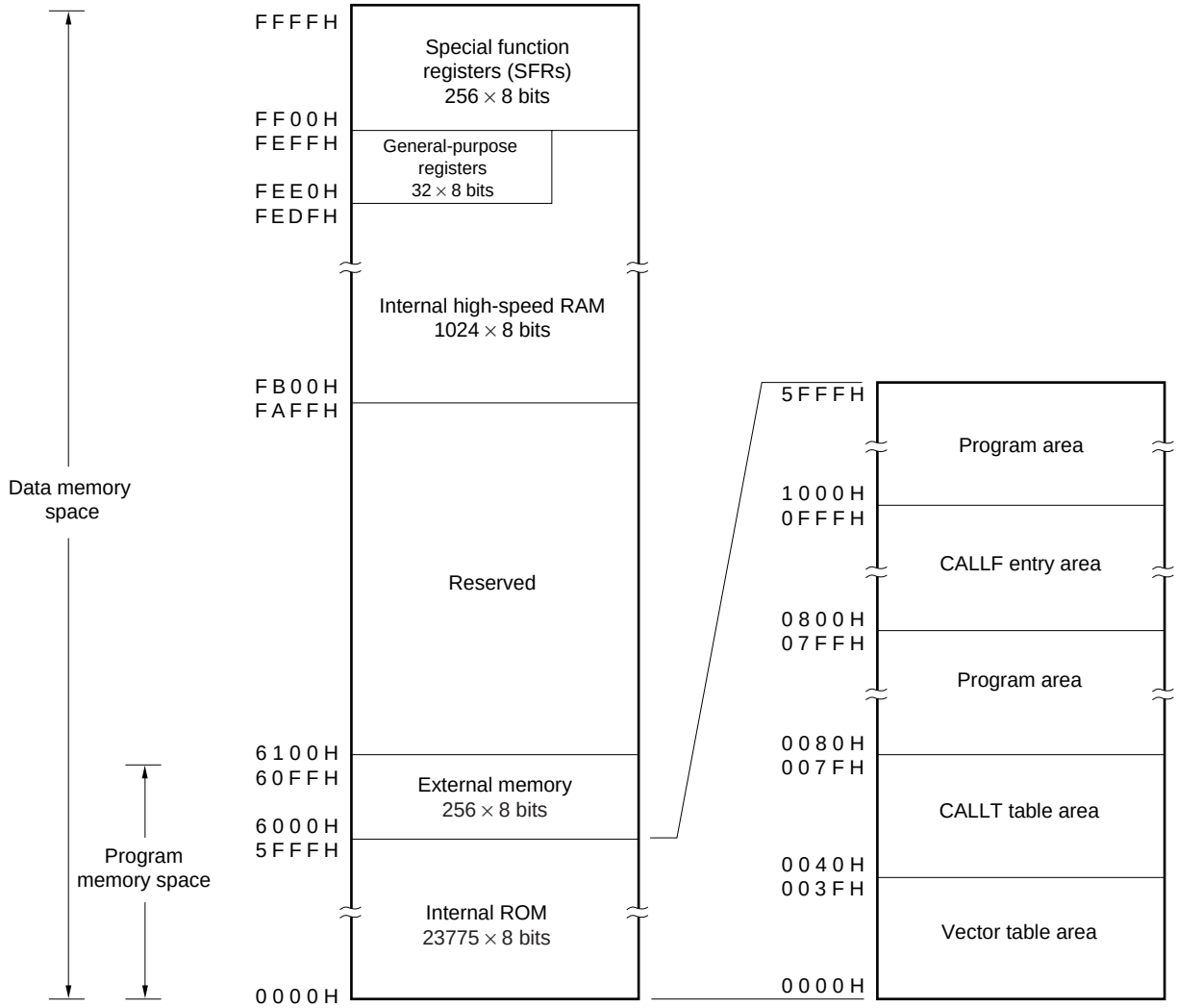


Figure 4-3. Memory Map (μPD780984, 780984(A))

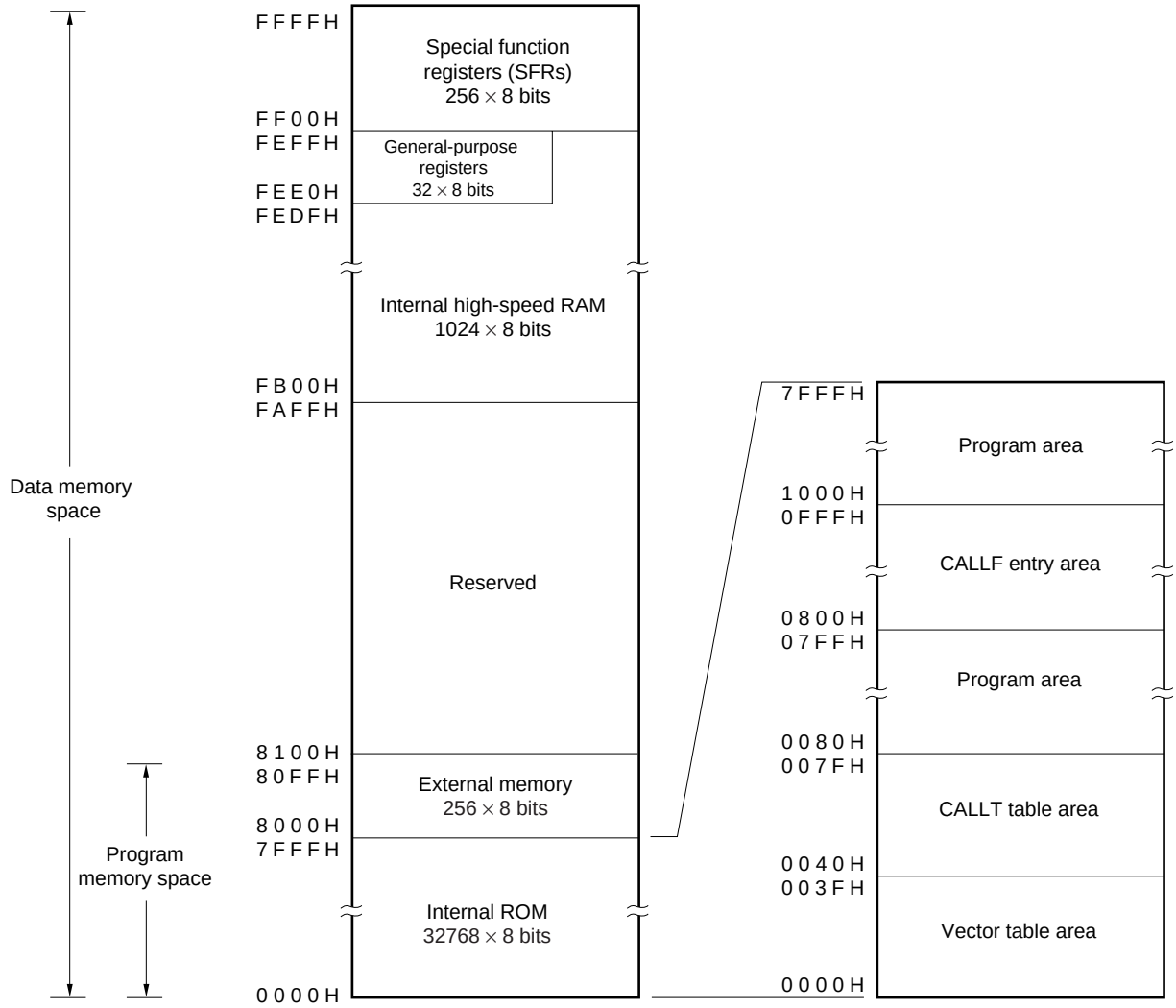


Figure 4-4. Memory Map (μPD780986, 780986(A))

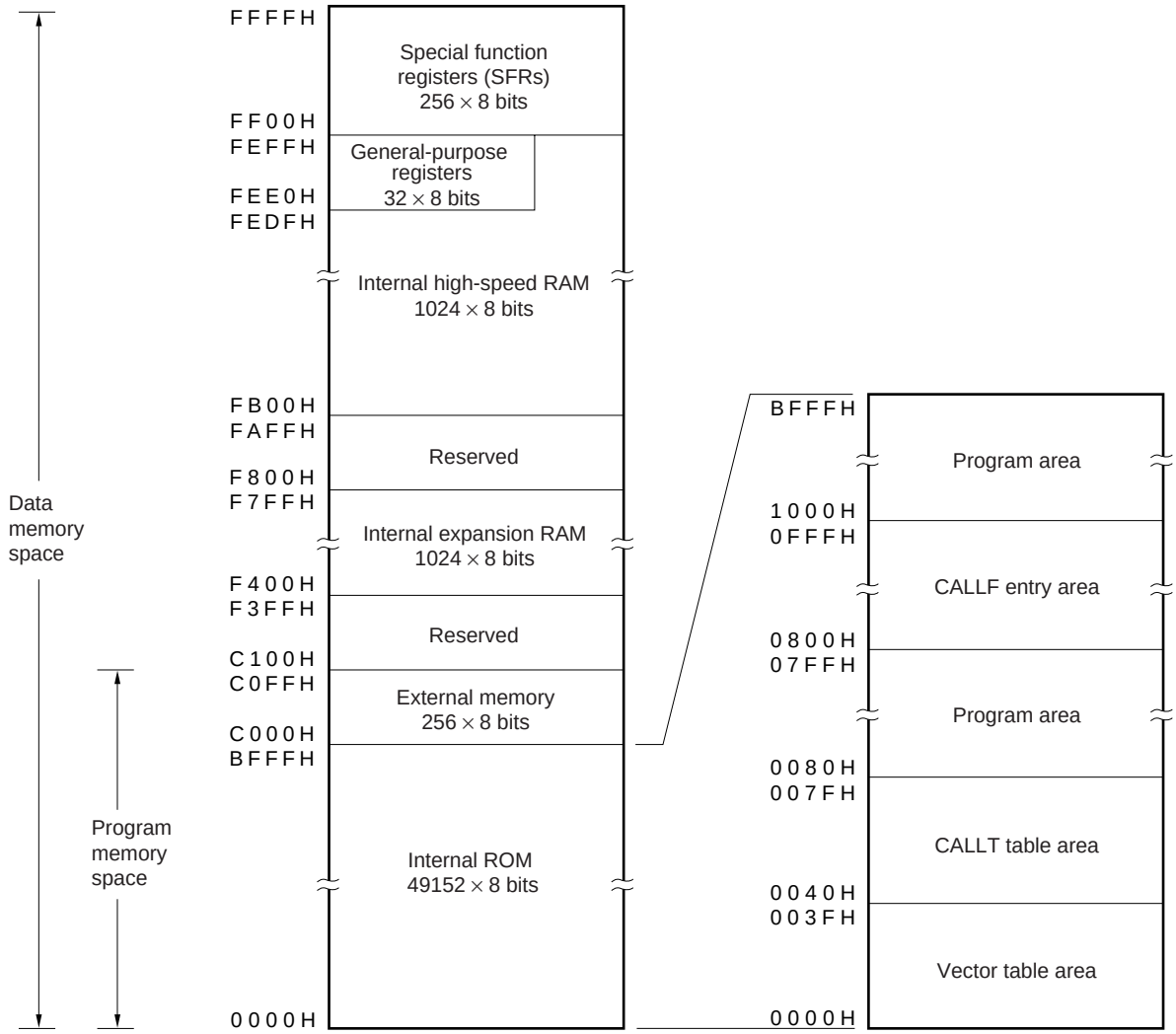
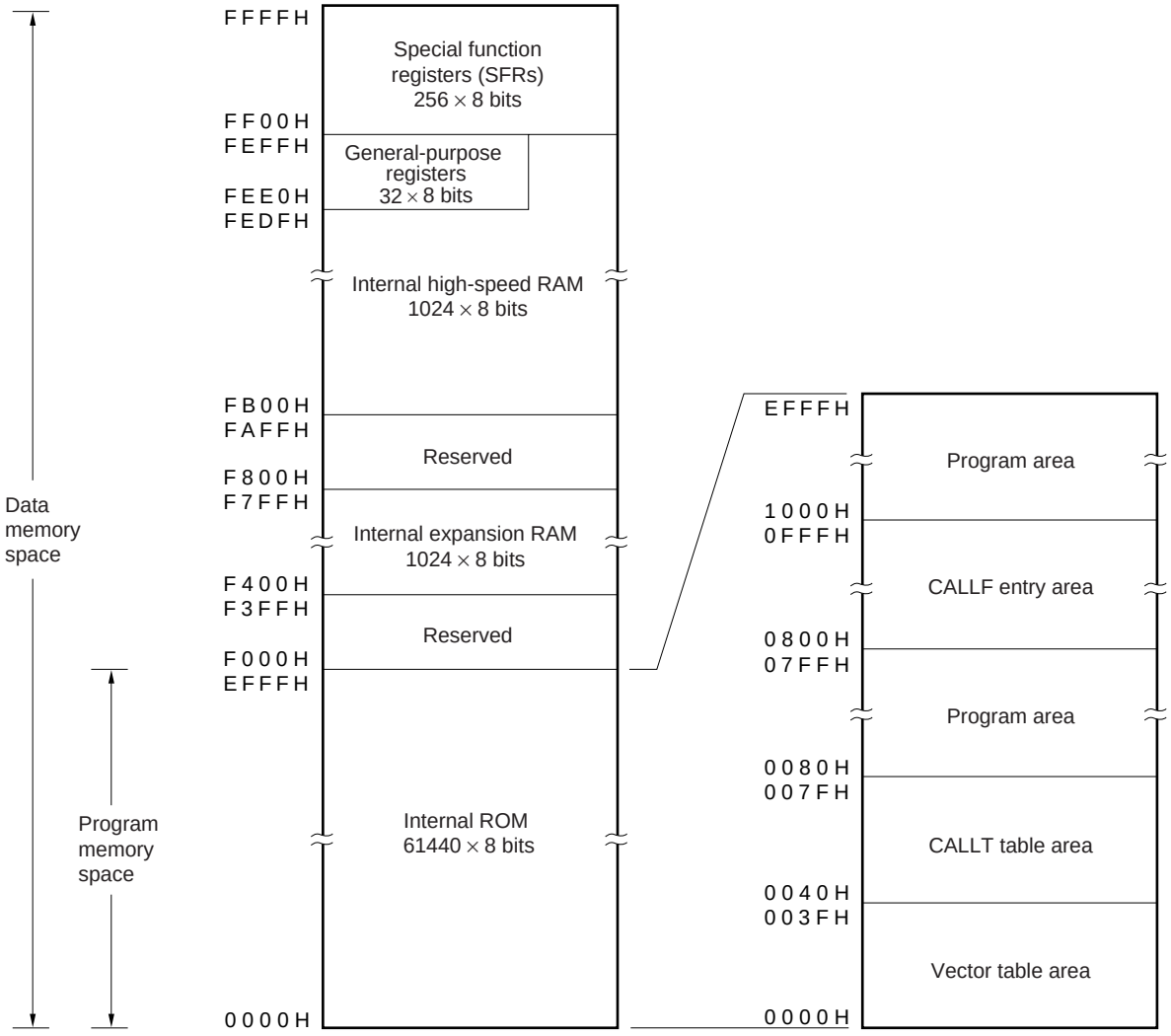


Figure 4-5. Memory Map (μPD780988, 780988(A))



5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following two types of I/O ports are available.

- CMOS input (Port 1): 8
- CMOS I/O (Port 0, ports 2 to 6): 39

Total: 47

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P03	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 1	P10 to P17	Input-only port.
Port 2	P20 to P26	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 3	P30 to P37	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.
Port 6	P64 to P67	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.

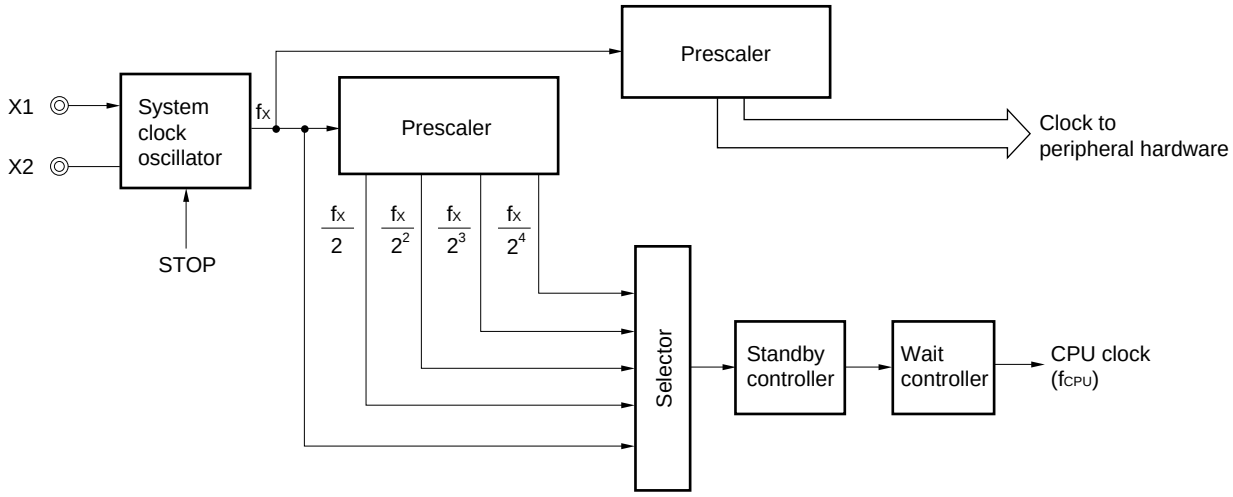
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38 MHz operation with system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counters

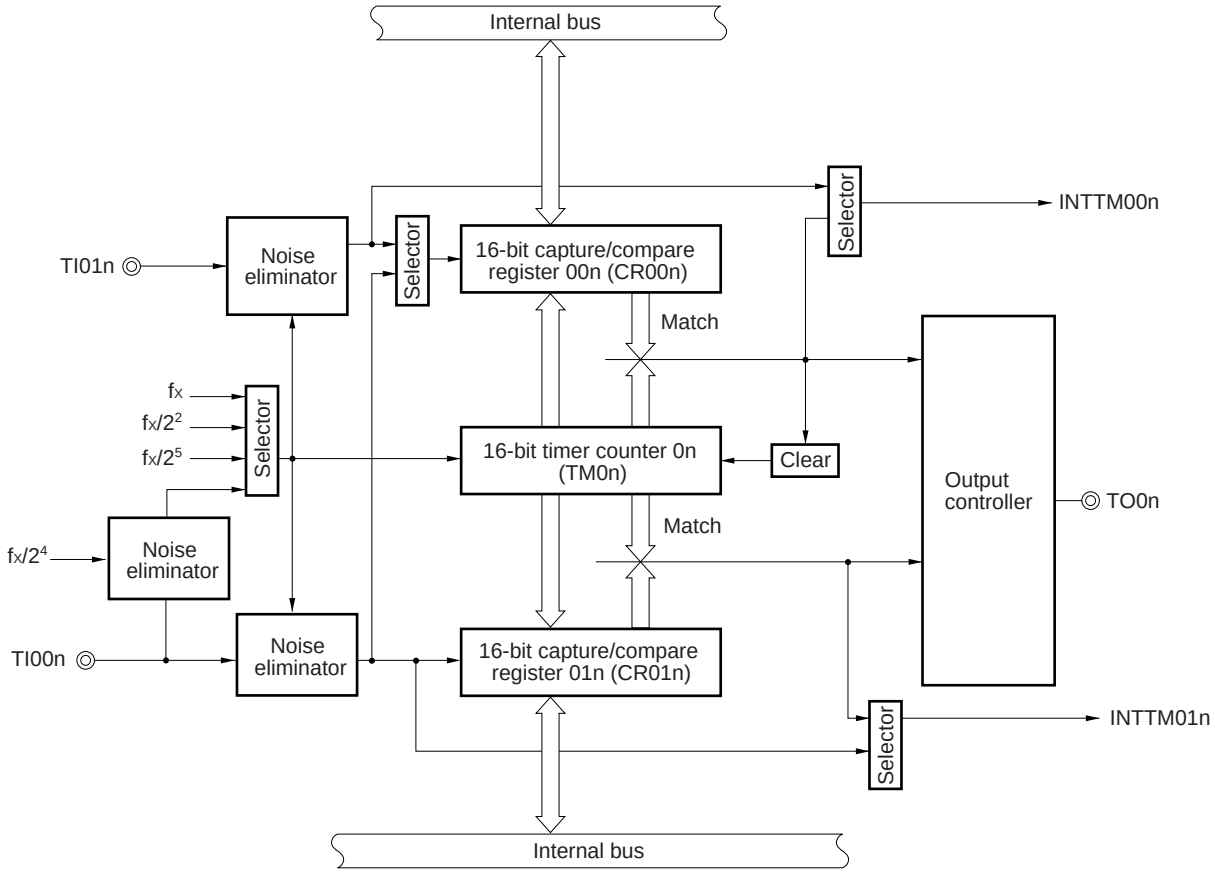
Seven timer/event counter channels are incorporated.

- 16-bit timer/event counter: 2 channels
- 8-bit timer/event counter: 3 channels
- 10-bit inverter control timer: 1 channel
- Watchdog timer: 1 channel

★ **Table 5-2. Operations of Timer/Event Counters**

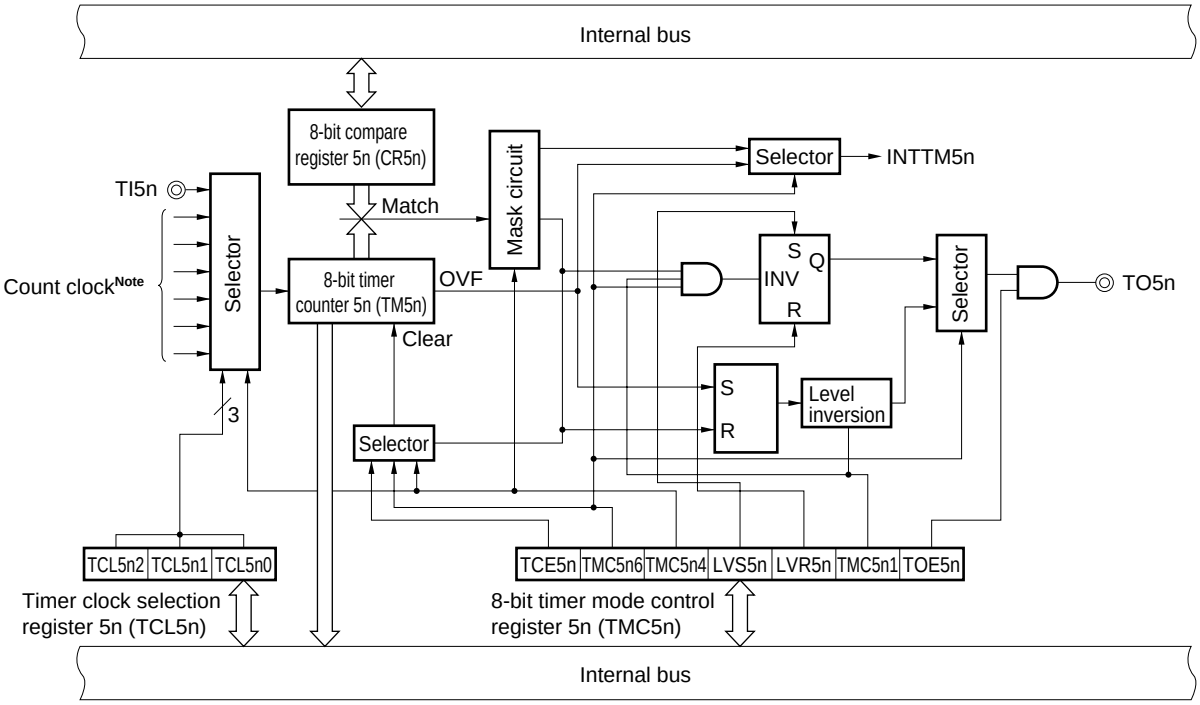
		16-Bit Timer/Event Counter	8-Bit Timer/Event Counter	10-Bit Inverter Control Timer	Watchdog Timer
Operation Mode	Interval timer	2 channels	3 channels	1 channel	1 channel
	External event counter	2 channels	3 channels	—	—
Function	Timer output	2 outputs	3 outputs	6 outputs	—
	PWM output	—	3 outputs	—	—
	PPG output	2 outputs	—	—	—
	Pulse width measurement	4 inputs	—	—	—
	Square wave output	2 outputs	3 outputs	—	—
	Interrupt requests	4	3	1	1

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter



Remark n = 0, 1

Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter



Note Count clock differs depending on the timer.

TM50: $f_X/2$, $f_X/2^3$, $f_X/2^5$, $f_X/2^7$, $f_X/2^9$, $f_X/2^{11}$

TM51: f_X, $f_X/2$, $f_X/2^2$, $f_X/2^3$, $f_X/2^4$, $f_X/2^5$

TM52: $f_X/2^4$, $f_X/2^5$, $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, $f_X/2^9$

Remark n = 0 to 2

Figure 5-4. Block Diagram of 10-Bit Inverter Control Timer

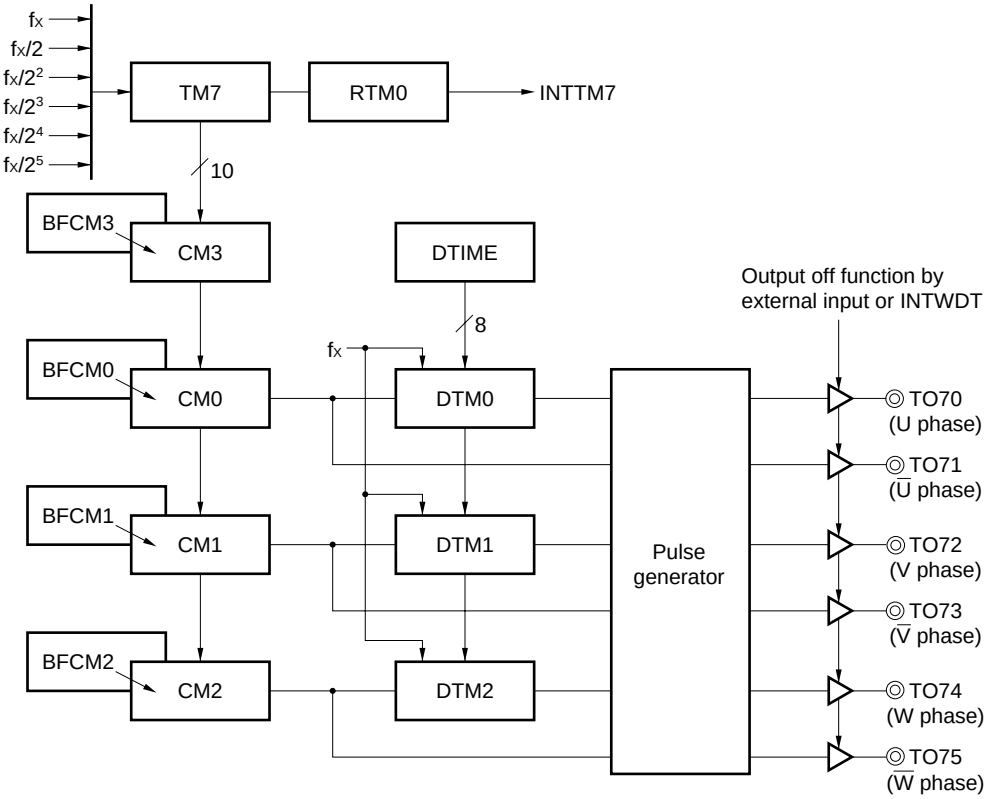
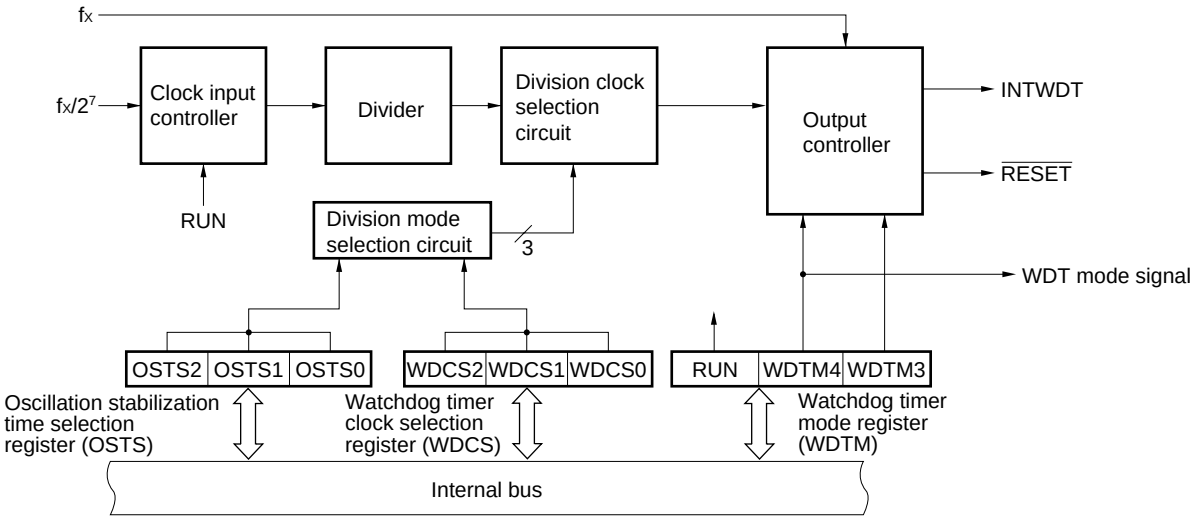


Figure 5-5. Watchdog Timer Block Diagram



5.4 Real-Time Output Ports

The following 2-channel real-time output port is incorporated.

- 8 bits × 1 or 4 bits × 2 … Real-time output port 0
- 6 bits × 1 or 4 bits × 1 … Real-time output port 1

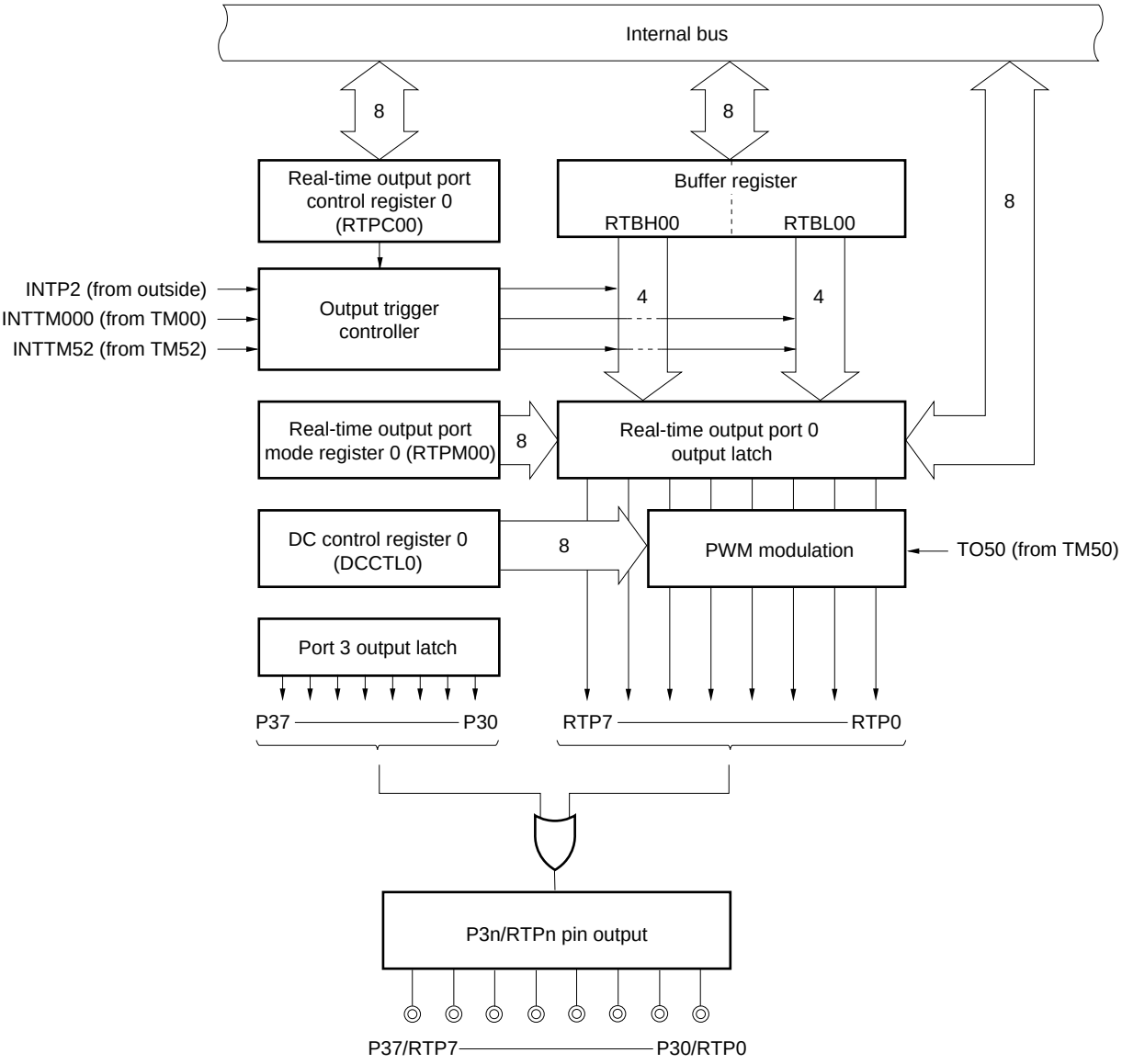
The real-time output port outputs data stored in buffers in synchronization with timer match interrupts or external interrupts, enabling pulse outputs without jitter.

Therefore, the real-time output port is suitable for applications in which any patterns are output at any interval, such as the open loop control of a stepper motor.

Furthermore PWM modulation can be applied to a specific pin for the output pattern.

Figure 5-6. Real-Time Output Port Block Diagram (1/2)

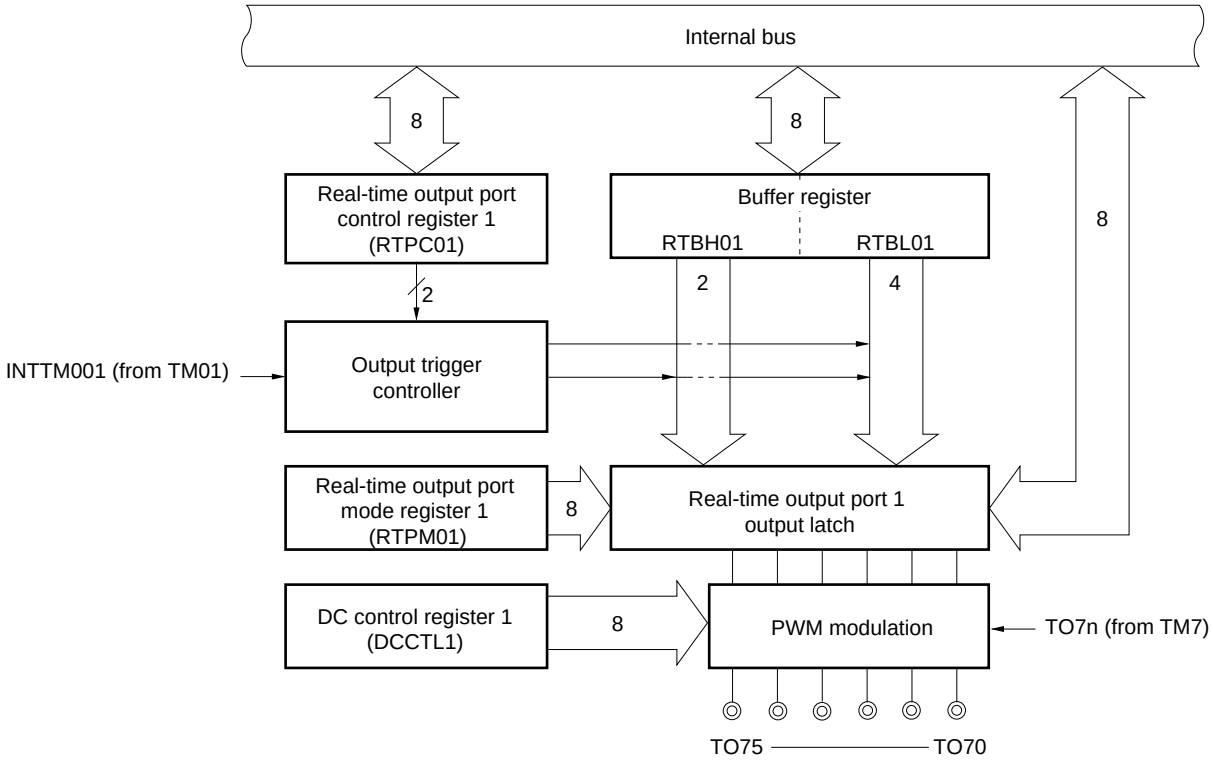
(a) Real-time output port 0 (8 bits × 1 or 4 bits × 2)



Remark n = 0 to 7

Figure 5-6. Real-Time Output Port Block Diagram (2/2)

(b) Real-time output port 1 (6 bits × 1 or 4 bits × 1)



Remark n = 0 to 5

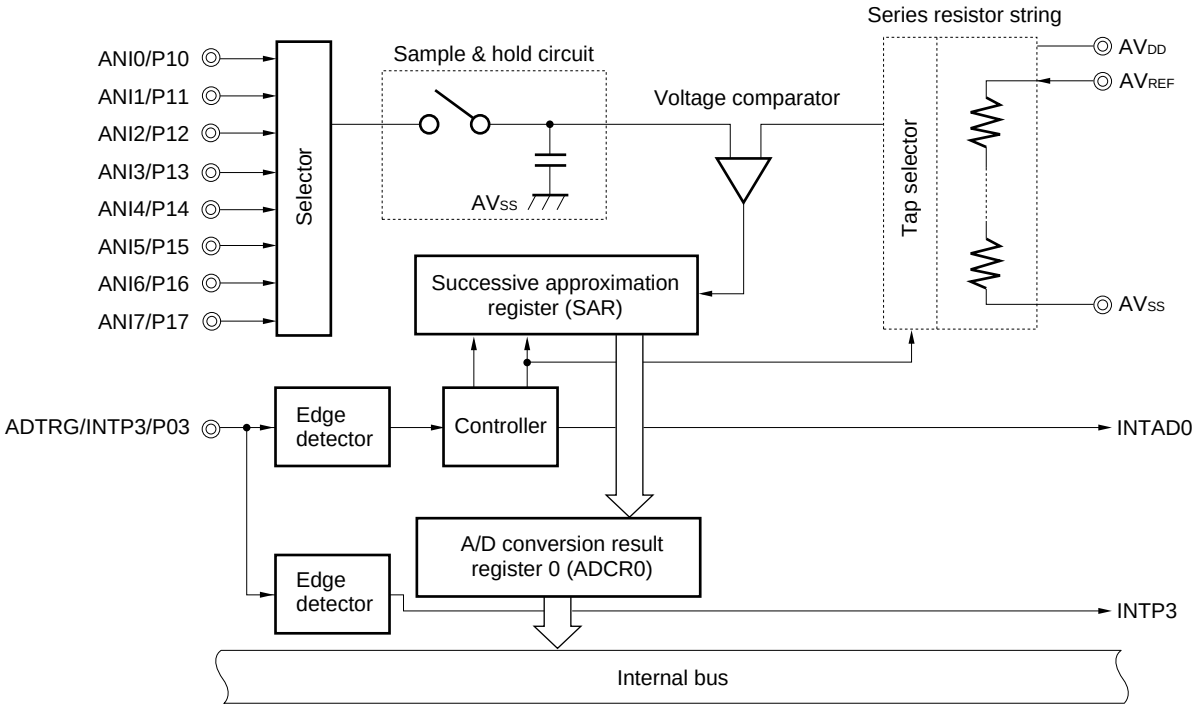
5.5 A/D Converter

An A/D converter consisting of eight 10-bit resolution channels is incorporated.

The following two A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-7. A/D Converter Block Diagram



5.6 Serial Interfaces

Three serial interface channels are incorporated.

- Serial interface (UART0n) (n = 0, 1): 2 channels
- Serial interface (SIO3): 1 channel

(1) Serial interface (UART00, UART01)

UART0n (n = 0, 1) provides the following modes:

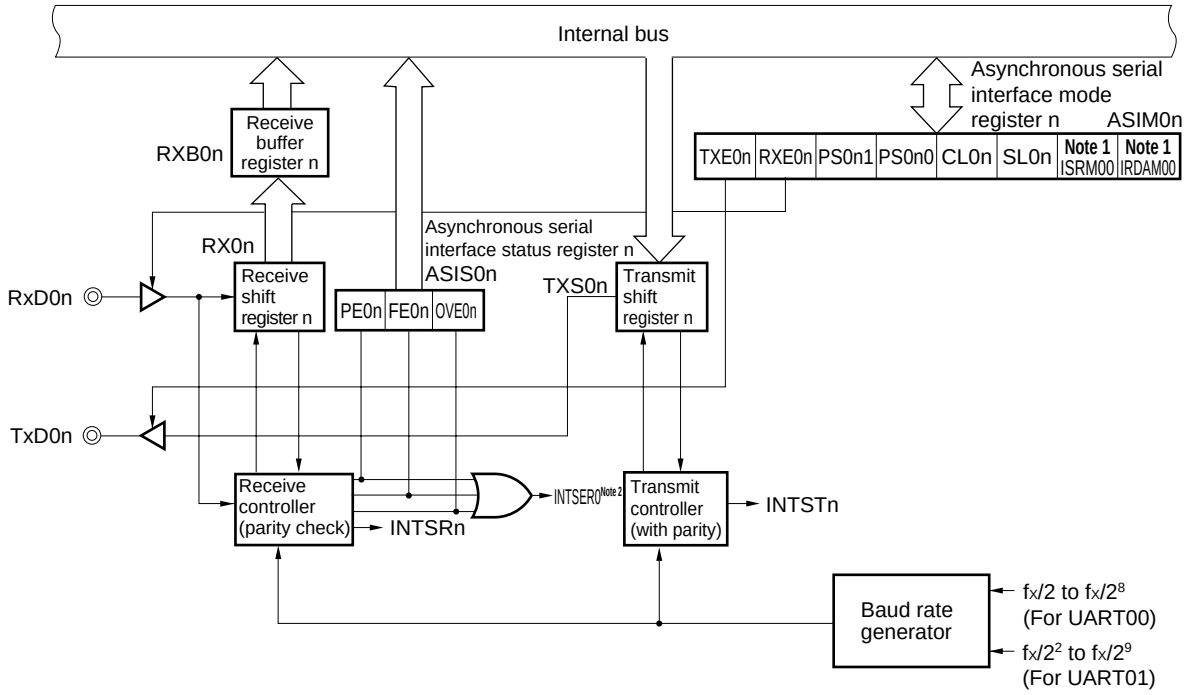
- **Asynchronous serial interface (UART) mode**

  This mode is used to transmit and receive 1-byte data following the start bit. Full-duplex operation is available. A UART dedicated baud rate generator is incorporated. Any baud rate in a wide range can be used for communication. By setting the mode register, the baud rate can be selected in the range of 600 bps to 115.2 kbps (@ f_X = 8.38 MHz operation) for UART00 and 300 bps to 38.4 kbps (@ f_X = 8.38 MHz operation) for UART01.

- **Infrared data transfer mode (UART00 only)**

  115.2 kbps baud rate communication (@ f_X = 7.3728 MHz operation) is available.

Figure 5-8. Block Diagram of Serial Interface (UART0n)



Notes 1. Fixed to 0 for UART01.

2. A reception error interrupt request is not generated for UART01.

Remark n = 0, 1

(2) Serial interface (SIO3)

SIO3 provides the 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed MSB first)**

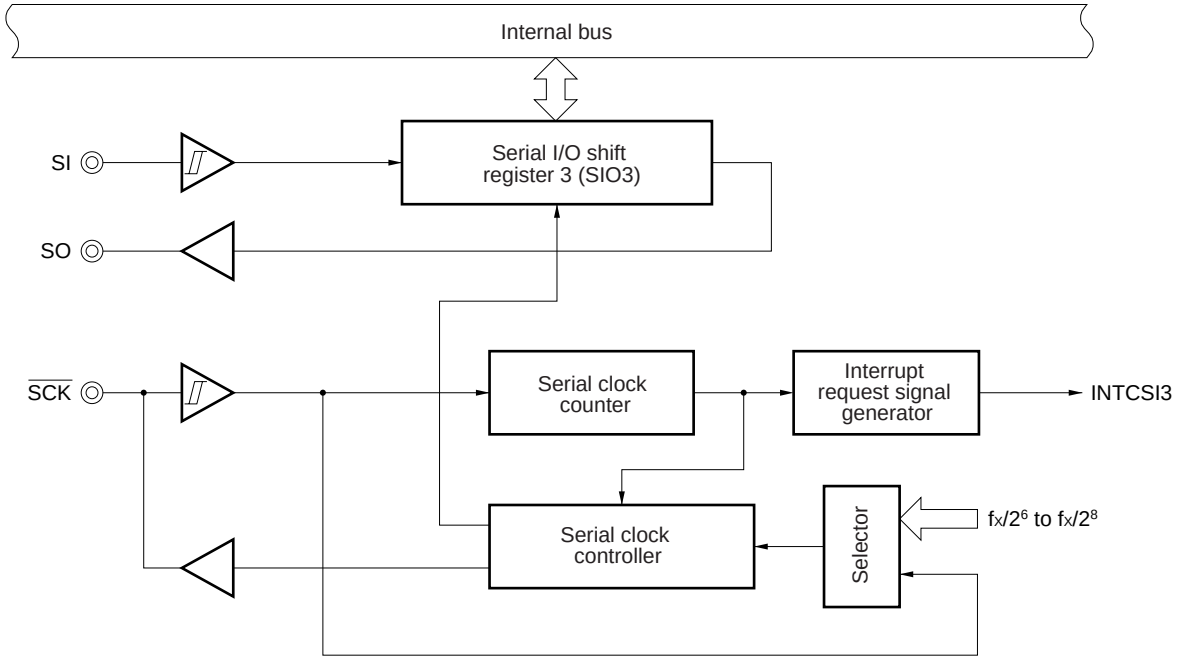
  This mode performs 8-bit data transfer using three lines: serial clock ($\overline{SCK}$), serial output (SO), and serial input (SI).

  The 3-wire serial I/O mode enables simultaneous transmission and reception, thereby speeding up data transfer processing.

  The first bit of 8-bit data for the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is valid when connecting a peripheral I/O or display controller in which a clocked serial interface is included.

Figure 5-9. Block Diagram of Serial Interface (SIO3)



6. INTERRUPT FUNCTIONS

A total of 26 interrupt sources are provided, divided into the following three types.

- Non-maskable interrupts: 1
- Maskable interrupts: 24
- Software interrupts: 1

Table 6-1. Interrupt Sources (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with non-maskable interrupt selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTP7			0014H	
	9	INTTM7	TM7 underflow	Internal	0016H	(B)
	10	INTTM000	TM00 and CR000 match signal generation (when compare register specified) TI010 valid edge detection (when capture register specified)		0018H	
	11	INTTM010	TM00 and CR010 match signal generation (when compare register specified) TI000 valid edge detection (when capture register specified)		001AH	
	12	INTTM001	TM01 and CR001 match signal generation (when compare register specified) TI011 valid edge detection (when capture register specified)		001CH	

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 23 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

Remark Two types of interrupt sources are available for the watchdog timer (INTWDT): non-maskable interrupt and maskable interrupt (internal). However, only one of these can be selected.

Table 6-1. Interrupt Sources (2/2)

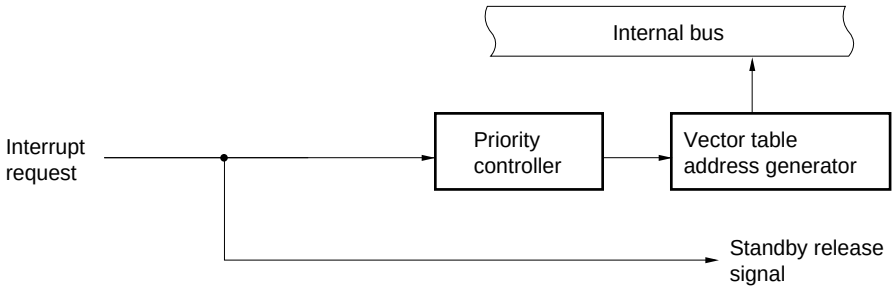
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	13	INTTM011	TM01 and CR011 match signal generation (when compare register specified) TI001 valid edge detection (when capture register specified)	Internal	001EH	(B)
	14	INTSER0	Occurrence of UART00 reception error		0020H	
	15	INTSR0	End of UART00 reception		0022H	
	16	INTST0	End of UART00 transmission		0024H	
	17	INTSR1	End of UART01 reception		0026H	
	18	INTST1	End of UART01 transmission		0028H	
	19	INTTM50	Generation of TM50 and CR50 match signal		002AH	
	20	INTTM51	Generation of TM51 and CR51 match signal		002CH	
	21	INTTM52	Generation of TM52 and CR52 match signal		002EH	
	22	INTCSI3	End of SIO3 transfer		0030H	
	23	INTAD0	End of A/D conversion		0032H	
Software	—	BRK	Execution of BRK instruction	—	003EH	(D)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 23 is the lowest.

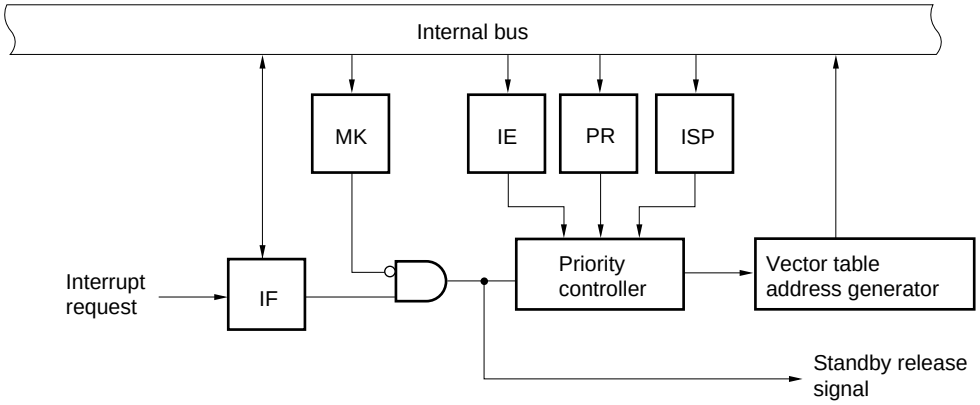
2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

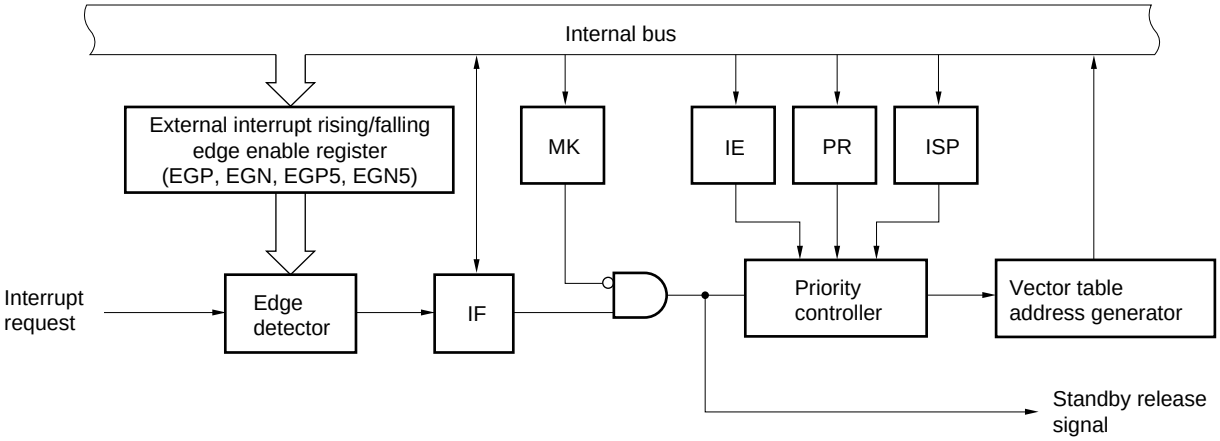
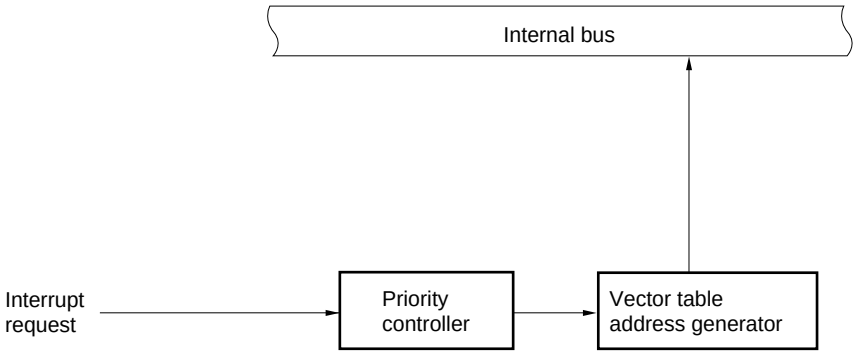


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

The external device expansion function connects external devices to areas other than the internal ROM, RAM, and SFRs.

Ports 4 and 6 are used for external device connection.

256 bytes of external memory expansion is possible for the μPD780982, 780983, 780984, 780986, 780982(A), 780983(A), 780984(A), and 780986(A).

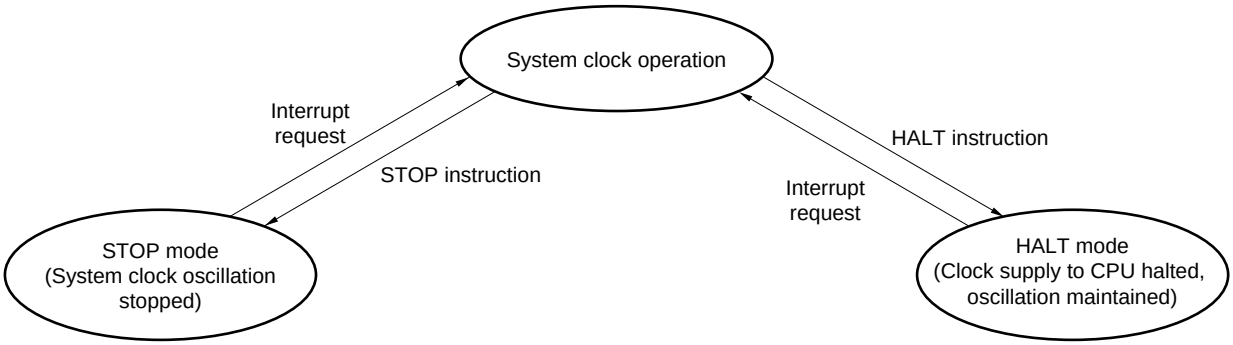
16 bytes of external memory expansion is possible for the μPD780988 and 780988(A) using the external access area of SFR space.

8. STANDBY FUNCTIONS

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Figure 8-1. Standby Functions



9. RESET FUNCTIONS

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL.

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR, DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P50 to P57, P64 to P67, TO70 to TO75, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3 and –0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P00, P01, P30 to P37, P40 to P47, P50 to P57, P64 to P67		–15	mA
		Total for P02, P03, P20 to P26, TO70 to TO75		–15	mA
Output current, low	I_{OL} Note	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P64 to P67 per pin	Peak value	20	mA
			rms value	10	mA
		P50 to P57, TO70 to TO75 per pin	Peak value	30	mA
			rms value	15	mA
		Total for P00, P01, P30 to P37, P40 to P47, P64 to P67	Peak value	50	mA
			rms value	20	mA
		Total for P02, P03, P20 to P26	Peak value	30	mA
			rms value	15	mA
		Total for TO70 to TO75	Peak value	100	mA
			rms value	70	mA
		Total for P50 to P57	Peak value	100	mA
			rms value	70	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

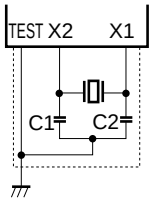
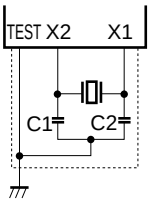
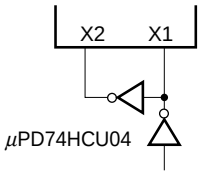
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P03, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75			15	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]		1.0		8.38	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		8.38	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			10	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		8.38	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		50		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	4.0	5.5
	CST2.00MG040	2.00	On-chip	On-chip	4.0	5.5
	CSA3.58MG	3.58	30	30	4.0	5.5
	CST3.58MGW	3.58	On-chip	On-chip	4.0	5.5
	CSA4.00MG	4.00	30	30	4.0	5.5
	CST4.00MGW	4.00	On-chip	On-chip	4.0	5.5
	CSA4.19MG	4.19	30	30	4.0	5.5
	CST4.19MGW	4.19	On-chip	On-chip	4.0	5.5
	CSA4.91MG	4.91	30	30	4.0	5.5
	CST4.91MGW	4.91	On-chip	On-chip	4.0	5.5
	CSA5.00MG	5.00	30	30	4.0	5.5
	CST5.00MGW	5.00	On-chip	On-chip	4.0	5.5
	CSA7.37MTZ	7.37	30	30	4.0	5.5
	CST7.37MTW	7.37	On-chip	On-chip	4.0	5.5
	CSA8.00MTZ	8.00	30	30	4.0	5.5
	CST8.00MTW	8.00	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ	8.38	30	30	4.0	5.5
	CST8.38MTW	8.38	On-chip	On-chip	4.0	5.5

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P37, P40 to P47, P50, P53, P64 to P67			0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P00 to P03, P20, P22, P24 to P26, P51, P52, P54 to P57			0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2			V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P37, P40 to P47, P50, P53, P64 to P67			0		0.3V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P00 to P03, P20, P22, P24 to P26, P51, P52, P54 to P57			0		0.2V_{DD}	V
	V_{IL3}	X1, X2			0		0.4	V
Output voltage, high	V_{OH1}	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA			V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P50 to P57, TO70 to TO75	5.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA			0.4	2.0	V
		P00 to P03, P20 to P26, P30 to P37, P40 to P47, P64 to P67	5.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA				0.4	V
	V_{OL2}	I_{OL} = 400 μA					0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75, $\overline{\text{RESET}}$				3	μA
	I_{LIH2}		X1, X2				20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75, $\overline{\text{RESET}}$				–3	μA
	I_{LIL2}		X1, X2				–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}					3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V					–3	μA
Software pull-up resistor	R_2	V_{IN} = 0 V P00 to P03, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	30	90	kΩ
Power supply current[Note 1]	I_{DD1}	8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 2]	When A/D converter stopped		6.5	19.5	mA
				When A/D converter operating		7.5	21.5	mA
	I_{DD2}	8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 2]	When peripheral functions stopped		1.0	3.0	mA
				When peripheral functions operating			7.6	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ±10%			0.1	30	μA

Notes 1. Refers to the total current flowing to the internal power supply (V_{DD0} and V_{DD1}). The peripheral operating current is included (however, the current flowing to the pull-up resistor of ports and AV_{REF} pin is not included).

2. High-speed operation mode (when the processor clock control register (PCC) is set to 00H).

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

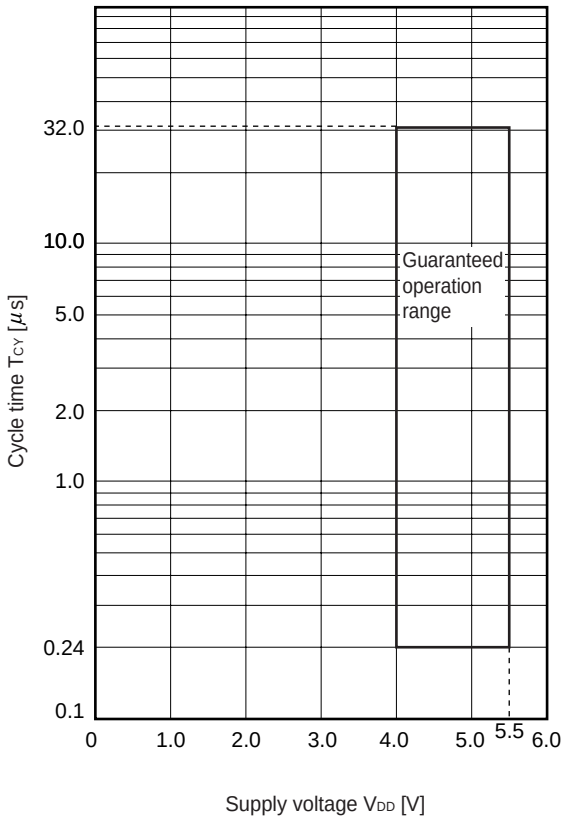
AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with system clock	0.24		32	μs
TI000, TI001, TI010, TI011 input frequency	f_{TI0}		0		f_X/64	MHz
TI000, TI001, TI010, TI011 input high-/low-level width	t_{TIH0} t_{TIL0}		$2/f_{sam}$ + 0.1[Note]			μs
TI50, TI51, TI52 input frequency	f_{TI5}	8-/16-bit precision	0		4	MHz
TI50, TI51, TI52 input high-/low-level width	t_{TIH5} t_{TIL5}	8-/16-bit precision	100			ns
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0 to INTP7	1			μs
TOFF input high-/low-level width	t_{TOFFH} t_{TOFFL}		2			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}		10			μs

Note Selection of $f_{sam} = f_X$, $f_X/4$, $f_X/32$ is possible with bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00) or with bits 0 and 1 (PRM010, PRM011) of prescaler mode register 01 (PRM01). Note that when selecting TI000 (TM00) or TI001 (TM01) valid edge as the count clock, $f_{sam} = f_X/16$.

T_{CY} vs. V_{DD} (System clock operation)



(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Time from address to data input	t_{ADD1}			$(2 + 2n)t_{CY} – 54$	ns
	t_{ADD2}			$(3 + 2n)t_{CY} – 60$	ns
Time from $\overline{RD}\downarrow$ to address output	t_{RDAD}		0	100	ns
Time from $\overline{RD}\downarrow$ to data input	t_{RDD1}			$(2 + 2n)t_{CY} – 87$	ns
	t_{RDD2}			$(3 + 2n)t_{CY} – 93$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY} – 33$		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY} – 33$		ns
Time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{RDWT1}			$t_{CY} – 43$	ns
	t_{RDWT2}			$t_{CY} – 43$	ns
Time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$ input	t_{WRWT}			$0.5t_{CY} – 25$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY} + 10$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL}		$(1.5 + 2n)t_{CY} – 15$		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY} – 15$		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.8t_{CY} – 15$	$1.2t_{CY}$	ns
Time from $\overline{RD}\uparrow$ to write data output	t_{RDWD}		40		ns
Time from $\overline{WR}\downarrow$ to write data output	t_{WRWD}		10	60	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY} + 25$	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY} + 25$	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of AD0 to AD7, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}		954			ns
$\overline{SCK}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(b) 3-wire serial I/O mode ($\overline{SCK}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(c) UART mode (UART00) (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					125000	bps

(d) UART mode (UART00) (Infrared data transfer mode)

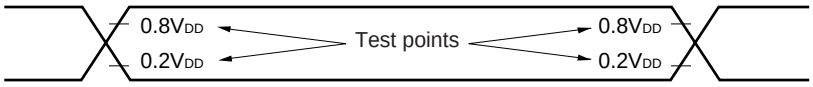
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					115200	bps
Bit rate allowable error					±0.87	%
Output pulse width			1.2		0.24/fbr[Note]	μs
Input pulse width			$4/f_X$			μs

Note fbr: Set baud rate

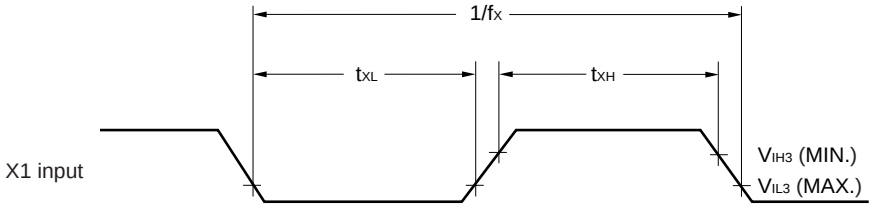
(e) UART mode (UART01) (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38400	bps

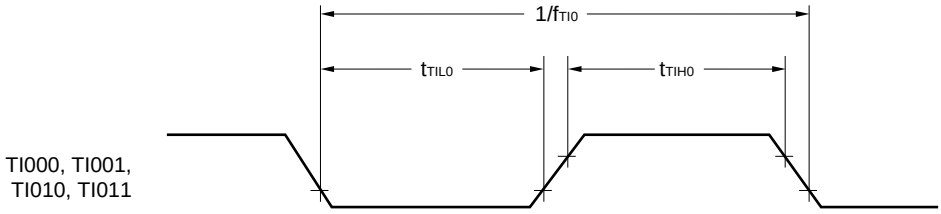
AC Timing Test Points (excluding X1 input)

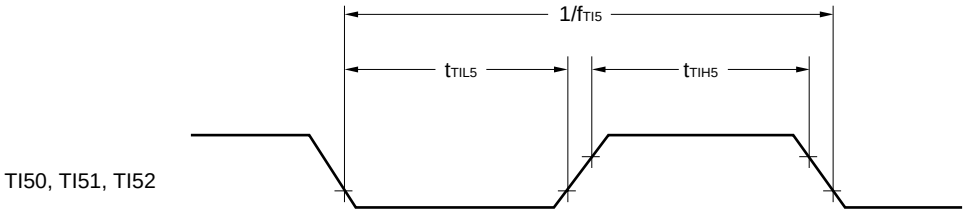


Clock Timing

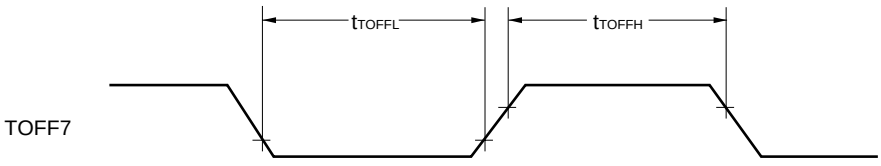


TI Timing



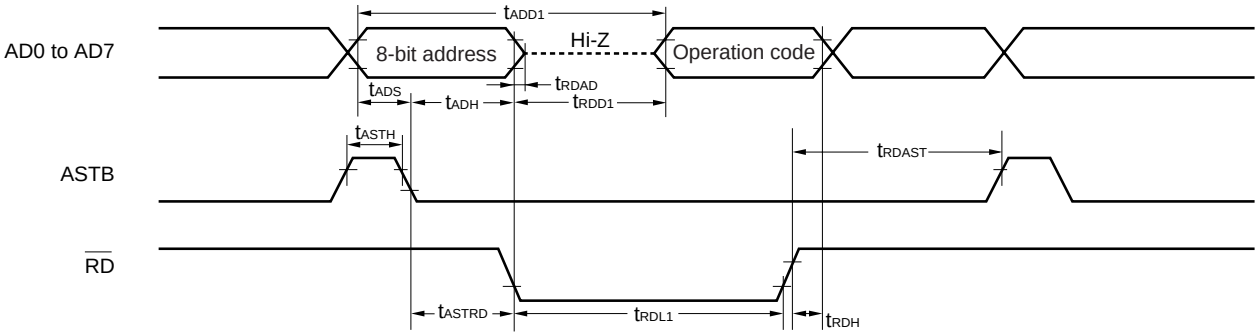


TOFF Timing

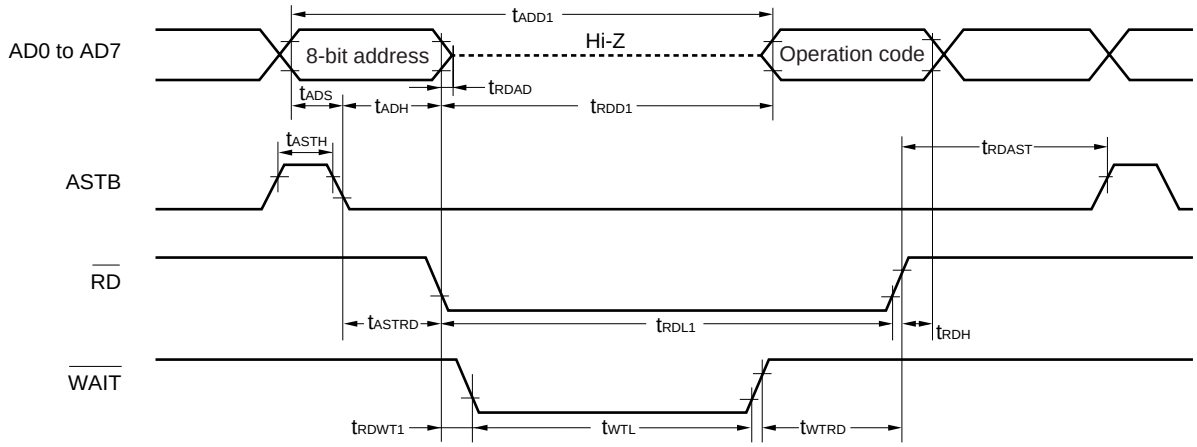


Read/Write Operation

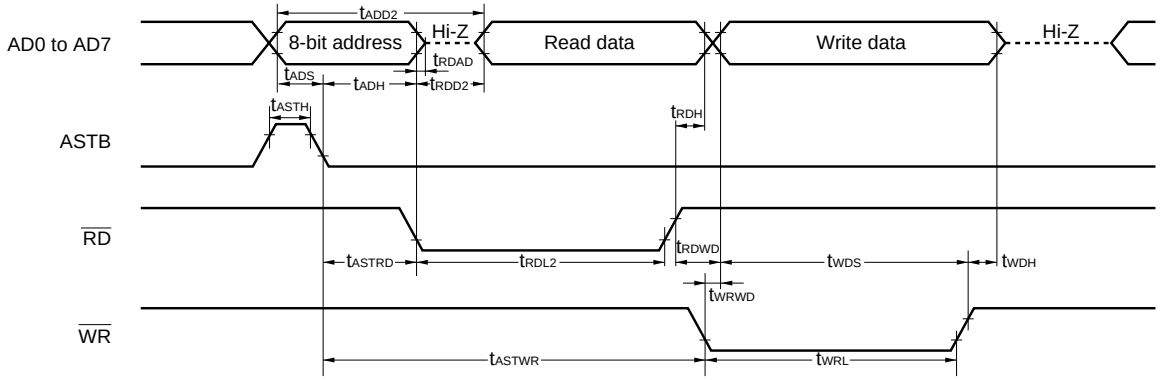
External fetch (no wait):



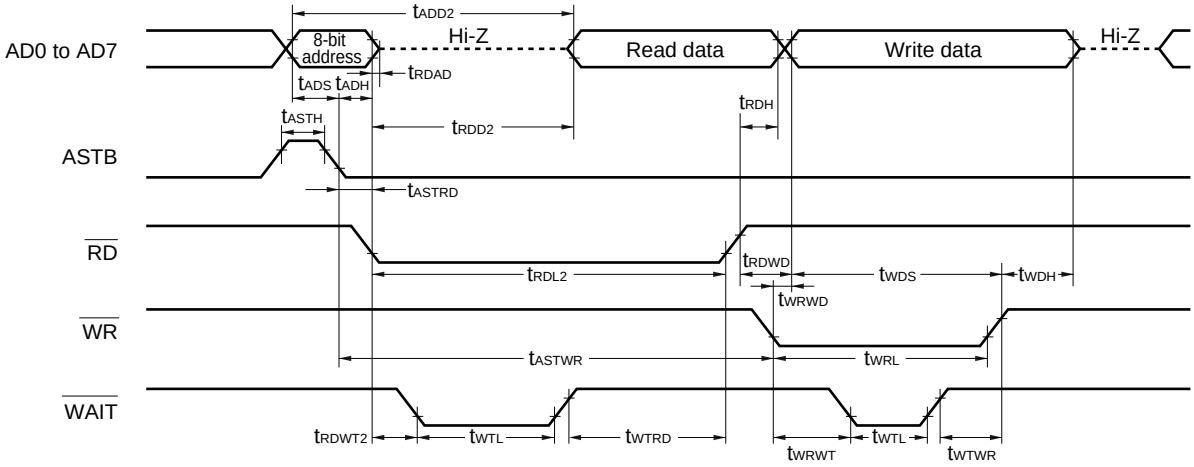
External fetch (wait insertion):



External data access (no wait):

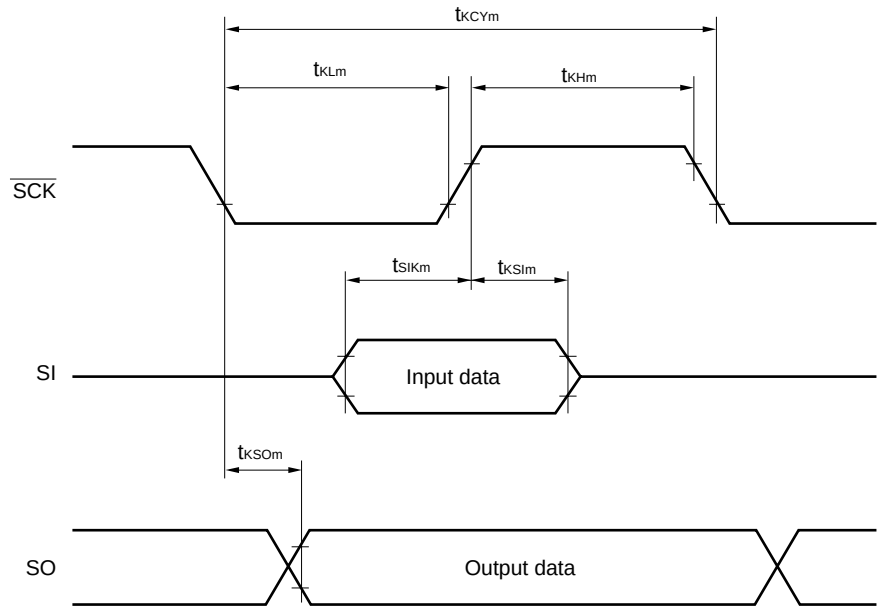


External data access (wait insertion):



Serial Transfer Timing

3-wire serial I/O mode:



m = 1, 2

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV_{REF} < 4.0 V	19		96	μs
Zero-scale error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
Full-scale error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
Integral linearity error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
Differential linearity error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	When A/D converter is not operating	20	40		kΩ

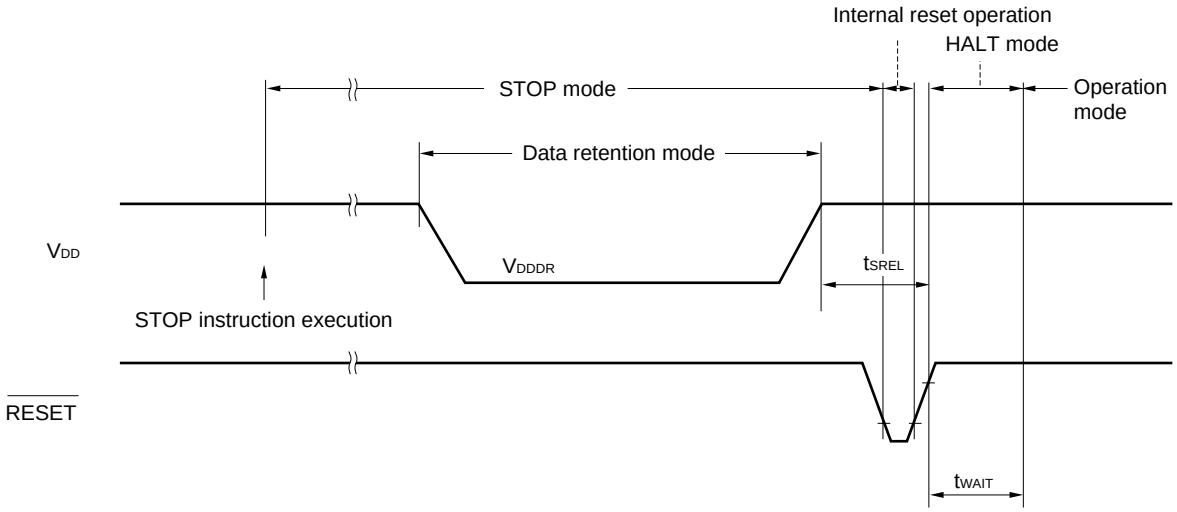
Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

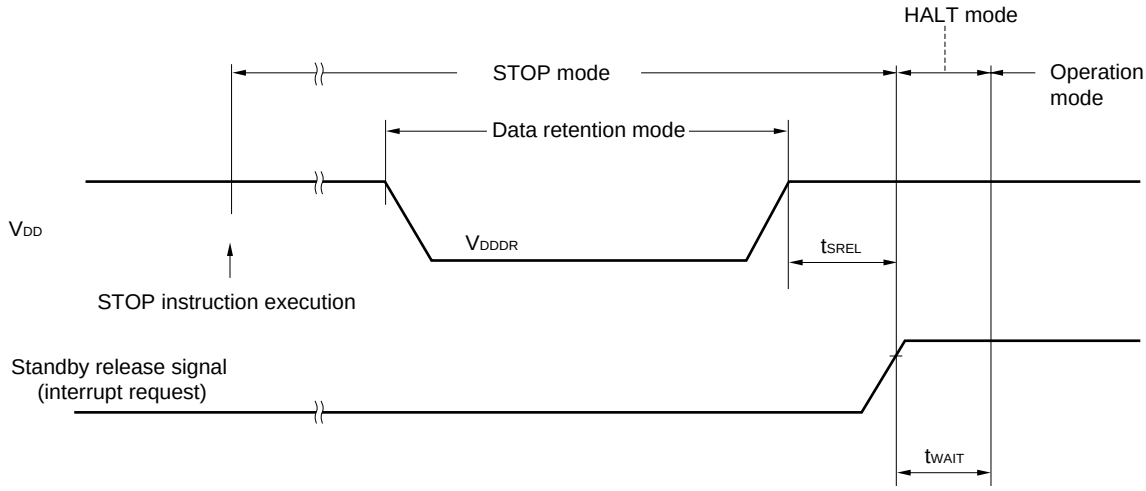
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

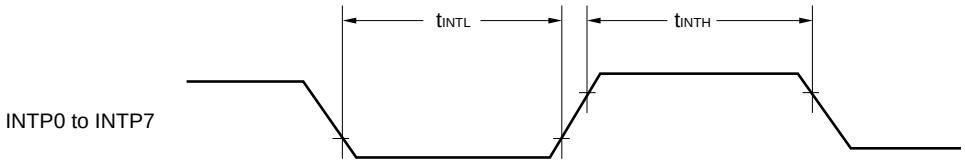
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



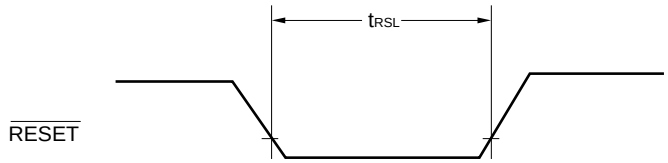
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

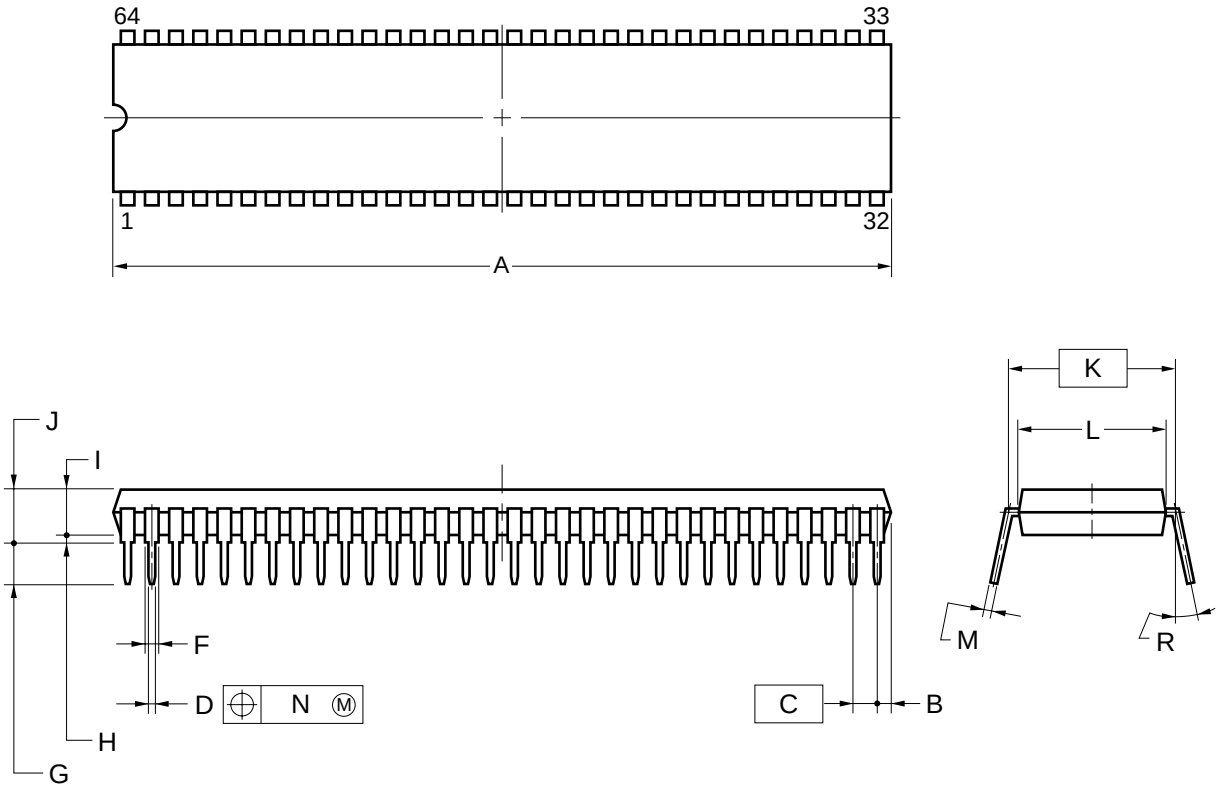


$\overline{\text{RESET}}$ Input Timing



12. PACKAGE DRAWINGS

64-PIN PLASTIC SDIP (19.05mm(750))



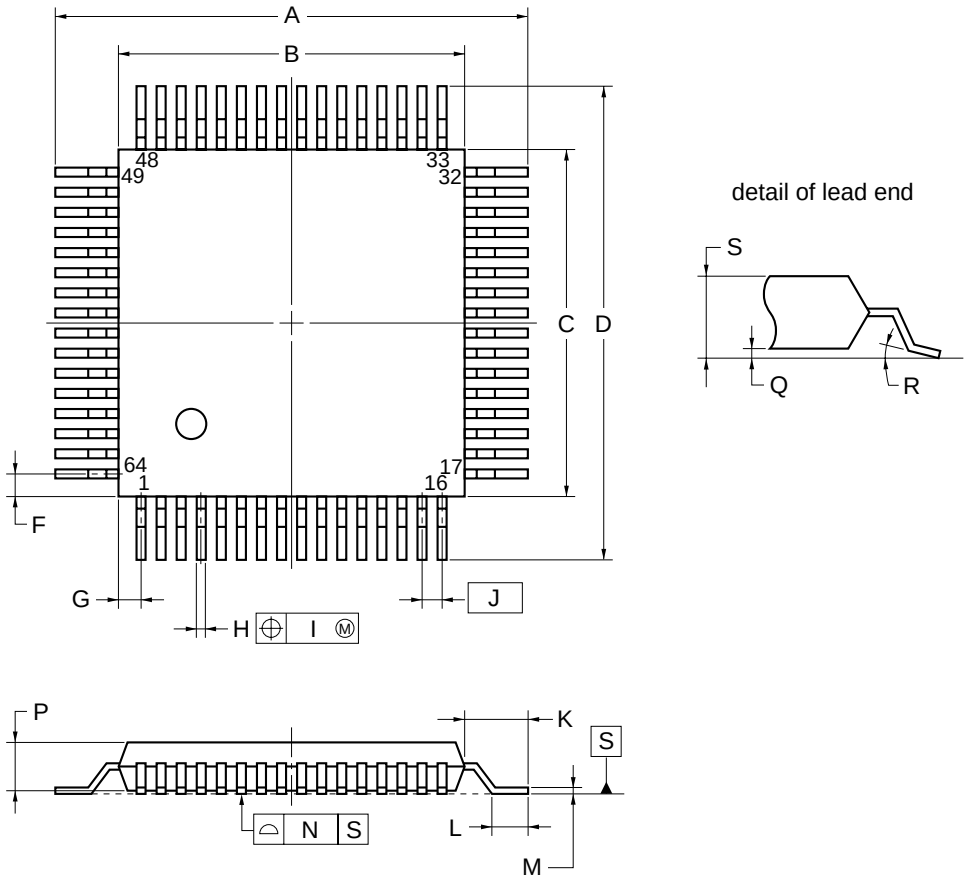
NOTES

1. Each lead centerline is located within 0.17 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	$58.0^{+0.68}_{-0.20}$
B	1.78 MAX.
C	1.778 (T.P.)
D	0.50±0.10
F	0.9 MIN.
G	3.2±0.3
H	0.51 MIN.
I	$4.05^{+0.26}_{-0.20}$
J	5.08 MAX.
K	19.05 (T.P.)
L	17.0±0.2
M	$0.25^{+0.10}_{-0.05}$
N	0.17
R	0 ~ 15°

P64C-70-750A,C-4

64-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.6±0.4
B	14.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.55±0.1
Q	0.1±0.1
R	5°±5°
S	2.85 MAX.

P64GC-80-AB8-5

13. RECOMMENDED SOLDERING CONDITIONS

The μPD780982, 780983, 780984, 780986, and 780988 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions

μPD780982GC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780983GC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780984GC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780986GC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780988GC-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780982GC(A)-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780983GC(A)-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780984GC(A)-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780986GC(A)-×××-AB8: 64-pin plastic QFP (14 × 14 mm)
μPD780988GC(A)-×××-AB8: 64-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

Table 13-2. Insertion Type Soldering Conditions

μPD780982CW-×××: 64-pin plastic SDIP (19.05 mm (750))
μPD780983CW-×××: 64-pin plastic SDIP (19.05 mm (750))
μPD780984CW-×××: 64-pin plastic SDIP (19.05 mm (750))
μPD780986CW-×××: 64-pin plastic SDIP (19.05 mm (750))
μPD780988CW-×××: 64-pin plastic SDIP (19.05 mm (750))

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780988 Subseries.
Also refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (part No. FL-PR2), Flashpro III (part No. FL-PR3, PG-FP3)	Flash programmer dedicated to microcontrollers incorporating flash memory
FA-64CW FA-64GC	Adapter for flash memory writing

(3) Debugging Tools

• When IE-78K0-NS in-circuit emulator is used

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board for enhancement and expansion of IE-78K0-NS function
IE-70000-98-IF-C	Adapter required when using PC-9800 Series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable required when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter required when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
★ IE-70000-PCI-IF-A	Interface adapter necessary when using PCI bus incorporated PC as host machine
IE-780988-NS-EM4	Emulation board to emulate μPD780988 Subseries
IE-78K0-NS-P01	I/O board necessary to emulate μPD780988 Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC NP-64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Conversion socket to connect the NP-64GC and a target system board on which the 64-pin plastic QFP (GC-AB8 type) can be mounted
TGC-064SAP	Conversion adapter to connect the NP-64GC-TQ and a target system board on which the 64-pin plastic QFP (GC-AB8 type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries

• When IE-78001-R-A in-circuit emulator is used

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when PC-9800 Series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
★ IE-70000-PCI-IF-A	Adapter necessary when using PCI bus incorporated PC as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780988-NS-EM4	Emulation board to emulate μPD780988 Subseries
IE-78K0-NS-P01	I/O board necessary to emulate μPD780988 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780988-NS-EM4 and IE-78K0-NS-P01 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on a target system board made for mounting 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780988.
- The CC78K0 and RX78K/0 are used in combination with the RA78K0 or DF780988.
- The FL-PR2, FL-PR3, FA-64CW, FA-64GC, NP-64CW, NP-64GC, and NP-64GC-TQ are products of Naito Densei Machida Mfg. Co., Ltd. (TEL +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- The TGC-064SAP is a product of Tokyo Eletech Corporation.
  For further information, contact: Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL +81-3-3820-7112)
  Osaka Electronics Department (TEL +81-6-6244-6672)
- For third-party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machine and OS suitable for each software are as follows.

Host Machine [OS] / Software	PC PC-9800 Series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.
μPD780988 Subseries User's Manual	U13029E
μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), 780988(A) Data Sheet	This manual
μPD78F0988 Data Sheet	U12805E
μPD780988 Subseries Inverter Control Application Note	U13119E
78K/0 Series Instructions User's Manual	U12326E
★ 78K/0 Series Basic (I) Application Note	U12704E
78K/0, 78K/0S Series Flash Memory Write Application Note	U14458E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U11802E
	Assembly Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
★ PG-FP3 Flash Memory Programmer		U13502E
★ IE-78K0-NS In-Circuit Emulator		U13731E
★ IE-78001-R-A In-Circuit Emulator		Under preparation
IE-780988-NS-EM4 Emulation Board		To be prepared
EP-78240 Emulation Probe		U10332E
SM78K0 System Simulator Windows Based	Reference	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E
★ ID78K0-NS Integrated Debugger Ver. 2.00 or later Windows Based	Operation	U14379E
★ ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamental	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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800-729-9288

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Tel: 0211-65 03 02
Fax: 0211-65 03 490

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