NEC

MOS INTEGRATED CIRCUIT

μPD784907, 784908

16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD784907 and μPD784908 are products of the μPD784908 Subseries in the 78K/IV Series. These products contain various peripheral hardware such as IEBus™ controller, ROM, RAM, I/O ports, 8-bit resolution A/D, timers, serial interface, and interrupt functions, as well as a high-speed, high-performance CPU.

In addition, the μPD78P4908 (one-time PROM product), which is used to evaluate the functions of mask ROM versions, and development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784908 Subseries User's Manual Hardware : U11787E
78K/IV Series User's Manual Instruction : U10905E

FEATURES

- 78K/IV Series
- ★ Minimum instruction execution time: 320 ns (at 6.29 MHz)
  160 ns (at 12.58 MHz)
- Number of I/O ports: 80
- Timer/counters: 16-bit timer/counter × 3 units
  16-bit timer × 1 unit
- Serial interface: 4 channels
  UART/IOE (3-wire serial I/O): 2 channels
  CSI (3-wire serial I/O): 2 channels
- PWM outputs: 2
- Standby function
  HALT/STOP/IDLE mode
- Clock frequency division function
- Watchdog timer: 1 channel
- Clock output function
  Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$
- A/D converter: 8-bit resolution × 8 channels
- On-chip IEBus controller
- Watch timer
- Low-power consumption
- ★ Supply voltage: V_{DD} = 4.0 to 5.5 V
  (Main clock: f_{XX} = 12.58 MHz,
  internal system clock = f_{XX},
  f_{CYK} = 79 ns)
  V_{DD} = 3.5 to 5.5 V
  (Other than above, f_{CYK} = 159 ns)

APPLICATIONS

Car audios, etc.

This document describes the μPD784908 unless otherwise specified.

The information in this document is subject to change without notice.

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Date Published February 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

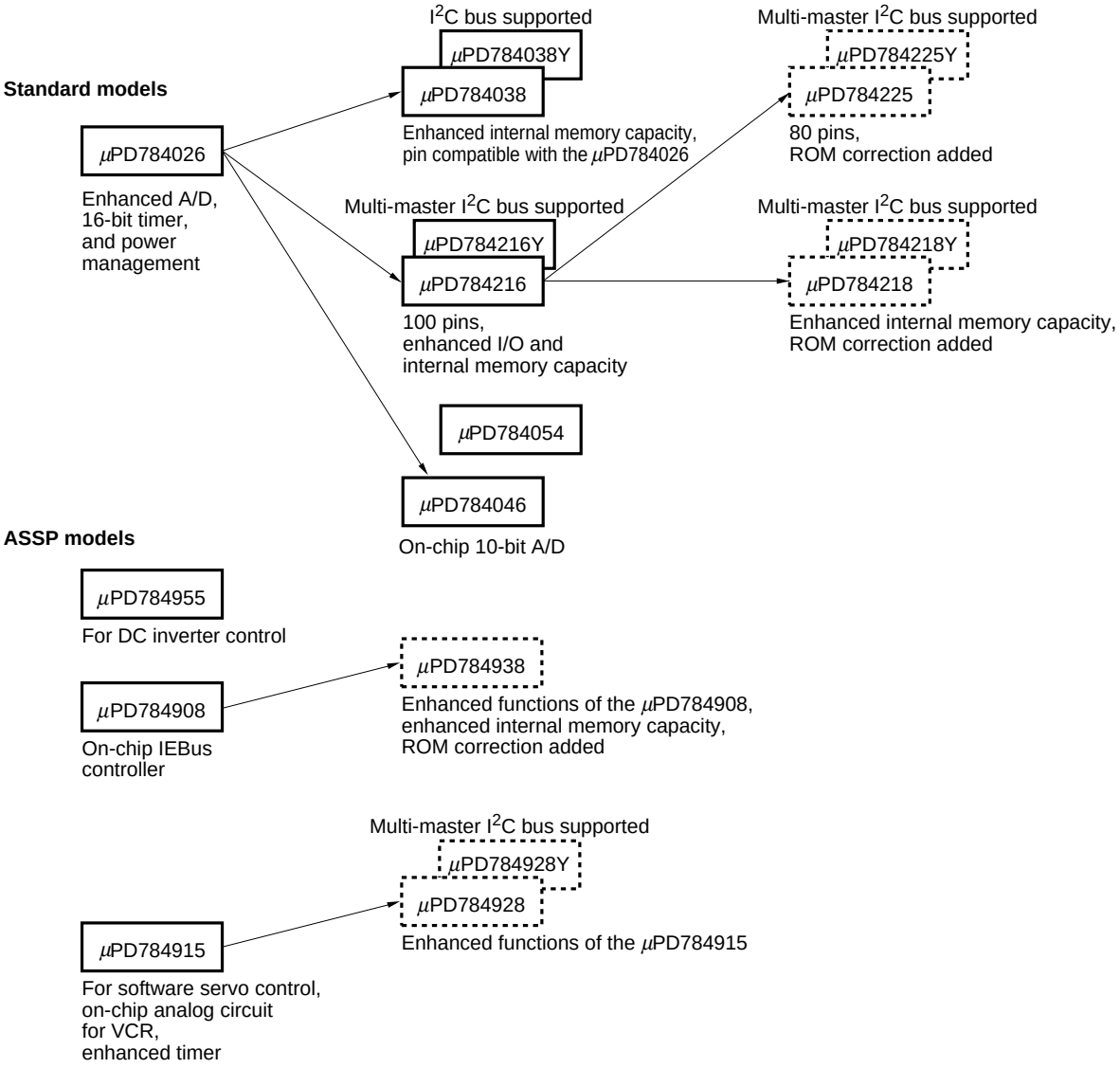
Part number	Package	Internal ROM (bytes)	Internal RAM (bytes)
μPD784907GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)	96 K	3,584
μPD784908GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)	128 K	4,352

Remark ××× indicates ROM code suffix.

★ 78K/IV SERIES PRODUCT LINEUP

: Under mass production

: Under development



FUNCTIONS

Item \ Part Number		μPD784907	μPD784908
Number of basic instructions (mnemonics)		113	
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
★ Minimum instruction execution time		320 ns/636 ns/1.27 μs/2.54 μs (at 6.29 MHz) 160 ns/320 ns/636 ns/1.27 μs (at 12.58 MHz)	
Internal memory	ROM	96 K	128 K
	RAM	3,584 bytes	4,352 bytes
Memory space		1 Mbyte with program and data spaces combined	
I/O ports	Total	80	
	Input	8	
	Input/output	72	
Additional function pins **Note**	LED direct drive outputs	24	
	Transistor direct drive	8	
	N-ch open drain	4	
Real-time output ports		4 bits × 2, or 8 bits × 1	
IEBus controller		Incorporated (simplified)	
Timer/counter		Timer/counter 0: (16 bits) — Timer register × 1; Capture register × 1; Compare register × 2 — Pulse output capability: • Toggle output • PWM/PPG output • One-shot pulse output	
		Timer/counter 1: (16 bits) — Timer register × 1; Capture register × 1; Capture/compare register × 1; Compare register × 1 — Real-time output port	
		Timer/counter 2: (16 bits) — Timer register × 1; Capture register × 1; Capture/compare register × 1; Compare register × 1 — Pulse output capability: • Toggle output • PWM/PPG output	
		Timer 3: (16 bits) — Timer register × 1; Compare register × 1	
Watch timer		Interrupt requests are generated at 0.5-second intervals. (A watch clock oscillator is incorporated.) ★ Either the main clock (6.29 MHz/12.58 MHz) or watch clock (32.7 kHz) can be selected as the input clock.	
Clock output		Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (can be used as a 1-bit output port)	
PWM outputs		12-bit resolution × 2 channels	
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) CSI (3-wire serial I/O): 2 channels	
A/D converter		8-bit resolution × 8 channels	

Note Additional function pins are included in the I/O pins.

Item \ Part Number		μPD784907	μPD784908
Watchdog timer		1 channel	
Standby		HALT/STOP/IDLE modes	
Interrupt	Hardware source	27 (20 internal, 7 external (sampling clock variable input: 1))	
	Software source	BRK or BRKCS instruction, operand error	
	Non-maskable	1 internal, 1 external	
	Maskable	19 internal, 6 external	
		4-level programmable priority 3 operation statuses: vectored interrupt, macro service, context switching	
★ Power supply voltage		V_{DD} = 4.0 to 5.5 V (Main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}, f_{CYK} = 79 ns) V_{DD} = 3.5 to 5.5 V (other than above, f_{CYK} = 159 ns)	
Package		100-pin plastic QFP (14 × 20 mm)	

CONTENTS

1. DIFFERENCES BETWEEN μPD784908 SUBSERIES PRODUCTS

The only difference between the μPD784907 and μPD784908 is their internal memory capacities.

The μPD78P4908 is produced by replacing the mask ROM in the μPD784907 or μPD784908 with 128-Kbyte one-time PROM. Table 1-1 shows the differences between these products.

Table 1-1. Differences between the μPD784908 Subseries Products

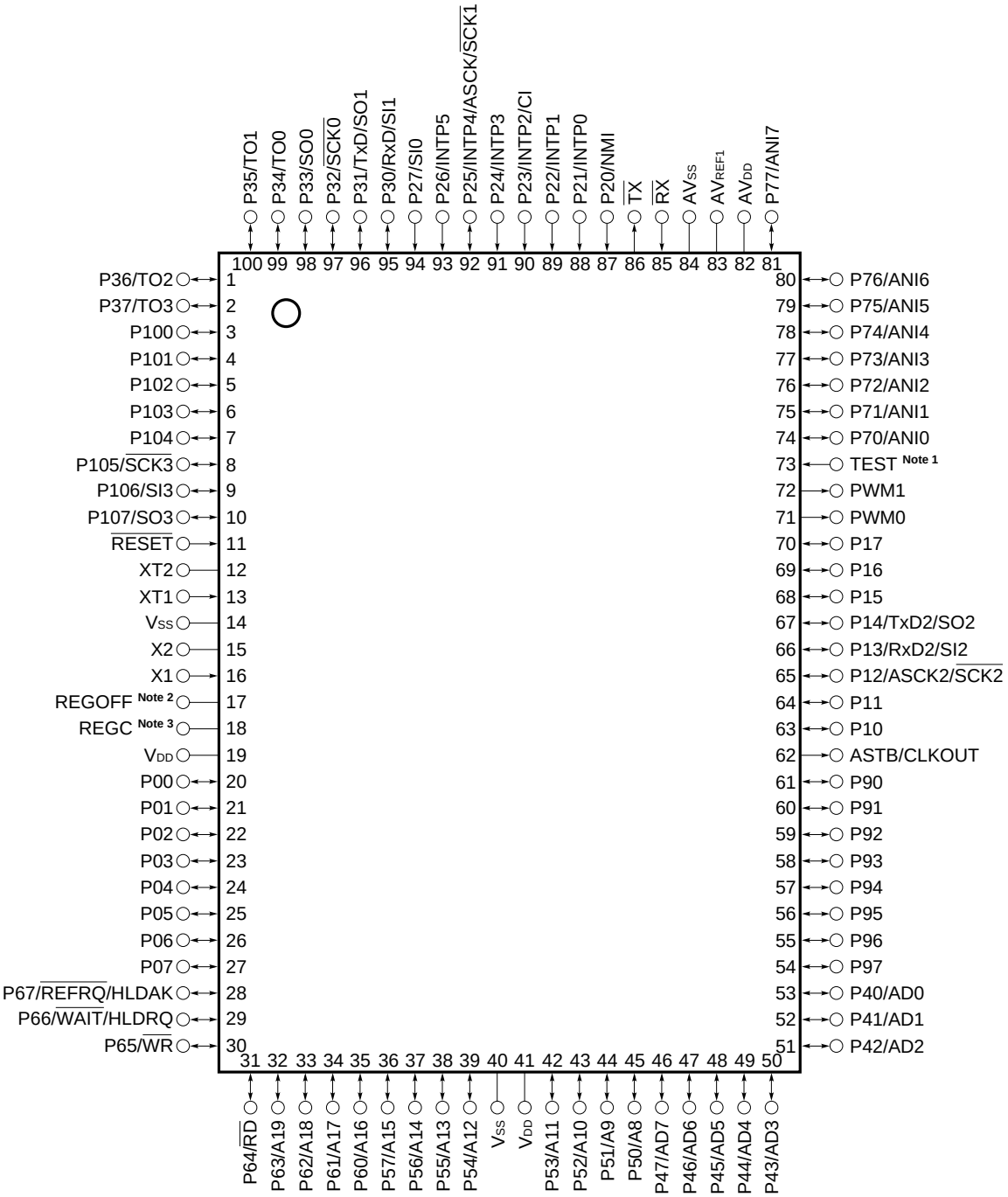
Item \ Part Number	μPD784907	μPD784908	μPD78P4908
Internal ROM	96 K (mask ROM)	128 K (mask ROM)	128 K (one-time PROM)
Internal RAM	3,584 bytes	4,352 bytes	
Regulator	Provided		None
★ Power supply voltage	V_{DD} = 4.0 to 5.5 V (Main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}, f_{CYK} = 79 ns) V_{DD} = 3.5 to 5.5 V (other than above, f_{CYK} = 159 ns)		V_{DD} = 4.5 to 5.5 V (Main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}, f_{CYK} = 79 ns) V_{DD} = 4.0 to 5.5 V (other than above, f_{CYK} = 159 ns)
Electrical specifications	Refer to the data sheet of each product.		

★ 2. MAJOR DIFFERENCES BETWEEN μPD784908 AND μPD78098 SUBSERIES

Item \ Series Name		μPD784908 Subseries	μPD78098 Subseries
Number of basic instructions (mnemonics)		113	63
Minimum instruction execution time		320/160 ns (at 6.29/12.58 MHz operation)	480 ns (at 6.29 MHz operation)
Timer/counter		16-bit timer/counter × 1 8/16-bit timer/counter × 2 8/16-bit timer × 1 Watch timer	16-bit timer/counter × 1 8/16-bit timer/counter × 2 Watch timer
		Single clock Watch clock for clock operation	Dual clock
Watchdog timer		Provided	
Serial interface		UART/IOE (3-wire serial I/O): 2 channels CSI (3-wire serial I/O): 2 channels	UART (3-wire serial I/O): 1 channel CSI/SBI (3-wire serial I/O): 1 channel CSI (3-wire serial I/O): 1 channel
PWM output		2	None
A/D converter		8-bit resolution × 8 channels	
D/A converter		None	
Interrupt	Hardware source	27	23 (two test flags)
	Internal	20	14
	External	7	7
External extended function		Provided (up to 1 Mbyte)	None
IEBus controller		Incorporated (simplified)	Incorporated (complete hardware)
Power supply voltage		• Mask ROM version V_{DD} = 4.0 to 5.5 V (Main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}, f_{CYK} = 79 ns) V_{DD} = 3.5 to 5.5 V (other than above, f_{CYK} = 159 ns) • PROM version V_{DD} = 4.5 to 5.5 V (Main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}, f_{CYK} = 79 ns) V_{DD} = 4.0 to 5.5 V (other than above, f_{CYK} = 159 ns)	V_{DD} = 2.7 to 6.0 V
Package		100-pin plastic QFP (14 × 20 mm)	80-pin plastic QFP (14 × 14 mm) 80-pin plastic WQFN (14 × 14 mm): μPD78P098A only

3. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic QFP (14 × 20 mm)**
  μPD784907GF-×××-3BA
  μPD784908GF-×××-3BA



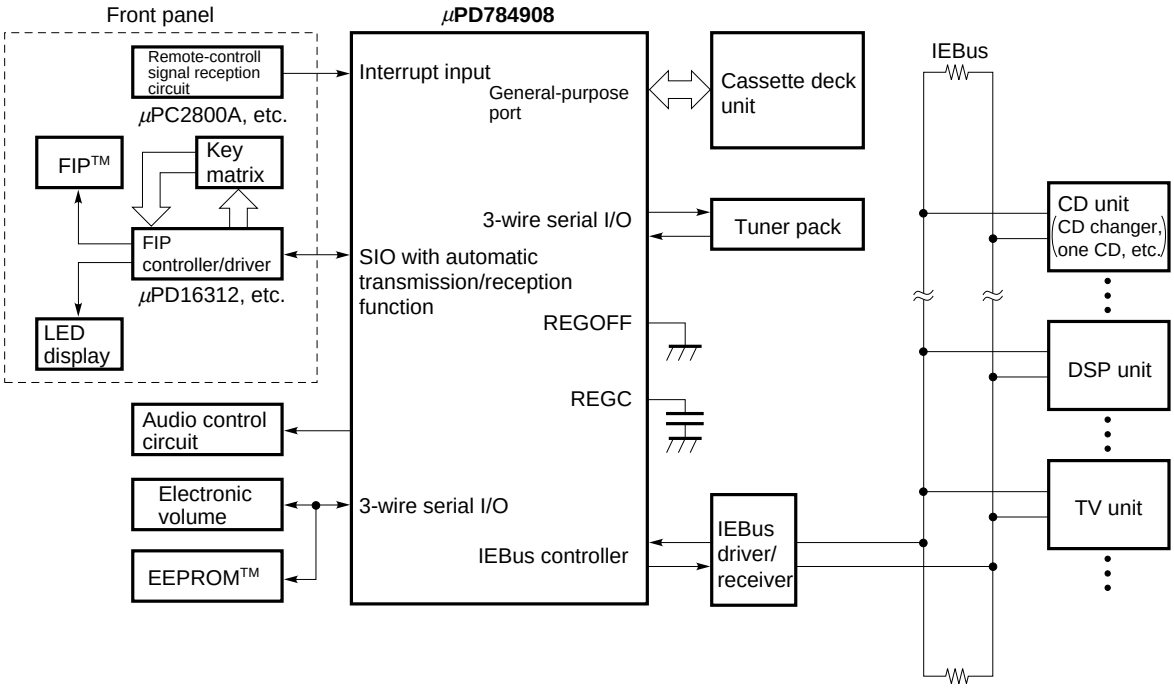
Notes 1. Connect the TEST pin directly to VSS.

2. Connect the REGOFF pin directly to VSS (select regulator operation).

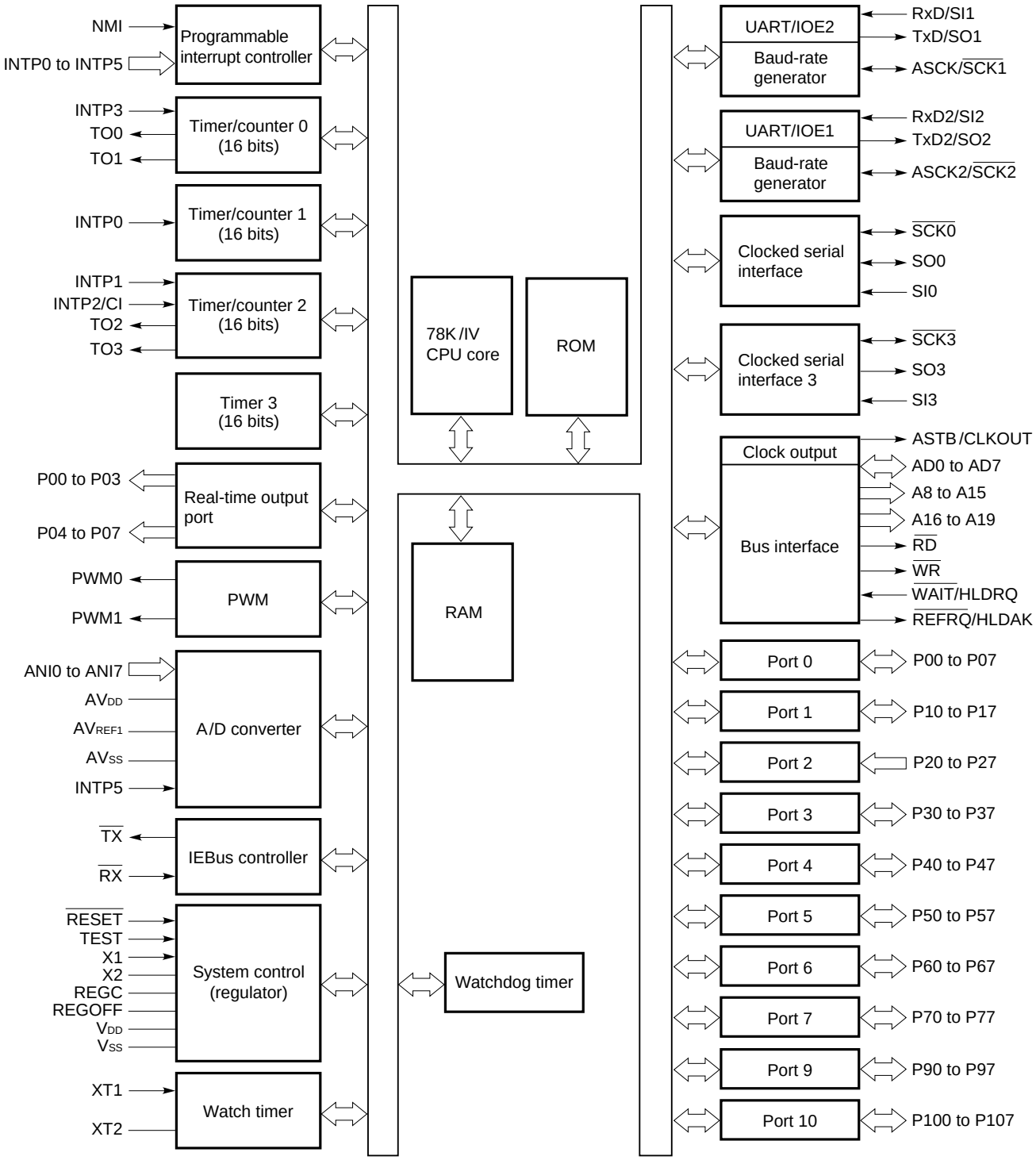
3. Connect the REGC pin to VSS via a capacitor of the order of 1 μF.

A8 to A19: Address bus
AD0 to AD7: Address/data bus
ANI0 to ANI7: Analog input
ASCK, ASCK2: Asynchronous serial clock
ASTB: Address strobe
AV_{DD}: Analog power supply
AV_{REF1}: Reference voltage
AV_{SS}: Analog ground
CI: Clock input
CLKOUT: Clock output
HLDAK: Hold acknowledge
HLDRQ: Hold request
INTP0 to INTP5: Interrupt from peripherals
NMI: Non-maskable interrupt
P00 to P07: Port 0
P10 to P17: Port 1
P20 to P27: Port 2
P30 to P37: Port 3
P40 to P47: Port 4
P50 to P57: Port 5
P60 to P67: Port 6
P70 to P77: Port 7
P90 to P97: Port 9
P100 to P107: Port 10
PWM0, PWM1: Pulse width modulation output
$\overline{RD}$: Read strobe
$\overline{REFRQ}$: Refresh request
REGC: Regulator capacitance
REGOFF: Regulator off
$\overline{RESET}$: Reset
$\overline{RX}$: IEBus receive data
RxD, RxD2: Receive data
$\overline{SCK0}$ to $\overline{SCK3}$: Serial clock
SI0 to SI3: Serial input
SO0 to SO3: Serial output
TEST: Test
TO0 to TO3: Timer output
$\overline{TX}$: IEBus transmit data
TxD, TxD2: Transmit data
V_{DD}: Power supply
V_{SS}: Ground
$\overline{WAIT}$: Wait
$\overline{WR}$: Write strobe
X1, X2: Crystal (main system clock)
XT1, XT2: Crystal (watch)

4. SYSTEM CONFIGURATION EXAMPLE (AUTOMOTIVE CAR AUDIO (TUNER DECK))



5. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities differ depending on the product.

6. PIN FUNCTIONS

6.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00 to P07	I/O	—	Port 0 (P0): • 8-bit I/O port. • Can be used as a real-time output port (4 bits × 2). • Input and output can be specified by 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive transistors.
P10	I/O	—	Port 1 (P1): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LEDs.
P11		—	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15 to P17		—	
P20	Input	NMI	Port 2 (P2): • 8-bit input port. • P20 does not function as a general-purpose port (non-maskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of on-chip pull-up resistors can be specified by software for pins P22 to P27 (in 6-bit units). • The P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin functions as the $\overline{\text{SCK1}}$ output pin by a CSIM1 specification.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode. • The use of the N-ch open drain can be specified for pins P32 and P33.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0	
P34 to P37		TO0 to TO3	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LEDs.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LEDs.

6.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60 to P63	I/O	A16 to A19	Port 6 (P6): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode.
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/HLDRQ	
P67		$\overline{REFRQ}$/HLDAK	
P70 to P77	I/O	ANI0 to ANI7	Port 7 (P7): • 8-bit I/O port. • Input and output can be specified in 1-bit units.
P90 to P97	I/O	—	Port 9 (P9): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode.
P100 to P104	I/O	—	Port 10 (P10): • 8-bit I/O port. • Input and output can be specified in 1-bit units. • The use of on-chip pull-up resistors can be simultaneously specified by software for all pins in input mode. • The use of the N-ch open drain can be specified for pins P105 and P107.
P105		$\overline{SCK3}$	
P106		SI3	
P107		SO3	

6.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	
TO0 to TO3	Output	P34 to P37	Timer output	
CI	Input	P23/INTP2	Input of a count clock for timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SI0	Input	P27	Serial data input (3-wire serial I/O 0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O 1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O 2)	
SI3		P106	Serial data input (3-wire serial I/O 3)	
SO0	Output	P33	Serial data output (3-wire serial I/O 0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O 1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O 2)	
SO3		P107	Serial data output (3-wire serial I/O 3)	
$\overline{\text{SCK0}}$	I/O	P32	Serial clock I/O (3-wire serial I/O 0)	
$\overline{\text{SCK1}}$		P25/INTP4/ASCK	Serial clock I/O (3-wire serial I/O 1)	
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock I/O (3-wire serial I/O 2)	
$\overline{\text{SCK3}}$		P105	Serial clock I/O (3-wire serial I/O 3)	
NMI	Input	P20	External interrupt request	—
INTP0		P21		• Input of a count clock for timer/counter 1 • Capture/trigger signal for CR11 or CR12
INTP1		P22		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR22
INTP2		P23/CI		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR21
INTP3		P24		• Input of a count clock for timer/counter 0 • Capture/trigger signal for CR02
INTP4		P25/ASCK/$\overline{\text{SCK1}}$		—
INTP5		P26		Input of a conversion start trigger for A/D converter
AD0 to AD7	I/O	P40 to P47	Time multiplexing address/data bus (for connecting external memory)	
A8 to A15	Output	P50 to P57	High-order address bus (for connecting external memory)	
A16 to A19	Output	P60 to P63	High-order address bus during address expansion (for connecting external memory)	
$\overline{\text{RD}}$	Output	P64	Strobe signal output for reading the contents of external memory	
$\overline{\text{WR}}$	Output	P65	Strobe signal output for writing on external memory	
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait insertion	
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{\text{WAIT}}$	Input of bus hold request	
HLDAK	Output	P67/$\overline{\text{REFRQ}}$	Output of bus hold response	
ASTB	Output	CLKOUT	Latch timing output of time multiplexing address (A0 to A7) (for connecting external memory)	

6.2 Non-Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
CLKOUT	Output	ASTB	Clock output
PWM0	Output	—	PWM output 0
PWM1	Output	—	PWM output 1
$\overline{RX}$	Input	—	Data input (IEBus)
$\overline{TX}$	Output	—	Data output (IEBus)
★ REGC	—	—	Capacitance connection for stabilizing the regulator output/power supply when the regulator is stopped. Connect to V_{SS} via a capacitor of order of 1μF.
★ REGOFF	—	—	Signal for specifying regulator operation
$\overline{RESET}$	Input	—	Chip reset
X1	Input	—	Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.)
X2	—		
XT1	Input	—	Watch clock connection
XT2	—	—	
ANI0 to ANI7	Input	P70 to P77	Analog voltage input for A/D converter
AV_{REF1}	—	—	To apply the reference voltage for A/D converter
AV_{DD}			Positive power supply for A/D converter
AV_{SS}			GND for A/D converter
V_{DD}			Positive power supply
V_{SS}			GND
TEST	Input		Connect directly to V_{SS}. (This pin is for IC test.)

6.3 Pin I/O Circuits and Recommended Connections of Unused Pins

The input/output circuit type of each pin and recommended connections of unused pins are shown in Table 6-1. For each type of input/output circuit, refer to Figure 6-1.

Table 6-1. Types of Pin I/O Circuits and Recommended Connections of Unused Pins (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00 to P07	5-A	I/O	Input: Connect to V_{DD} Output: Leave open
P10, P11			
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15 to P17			
P20/NMI	2	Input	Connect to V_{DD} or V_{SS}
P21/INTP0			
P22/INTP1	2-A		Connect to V_{DD}
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	I/O	Input: Connect to V_{DD} Output: Leave open
P26/INTP5	2-A	Input	Connect to V_{DD}
P27/SI0			
P30/RxD/SI1	5-A	I/O	Input: Connect to V_{DD} Output: Leave open
P31/TxD/SO1			
P32/$\overline{SCK0}$	10-A		
P33/SO0			
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0 to P77/ANI7	20	I/O	Input: Connect to V_{DD} or V_{SS} Output: Leave open
P90 to P97	5-A		
P100 to P104			
P105/$\overline{SCK3}$	10-A		
P106/SI3	8-A		
P107/SO3	10-A		
ASTB/CLKOUT	4	Output	Leave open

Table 6-1. Types of Pin I/O Circuits and Recommended Connections of Unused Pins (2/2)

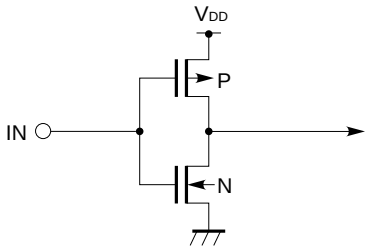
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
$\overline{\text{RESET}}$	2	Input	—
TEST	1		Connect directly to V_{SS}
XT2	—	—	Leave open
XT1	—	Input	Connect to V_{SS}
PWM0, PWM1	3	Output	Leave open
★ $\overline{\text{RX}}$	1	Input	Connect to V_{DD} or V_{SS}
$\overline{\text{TX}}$	3	Output	Leave open
AV_{REF1}	—	—	Connect to V_{SS}
AV_{SS}			
AV_{DD}			Connect to V_{DD}

Caution Connect an I/O pin, whose input/output mode is undefined, to V_{DD} via a resistor of several 10 kΩ (especially if the voltage on the reset input pin rises higher than the low level input at power on or when the mode is being switched between input and output by software).

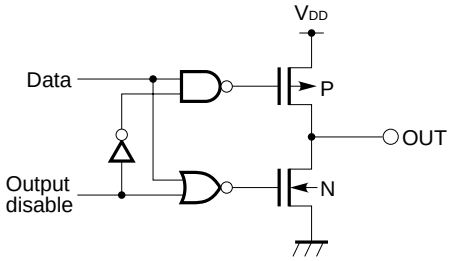
Remark Since type numbers are commonly used in the 78K Series, these numbers are not always serial in each product (some circuits are not included).

Figure 6-1. I/O Circuits for Pins

Type 1

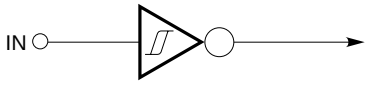


Type 4



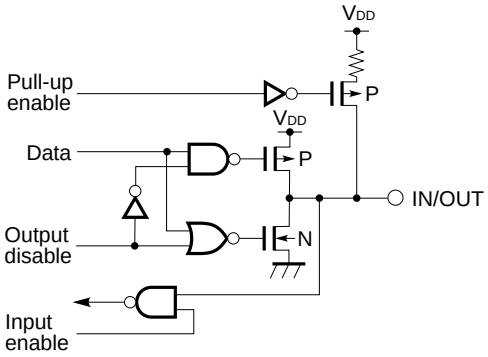
Push-pull output which can output high impedance (both the positive and negative channels are off.)

Type 2

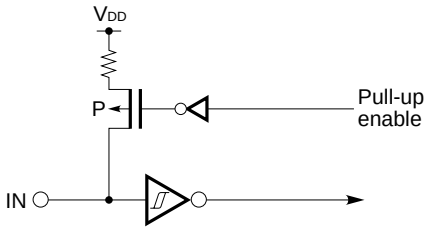


Schmitt trigger input with hysteresis characteristics

Type 5-A

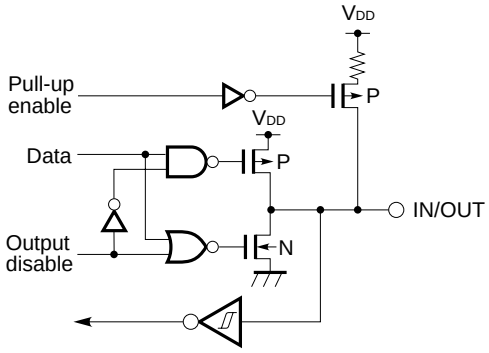


Type 2-A

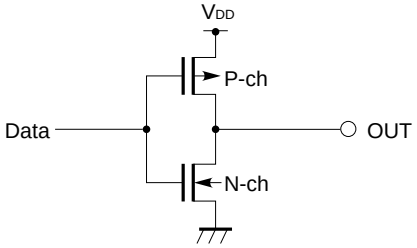


Schmitt trigger input with hysteresis characteristics

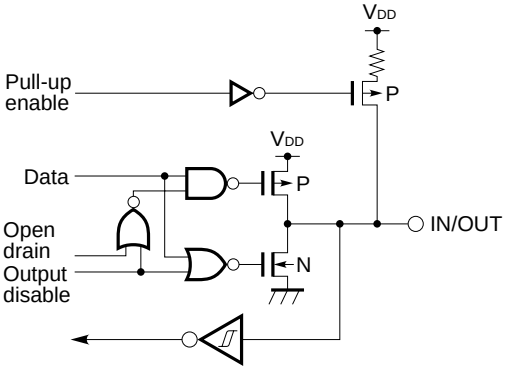
Type 8-A

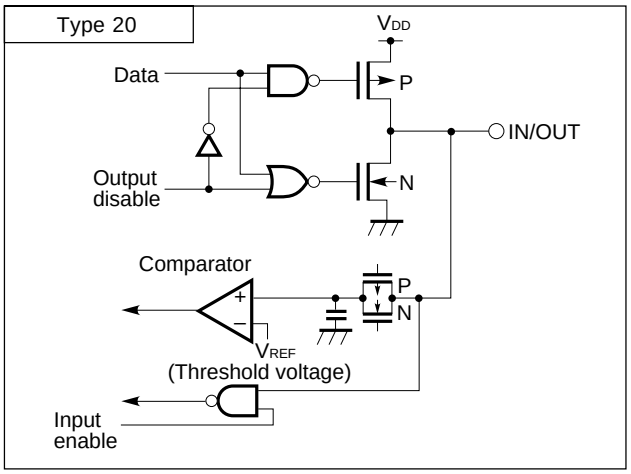


Type 3



Type 10-A




Type 20
VDD
Data
P
IN/OUT
Output
disable
N
Comparator
P
N
VREF
(Threshold voltage)
Input
enable

7. CPU ARCHITECTURE

7.1 Memory Space

A memory space of 1 Mbyte can be accessed. By using a LOCATION instruction, the mode for mapping internal data areas (special function registers and internal RAM) can be selected. A LOCATION instruction must always be executed after a reset, and can be used only once.

(1) When the LOCATION 0 instruction is executed

- **Internal memory**

  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784907	0F100H to 0FFFFH	00000H to 0F0FFH 10000H to 17FFFH
μPD784908	0EE00H to 0FFFFH	00000H to 0FDFFH 10000H to 1FFFFH

Caution The following internal ROM areas, existing at the same addresses as the internal data areas, cannot be used when the LOCATION 0 instruction is executed:

Part Number	Unusable Area
μPD784907	0F100H to 0FFFFH (3,840 bytes)
μPD784908	0EE00H to 0FFFFH (4,608 bytes)

- **External memory**

  The external memory is accessed in external memory expansion mode.

(2) When the LOCATION 0FH instruction is executed

- **Internal memory**

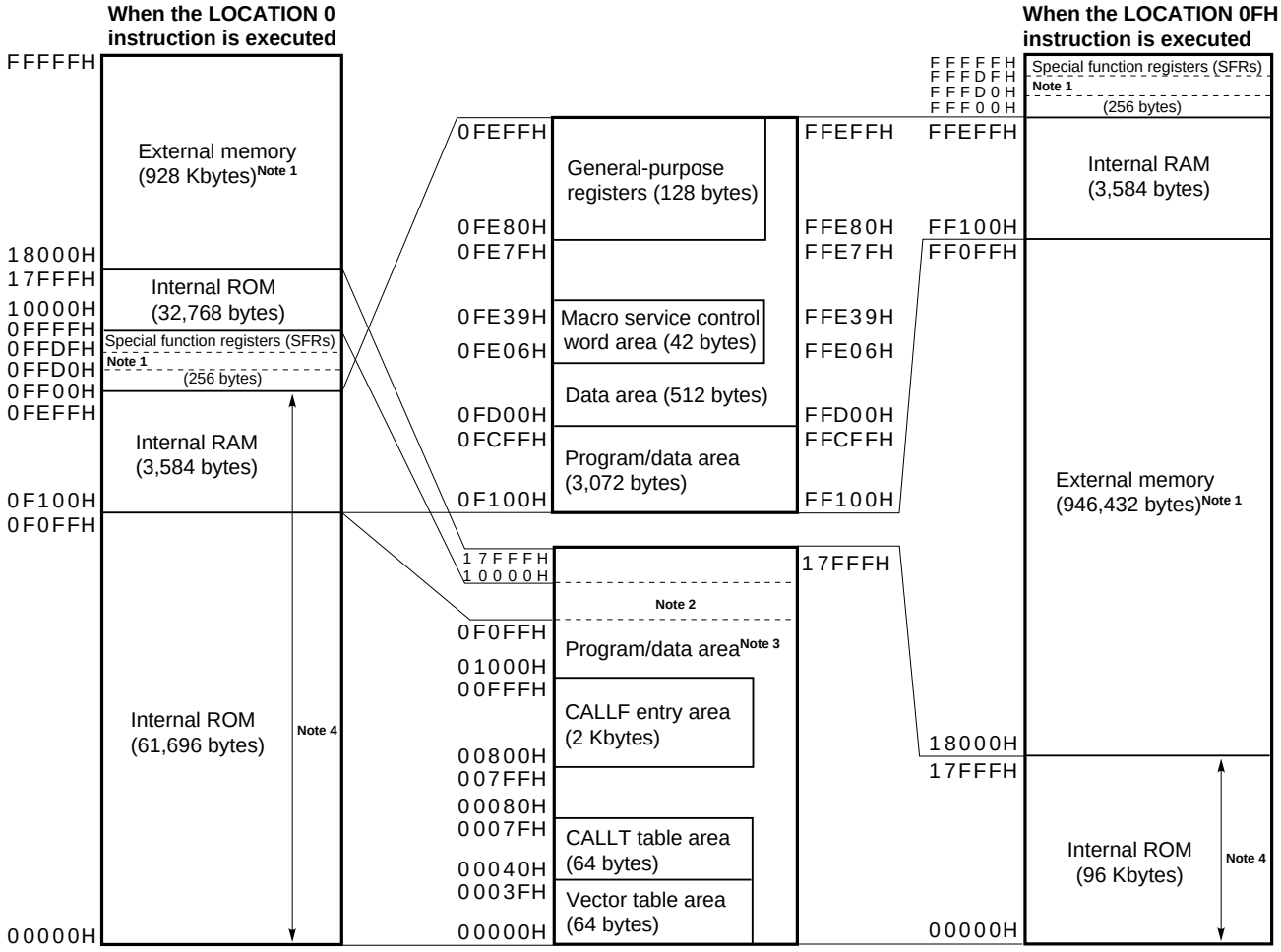
  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784907	FF100H to FFFFFH	00000H to 17FFFH
μPD784908	FEE00H to FFFFFH	00000H to 1FFFFH

- **External memory**

  The external memory is accessed in external memory expansion mode.

Figure 7-1. μPD784907 Memory Map



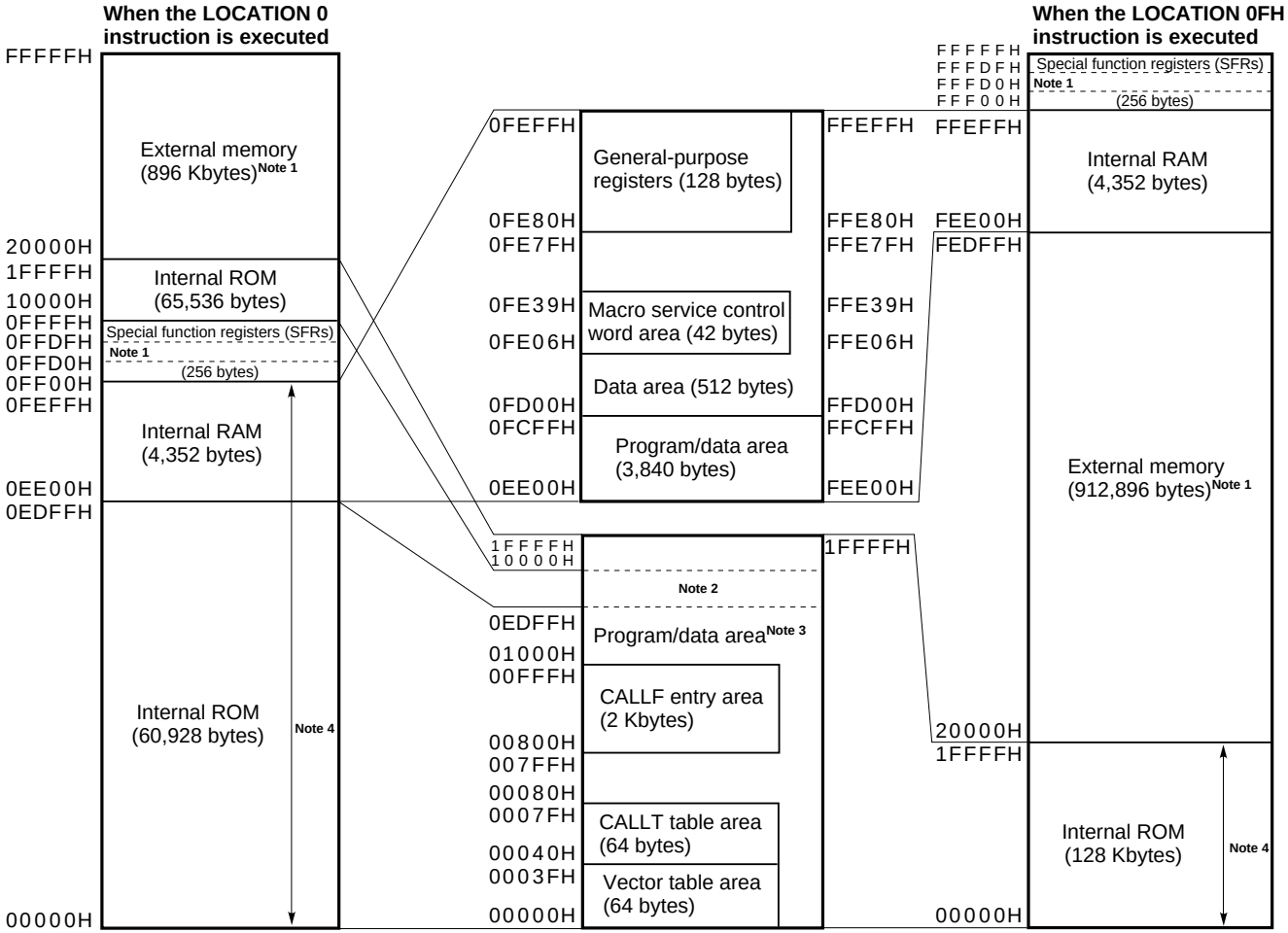
Notes 1. Accessed in external memory expansion mode.

2. This 3,840-byte area can be used as an internal ROM area only when the LOCATION 0FH instruction is executed.

3. When the LOCATION 0 instruction is executed: 94,464 bytes
When the LOCATION 0FH instruction is executed: 98,304 bytes

4. Base area and entry area based on a reset or interrupt. However, internal RAM is not used as a reset entry area.

Figure 7-2. μPD784908 Memory Map



Notes 1. Accessed in external memory expansion mode.

2. This 4,608-byte area can be used as an internal ROM area only when the LOCATION 0FH instruction is executed.

3. When the LOCATION 0 instruction is executed: 126,464 bytes
When the LOCATION 0FH instruction is executed: 131,072 bytes

4. Base area and entry area based on a reset or interrupt. However, internal RAM is not used as a reset entry area.

7.2 CPU Registers

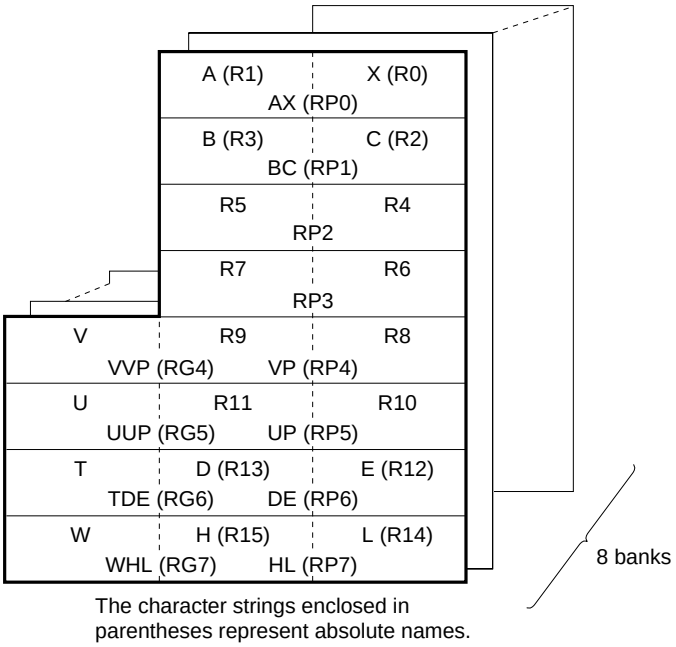
7.2.1 General-purpose registers

A set of general-purpose registers consists of sixteen 8-bit general-purpose registers. Two 8-bit general-purpose registers can be combined to form a 16-bit general-purpose register. Moreover, four 16-bit general-purpose registers, when combined with an 8-bit register for address extension, can be used as 24-bit address specification registers.

Eight banks of this register set are provided. The user can switch between banks by software or the context switching function.

General-purpose registers other than the V, U, T, and W registers used for address extension are mapped onto internal RAM.

Figure 7-3. General-Purpose Register Format



The character strings enclosed in parentheses represent absolute names.

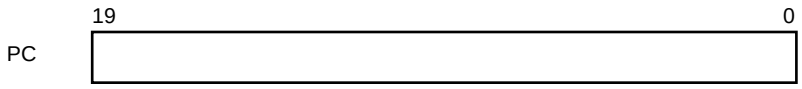
Caution By setting the RSS bit of PSW to 1, R4, R5, R6, R7, RP2, and RP3 can be used as the X, A, C, B, AX, and BC registers, respectively. However, this function must be used only when using programs for the 78K/III series.

7.2.2 Control registers

(1) Program counter (PC)

This register is a 20-bit program counter. The program counter is automatically updated by program execution.

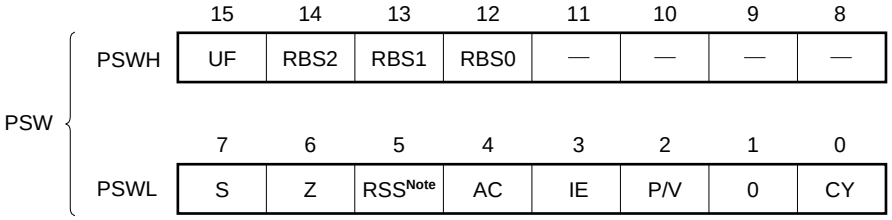
Figure 7-4. Format of Program Counter (PC)



(2) Program Status Word (PSW)

This register holds the CPU state. The program status word is automatically updated by program execution.

Figure 7-5. Format of Program Status Word (PSW)



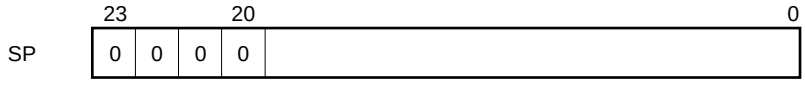
Note This flag is used to maintain compatibility with the 78K/III Series. This flag must be set to 0 when programs for the 78K/III Series are not being used.

(3) Stack pointer (SP)

This register is a 24-bit pointer for holding the start address of the stack.

The higher 4 bits must be set to 0.

Figure 7-6. Format of Stack Pointer (SP)



7.2.3 Special function registers (SFRs)

The special function registers are registers with special functions such as mode registers and control registers for built-in peripheral hardware. The special function registers are mapped onto the 256-byte space between 0FF00H and 0FFFFH[Note].

Note On execution of the LOCATION 0 instruction. FFF00H to FFFFFH when the LOCATION 0FH instruction is executed.

Caution Do not access an address in this area where no SFR is allocated, as the μPD784908 may be placed in the deadlock state. The deadlock state can be cleared only by a reset.

Table 7-1 lists the special function registers (SFRs). The symbols of the table columns are explained below.

- Symbol ..... Symbol indicating an on-chip SFR. The symbols listed in the table are reserved words for the NEC assembler (RA78K4). In the C compiler (CC78K4), the symbols can be used as sfr variables with the #pragma sfr command.
- R/W ..... Indicates whether the SFR is read-only, write-only, or read/write.
  R/W: Read/write
  R: Read-only.
  W: Write-only.
- Bit units for manipulation ..... Indicates the maximum number of bits that can be manipulated whenever an SFR is manipulated. An SFR that supports 16-bit manipulation can be described in the sfrp operand. For address specification, an even-numbered address must be specified.
  An SFR that can be manipulated in 1-bit units can be described as the operand of a bit manipulation instruction.
- After reset ..... Indicates the state of the register when the $\overline{\text{RESET}}$ signal has been input.

Table 7-1. Special Function Registers (SFRs) (1/5)

Address[Note]	Special Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 bit	8 bits	16 bits	
0FF00H	Port 0	P0		R/W	○	○	—	Undefined
0FF01H	Port 1	P1			○	○	—	
0FF02H	Port 2	P2		R	○	○	—	
0FF03H	Port 3	P3		R/W	○	○	—	
0FF04H	Port 4	P4			○	○	—	
0FF05H	Port 5	P5			○	○	—	
0FF06H	Port 6	P6			○	○	—	00H
0FF07H	Port 7	P7			○	○	—	Undefined
0FF09H	Port 9	P9			○	○	—	
0FF0AH	Port 10	P10			○	○	—	
0FF0EH	Port 0 buffer register L	P0L			○	○	—	
0FF0FH	Port 0 buffer register H	P0H			○	○	—	
0FF10H	Compare register (timer/counter 0)	CR00			—	—	○	
0FF12H	Capture/compare register (timer/counter 0)	CR01			—	—	○	
0FF14H	Compare register L (timer/counter 1)	CR10	CR10W		—	○	○	
0FF15H	Compare register H (timer/counter 1)	—			—	—		
0FF16H	Capture/compare register L (timer/counter 1)	CR11	CR11W		—	○	○	
0FF17H	Capture/compare register H (timer/counter 1)	—			—	—		
0FF18H	Compare register L (timer/counter 2)	CR20	CR20W		—	○	○	
0FF19H	Compare register H (timer/counter 2)	—			—	—		
0FF1AH	Capture/compare register L (timer/counter 2)	CR21	CR21W		—	○	○	
0FF1BH	Capture/compare register H (timer/counter 2)	—			—	—		
0FF1CH	Compare register L (timer 3)	CR30	CR30W		—	○	○	
0FF1DH	Compare register H (timer 3)	—			—	—		
0FF20H	Port 0 mode register	PM0			○	○	—	FFH
0FF21H	Port 1 mode register	PM1			○	○	—	
0FF23H	Port 3 mode register	PM3			○	○	—	
0FF24H	Port 4 mode register	PM4			○	○	—	
0FF25H	Port 5 mode register	PM5			○	○	—	
0FF26H	Port 6 mode register	PM6			○	○	—	
0FF27H	Port 7 mode register	PM7			○	○	—	
0FF29H	Port 9 mode register	PM9			○	○	—	
0FF2AH	Port 10 mode register	PM10			○	○	—	
0FF2EH	Real-time output port control register	RTPC			○	○	—	00H
0FF30H	Capture/compare control register 0	CRC0			—	○	—	10H
0FF31H	Timer output control register	TOC			○	○	—	00H
0FF32H	Capture/compare control register 1	CRC1			—	○	—	
0FF33H	Capture/compare control register 2	CRC2			—	○	—	10H

Note When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 7-1. Special Function Registers (SFRs) (2/5)

Address[Note]	Special Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 bit	8 bits	16 bits	
0FF36H	Capture register (timer/counter 0)	CR02		R	—	—	○	0000H
0FF38H	Capture register L (timer/counter 1)	CR12	CR12W		—	○	○	
0FF39H	Capture register H (timer/counter 1)	—			—	—		
0FF3AH	Capture register L (timer/counter 2)	CR22	CR22W		—	○	○	
0FF3BH	Capture register H (timer/counter 2)	—			—	—		
0FF41H	Port 1 mode control register	PMC1		R/W	○	○	—	00H
0FF43H	Port 3 mode control register	PMC3			○	○	—	
0FF4AH	Port 10 mode control register	PMC10			○	○	—	
0FF4EH	Register L for optional pull-up resistor	PUOL			○	○	—	
0FF4FH	Register H for optional pull-up resistor	PUOH			○	○	—	
0FF50H	Timer register 0	TM0		R	—	—	○	0000H
0FF51H				—	—			
0FF52H	Timer register 1	TM1	TM1W		—	○	○	
0FF53H		—			—	—		
0FF54H	Timer register 2	TM2	TM2W		—	○	○	
0FF55H		—			—	—		
0FF56H	Timer register 3	TM3	TM3W		—	○	○	
0FF57H		—			—	—		
0FF5CH	Prescaler mode register 0	PRM0		R/W	—	○	—	11H
0FF5DH	Timer control register 0	TMC0			○	○	—	00H
0FF5EH	Prescaler mode register 1	PRM1			—	○	—	11H
0FF5FH	Timer control register 1	TMC1			○	○	—	00H
0FF68H	A/D converter mode register	ADM			○	○	—	00H
0FF6AH	A/D conversion result register	ADCR		R	—	○	—	Undefined
0FF6CH	A/D current cut selection register	IEAD		R/W	○	○	—	00H
0FF6FH	Clock timer mode register	WM			○	○	—	
0FF70H	PWM control register	PWMC			○	○	—	05H
0FF71H	PWM prescaler register	PWPR			—	○	—	00H
0FF72H	PWM modulo register 0	PWM0			—	—	○	Undefined
0FF74H	PWM modulo register 1	PWM1			—	—	○	
0FF7DH	One-shot pulse output control register	OSPC			○	○	—	00H
0FF80H	Clocked serial interface mode register 3	CSIM3			○	○	—	
0FF82H	Clocked serial interface mode register	CSIM			○	○	—	

Note When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 7-1. Special Function Registers (SFRs) (3/5)

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FF84H	Clocked serial interface mode register 1	CSIM1	R/W	○	○	—	00H
0FF85H	Clocked serial interface mode register 2	CSIM2		○	○	—	
0FF86H	Serial shift register	SIO		—	○	—	Undefined
0FF88H	Asynchronous serial interface mode register	ASIM		○	○	—	00H
0FF89H	Asynchronous serial interface mode register 2	ASIM2		○	○	—	
0FF8AH	Asynchronous serial interface status register	ASIS	R	○	○	—	
0FF8BH	Asynchronous serial interface status register 2	ASIS2		○	○	—	
0FF8CH	Serial receive buffer: UART0	RXB		—	○	—	Undefined
	Serial transmission shift register: UART0	TXS	W	—	○	—	
	Serial shift register: IOE1	SIO1	R/W	—	○	—	
0FF8DH	Serial receive buffer: UART2	RXB2	R	—	○	—	
	Serial transmission shift register: UART2	TXS2	W	—	○	—	
	Serial shift register: IOE2	SIO2	R/W	—	○	—	
0FF8EH	Serial shift register 3: IOE3	SIO3		—	○	—	
0FF90H	Baud rate generator control register	BRGC		—	○	—	00H
0FF91H	Baud rate generator control register 2	BRGC2		—	○	—	
0FFA0H	External interrupt mode register 0	INTM0		○	○	—	
0FFA1H	External interrupt mode register 1	INTM1		○	○	—	
0FFA4H	Sampling clock selection register	SCS0		—	○	—	
0FFA8H	In-service priority register	ISPR	R	○	○	—	
0FFAAH	Interrupt mode control register	IMC	R/W	○	○	—	80H
0FFACH	Interrupt mask register 0L	MK0L MK0		○	○	○	FFFFH
0FFADH	Interrupt mask register 0H	MK0H		○	○		
0FFAEH	Interrupt mask register 1L	MK1L MK1		○	○	○	FFFFH
0FFAFH	Interrupt mask register 1H	MK1H		○	○		
0FFB0H	Bus control register	BCR		○	○	—	00H
0FFB2H	Unit address register	UAR		—	—	○	0000H
0FFB4H	Slave address register	SAR		—	—	○	
0FFB6H	Partner address register	PAR	R	—	—	○	
0FFB8H	Control data register	CDR	R/W	—	○	—	01H
0FFB9H	Telegraph length register	DLR		—	○	—	

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 7-1. Special Function Registers (SFRs) (4/5)

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FFBAH	Data register	DR	R/W	—	○	—	00H
0FFBBH	Unit status register	USR	R	○	○	—	
0FFBCH	Interrupt status register	ISR	R/W	○	○	—	
0FFBDH	Slave status register	SSR	R	○	○	—	41H
0FFBEH	Success count register	SCR		—	○	—	01H
0FFBFH	Communication count register	CCR		—	○	—	20H
0FFC0H	Standby control register	STBC	R/W	—	○[Note 2]	—	30H
0FFC2H	Watchdog timer mode register	WDM		—	○[Note 2]	—	00H
0FFC4H	Memory expansion mode register	MM		○	○	—	20H
0FFC5H	Hold mode register	HLDM		○	○	—	00H
0FFC6H	Clock output mode register	CLOM		○	○	—	
0FFC7H	Programmable wait control register 1	PWC1		—	○	—	AAH
0FFC8H	Programmable wait control register 2	PWC2		—	—	○	AAAAH
0FFCCH	Refresh mode register	RFM		○	○	—	00H
0FFCDH	Refresh area specification register	RFA		○	○	—	
0FFCFH	Oscillation stabilization time specification register	OSTS		—	○	—	
0FFD0H to 0FFDFH	External SFR area	—		○	○	—	—
0FFE0H	Interrupt control register (INTP0)	PIC0		○	○	—	43H
0FFE1H	Interrupt control register (INTP1)	PIC1		○	○	—	
0FFE2H	Interrupt control register (INTP2)	PIC2		○	○	—	
0FFE3H	Interrupt control register (INTP3)	PIC3		○	○	—	
0FFE4H	Interrupt control register (INTC00)	CIC00		○	○	—	
0FFE5H	Interrupt control register (INTC01)	CIC01		○	○	—	
0FFE6H	Interrupt control register (INTC10)	CIC10		○	○	—	
0FFE7H	Interrupt control register (INTC11)	CIC11		○	○	—	
0FFE8H	Interrupt control register (INTC20)	CIC20		○	○	—	
0FFE9H	Interrupt control register (INTC21)	CIC21		○	○	—	
0FFEAH	Interrupt control register (INTC30)	CIC30		○	○	—	
0FFEBH	Interrupt control register (INTP4)	PIC4		○	○	—	
0FFECH	Interrupt control register (INTP5)	PIC5		○	○	—	
0FFEDH	Interrupt control register (INTAD)	ADIC		○	○	—	
0FFEEH	Interrupt control register (INTSER)	SERIC		○	○	—	

Notes 1. When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

2. A write operation can be performed only with special instructions MOV STBC,#byte and MOV WDM,#byte. Other instructions cannot perform a write operation.

Table 7-1. Special Function Registers (SFRs) (5/5)

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FFEFH	Interrupt control register (INTSR)	SRIC	R/W	○	○	—	43H
	Interrupt control register (INTCSI1)	CSIIC1		○	○	—	
0FFF0H	Interrupt control register (INTST)	STIC		○	○	—	
0FFF1H	Interrupt control register (INTCSI)	CSIIC		○	○	—	
0FFF2H	Interrupt control register (INTSER2)	SERIC2		○	○	—	
0FFF3H	Interrupt control register (INTSR2)	SRIC2		○	○	—	
	Interrupt control register (INTCSI2)	CSIIC2		○	○	—	
0FFF4H	Interrupt control register (INTST2)	STIC2		○	○	—	
0FFF6H	Interrupt control register (INTIE1)	IEIC1		○	○	—	
0FFF7H	Interrupt control register (INTIE2)	IEIC2		○	○	—	
0FFF8H	Interrupt control register (INTW)	WIC		○	○	—	
0FFF9H	Interrupt control register (INTCSI3)	CSIIC3		○	○	—	
0FFFCH	Internal memory size switching register[Note 2]	IMS		—	○	—	FFH

Notes 1. When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

2. A write to this register is meaningful only for the μPD78P4908.

8. PERIPHERAL HARDWARE FUNCTIONS

8.1 Ports

The ports shown in Figure 8-1 are provided to make various control operations possible. Table 8-1 shows the functions of the ports. When inputting to port 0 to port 6, port 9, and port 10, an on-chip pull-up resistor can be specified by software.

Figure 8-1. Port Configuration

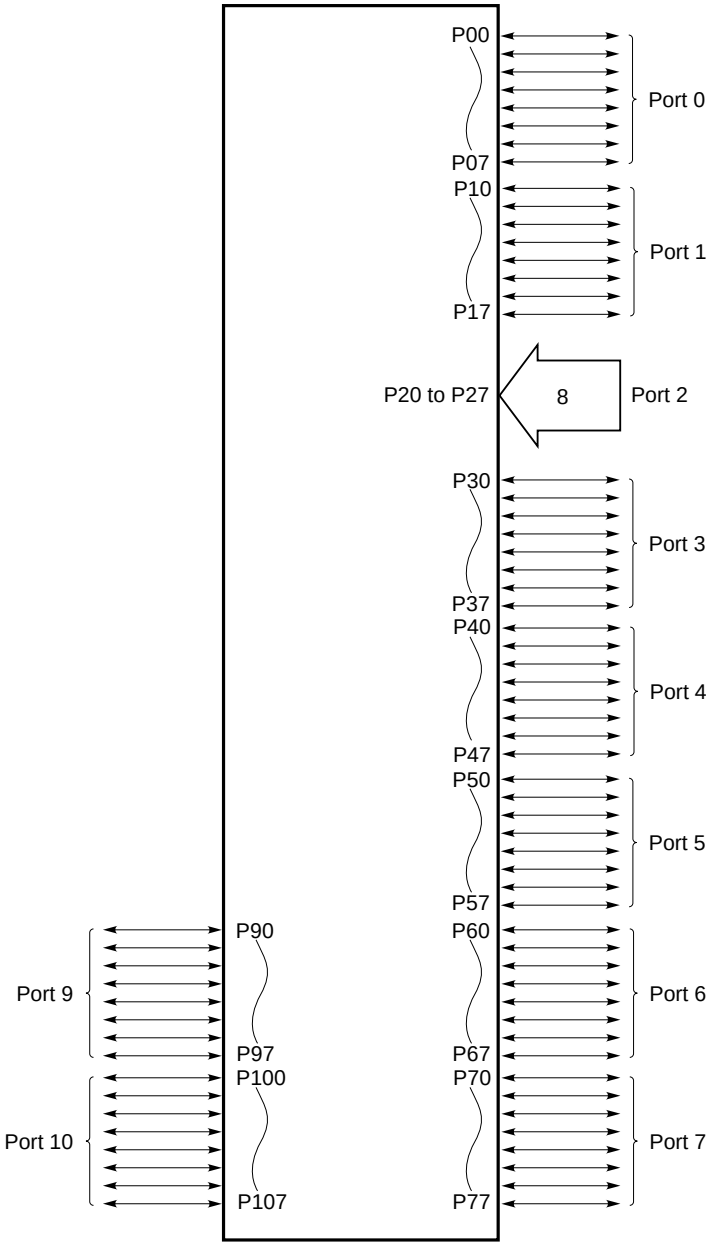


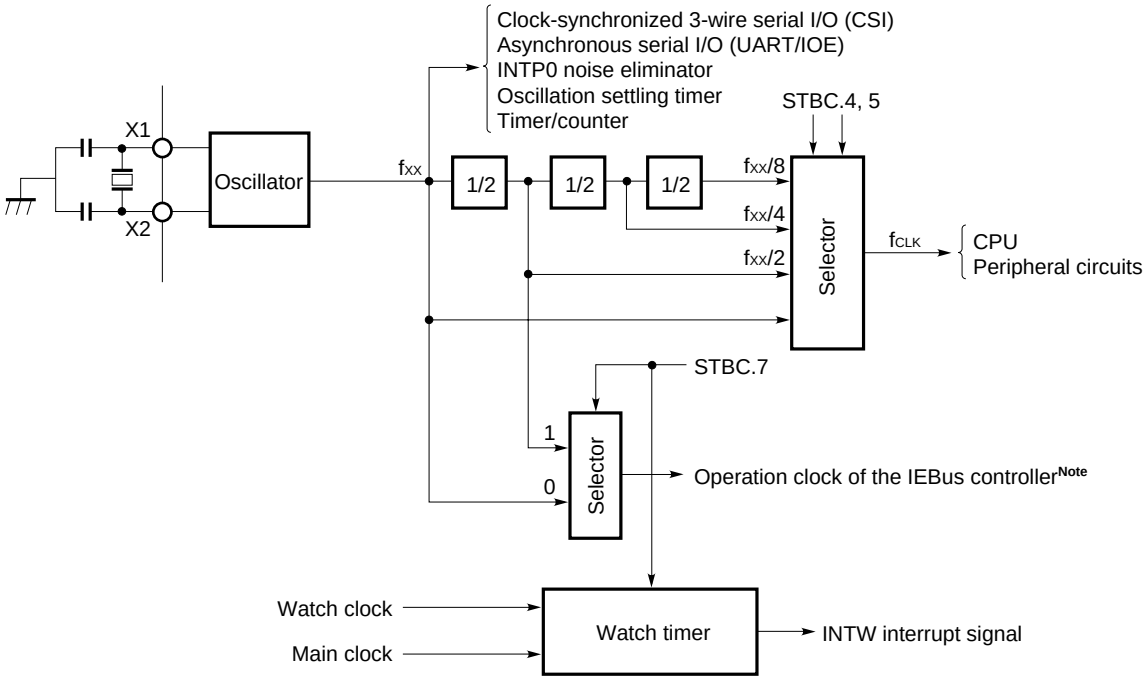
Table 8-1. Port Functions

Port Name	Pin Name	Function	Specification of Pull-up Resistor Connection by Software
Port 0	P00 to P07	• Input or output mode can be specified in 1-bit units • Operable as 4-bit real-time outputs (P00 to P03, P04 to P07) • Can drive transistors	All port pins in input mode
Port 1	P10 to P17	• Input or output mode can be specified in 1-bit units • Can drive LEDs	All port pins in input mode
Port 2	P20 to P27	• Input port	In 6-bit units (P22 through P27)
Port 3	P30 to P37	• Input or output mode can be specified in 1-bit units • Either pin P32/$\overline{\text{SCK0}}$ or P33/SO0 can be set as the N-ch open drain.	All port pins in input mode
Port 4	P40 to P47	• Input or output mode can be specified in 1-bit units • Can drive LEDs	All port pins in input mode
Port 5	P50 to P57	• Input or output mode can be specified in 1-bit units • Can drive LEDs	All port pins in input mode
Port 6	P60 to P67	• Input or output mode can be specified in 1-bit units	All port pins in input mode
Port 7	P70 to P77	• Input or output mode can be specified in 1-bit units	—
Port 9	P90 to P97	• Input or output mode can be specified in 1-bit units	All port pins in input mode
Port 10	P100 to P107	• Input or output mode can be specified in 1-bit units • Either pin P105/$\overline{\text{SCK3}}$ or P107/SO3 can be set as the N-ch open drain.	All port pins in input mode

8.2 Clock Generator

A circuit for generating the clock signal required for operation is provided. The clock generator has a frequency divider. If high-speed operation is not necessary, the internal operating frequency can be lowered by the frequency divider to reduce the current consumption.

Figure 8-2. Block Diagram of Clock Generator

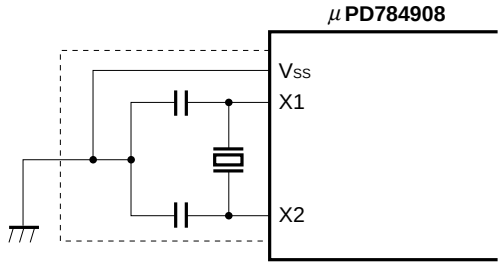


Note Set bit 7 of the standby control register (STBC) to 1.

Remark f_{XX}: Oscillator frequency or external clock input frequency
f_{CLK}: Internal operating frequency

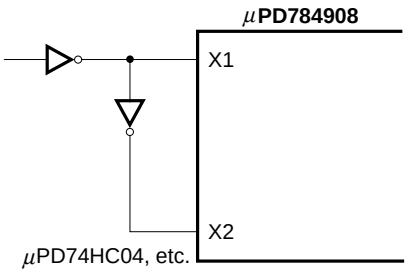
Figure 8-3. Examples of Using Oscillator

(1) Crystal/ceramic oscillation

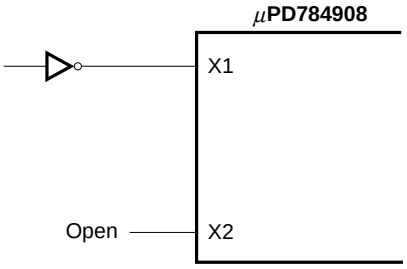


(2) External clock

- When EXTC bit of OSTS = 1



- When EXTC bit of OSTS = 0



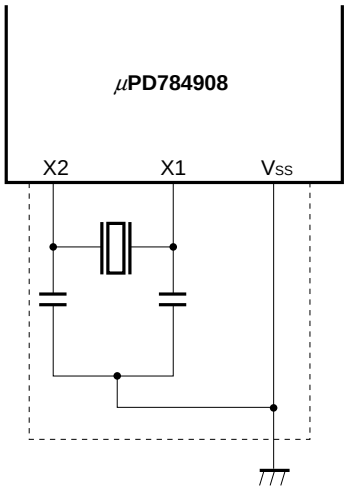
Caution When using the clock generator, wire in the area enclosed by the broken lines to avoid adverse influence from capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Make the ground point of the oscillator capacitor the same potential as VSS. Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

Compared with the main system clock oscillator, the watch clock oscillator, which is a low-gain circuit designed to reduce current consumption, is more likely to cause noise-induced malfunctions. Therefore, special care should be taken when using the watch clock oscillator.

The microcontroller can operate normally only when the oscillation is normal and stable. If a high-precision oscillator frequency is required, consult with the oscillator manufacturer.

Figure 8-4. Notes on Connecting the Oscillator



Cautions 1. Place the oscillator as close as possible to pins X1 and X2 (XT1 and XT2).

2. Do not let other signal lines cross that part of the circuit enclosed in broken lines.

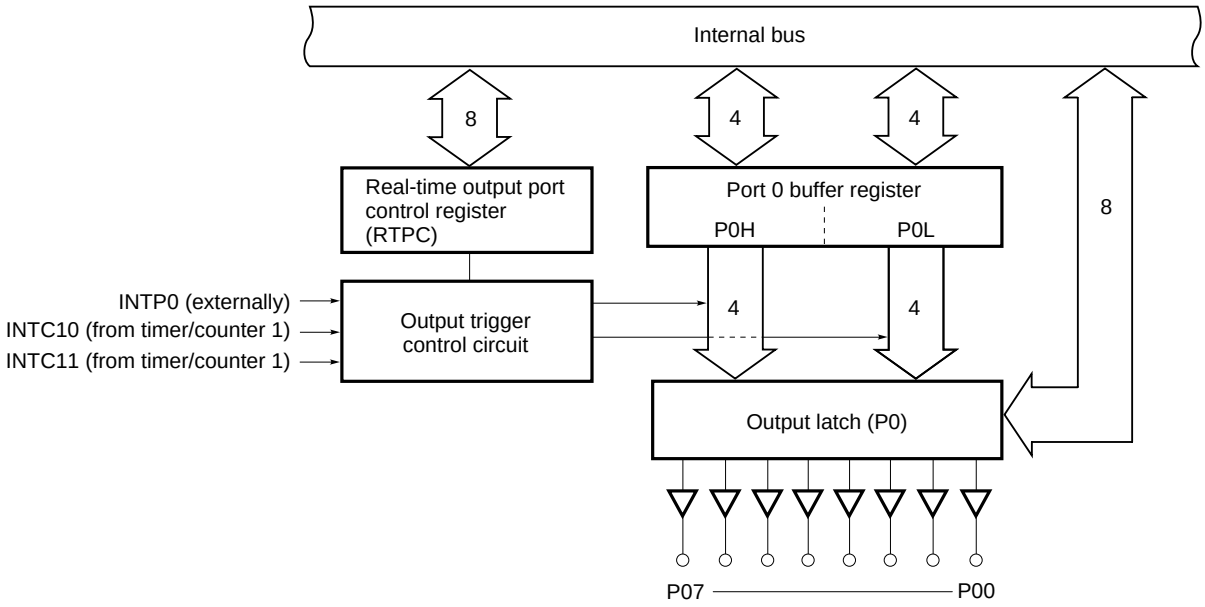
8.3 Real-Time Output Port

The real-time output port outputs data stored in the buffer, synchronized with a timer/counter 1 match interrupt or external interrupt. Thus, pulse output that is free of jitter can be obtained.

Therefore, the real-time output port is best suited to applications (such as open-loop control over stepping motors) where an arbitrary pattern is output at arbitrary intervals.

As shown in Figure 8-5, the real-time output port is built around port 0 and the port 0 buffer register (P0H, P0L).

Figure 8-5. Block Diagram of Real-Time Output Port



8.4 Timers/Counters

Three timer/counter units and one timer unit are incorporated.

Moreover, because seven interrupt requests are supported, these timers/counters can be used as seven timer/counter units.

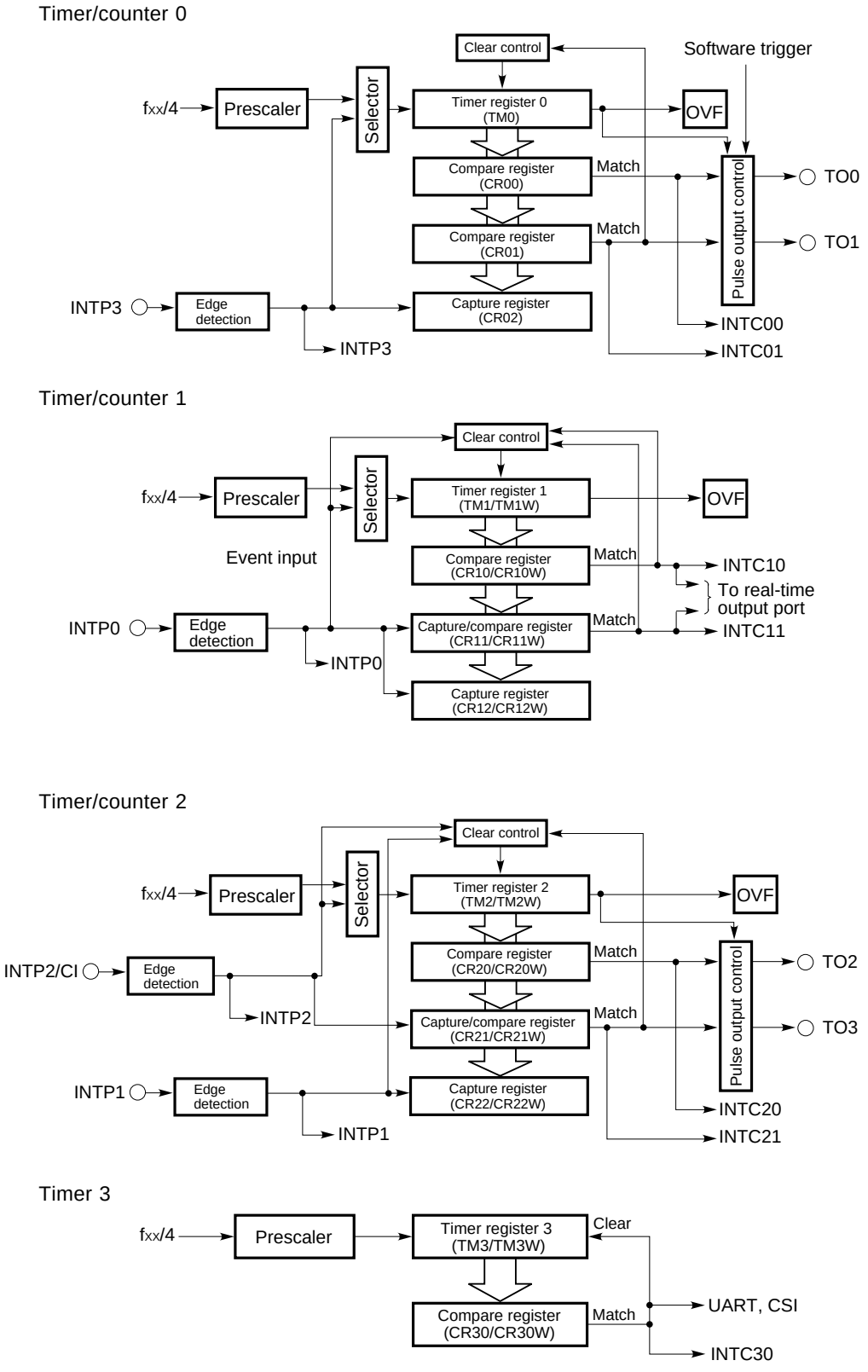
Table 8-2. Timers/Counters Operation

Item \ Name		Timer/Counter 0	Timer/Counter 1	Timer/Counter 2	Timer 3
Count width	8 bits	—	○	○	○
	16 bits	○	○	○	○
Operating mode	Interval timer	2 ch	2 ch	2 ch	1 ch
	External event counter	○	○	○	—
	One-shot timer	—	—	○	—
Function	Timer output	2 ch	—	2 ch	—
	Toggle output	○	—	○	—
	PWM/PPG output	○	—	○	—
	One-shot pulse output[Note]	○	—	—	—
	Real-time output	—	○	—	—
	Pulse width measurement	1 input	1 input	2 inputs	—
	Number of interrupt requests	2	2	2	1

Note The one-shot pulse output function makes the level of a pulse output active by software, and makes the level of a pulse output inactive by hardware (interrupt request signal).

Note that this function differs from the one-shot timer function of timer/counter 2.

Figure 8-6. Timer/Counter Block Diagram



Remark OVF: Overflow flag

8.5 Watch Timer

★ As the count clock, either of two types of clock can be input to the watch timer: the main clock (6.29 MHz/12.58 MHz) or the watch clock (32.768 kHz). They can be selected using the control register. The watch clock is input to the watch timer only. It is not input to the CPU or other peripheral circuits. Therefore, the speed of CPU operation cannot be slowed by the watch clock.

The watch timer generates interrupt signals (INTW), at 0.5-second intervals**Note**, by dividing the count clock. At the same time, the watch timer sets the interrupt request flag (WIF) (where WIF refers to bit 7 of the interrupt control register (WIC)).

By switching modes, the INTW generation interval can be changed to about 1 ms (fast-forward mode: normal operation speed × 512).

When the main clock is selected as the count clock, the watch timer stops if in STOP or IDLE standby mode, but continues operating if in HALT standby mode. When the watch clock is selected as the count clock, the watch timer continues operating regardless of the standby mode. The operation of the watch clock oscillator is controlled by means of the watch timer mode register (WM).

The watch timer of the μPD784908 does not have a buzzer output function.

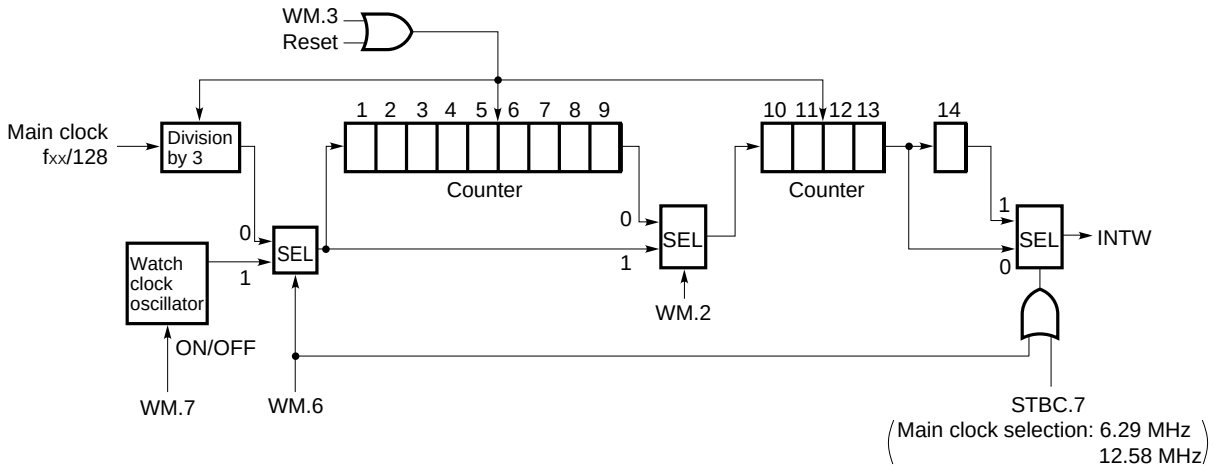
Note After the operation is enabled, the time until first INTW generation is not 0.5 s.

Table 8-3. Relationship between Count Clock and Watch Timer Operation

Count Clock Selection	Normal Operation Mode	Standby Modes		
		HALT mode	STOP mode	IDLE mode
Main clock	Operable	Operable	Stopped	Stopped
Watch clock	Operable	Operable	Operable	Operable

The watch timer consists of a frequency divider which divides the count clock by 3 and a counter which divides the frequency output from the frequency divider by 2^{14}. As the count clock, select the signal obtained by dividing the internal system clock by 128 or that output by the watch clock oscillator.

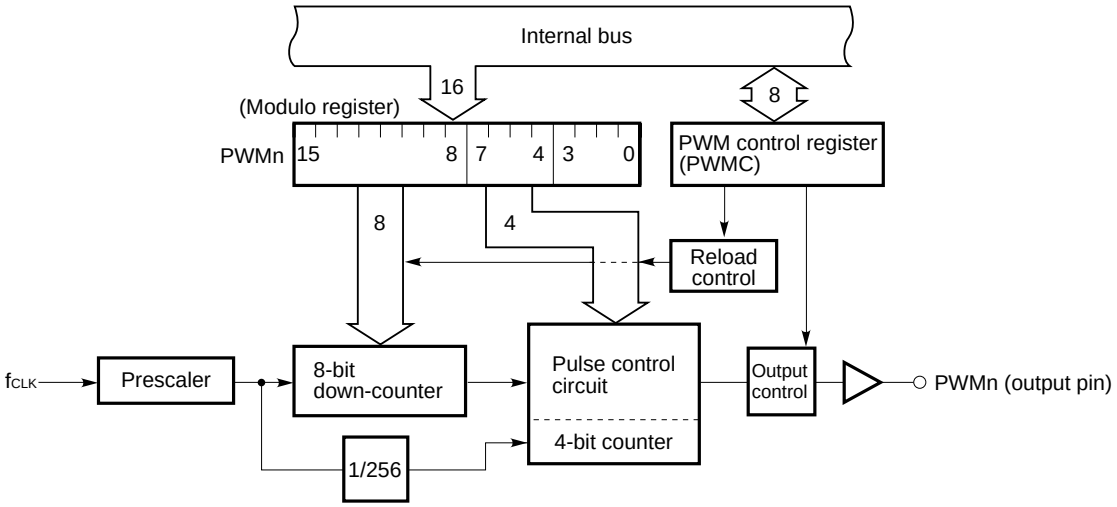
★ **Figure 8-7. Watch Timer Block Diagram**



8.6 PWM Output (PWM0, PWM1)

Two channels of PWM (pulse width modulation) output circuitry with a resolution of 12 bits and a repetition frequency of 24.57 kHz (fCLK = 6.29 MHz) are incorporated. Low or high active level can be selected for the PWM output channels, independently of each other. This output is best suited to DC motor speed control.

Figure 8-8. Block Diagram of PWM Output Unit



Remark n = 0, 1

8.7 A/D Converter

An analog/digital (A/D) converter having 8 multiplexed analog inputs (ANI0 through ANI7) is incorporated.

The successive approximation system is used for conversion. The result of conversion is held in the 8-bit A/D conversion result register (ADCR). Thus, speedy high-precision conversion can be achieved.

A/D conversion can be started in the following two ways:

- Hardware start: Conversion is started by trigger input (INTP5).
- Software start: Conversion is started by setting the bit of the A/D converter mode register (ADM).

After conversion has started, one of the following modes can be selected:

- Scan mode: Multiple analog inputs are selected sequentially to convert multiple pins.
- Select mode: A single analog input is selected at all times to enable conversion data to be obtained continuously.

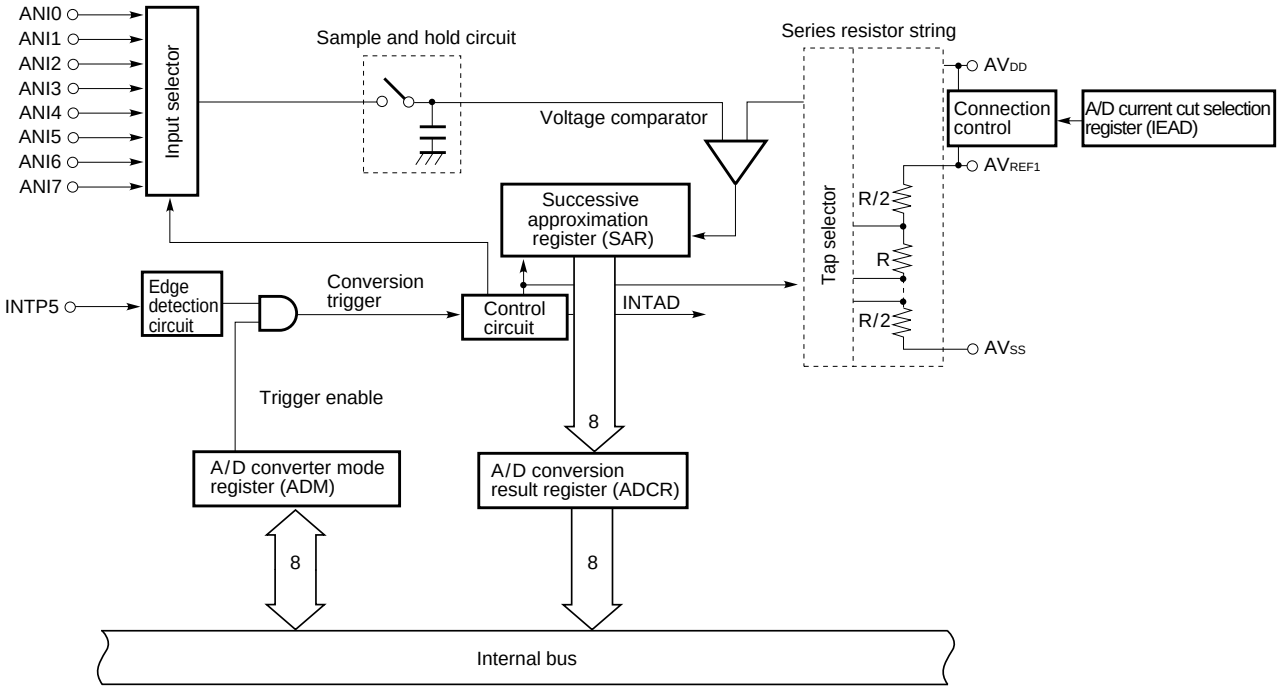
ADM is used to specify the above modes, as well as the termination of conversion.

When the result of conversion is transferred to ADCR, an interrupt request (INTAD) is generated. Using this feature, the results of conversion can be continuously transferred to memory by the macro service.

Cautions 1. For this product, apply the same voltage as the power supply voltage (AV_{DD}) to the reference voltage input pin (AV_{REF1}).

2. When port 7 is used as both an output port and A/D input line, do not manipulate the output port while A/D conversion is in progress.

Figure 8-9. Block Diagram of A/D Converter



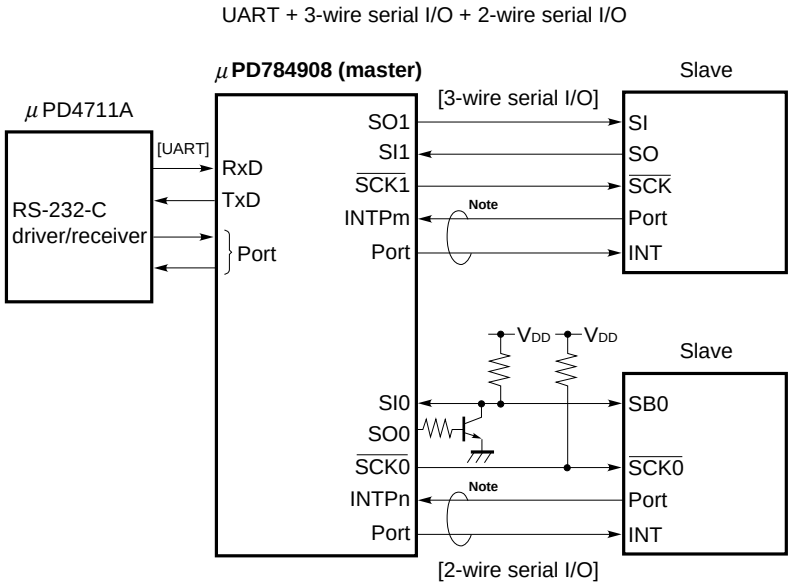
8.8 Serial Interface

Four independent serial interface channels are incorporated.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Synchronous serial interface (CSI) × 2
  - 3-wire serial I/O (IOE)

This makes it possible for communication with an external system and local communication within the system to be simultaneously executed (see **Figure 8-10**).

Figure 8-10. Example of Serial Interface



Note Handshake line

8.8.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two serial interface channels, from which asynchronous serial interface mode and 3-wire serial I/O mode can be selected, are provided.

(1) Asynchronous serial interface mode

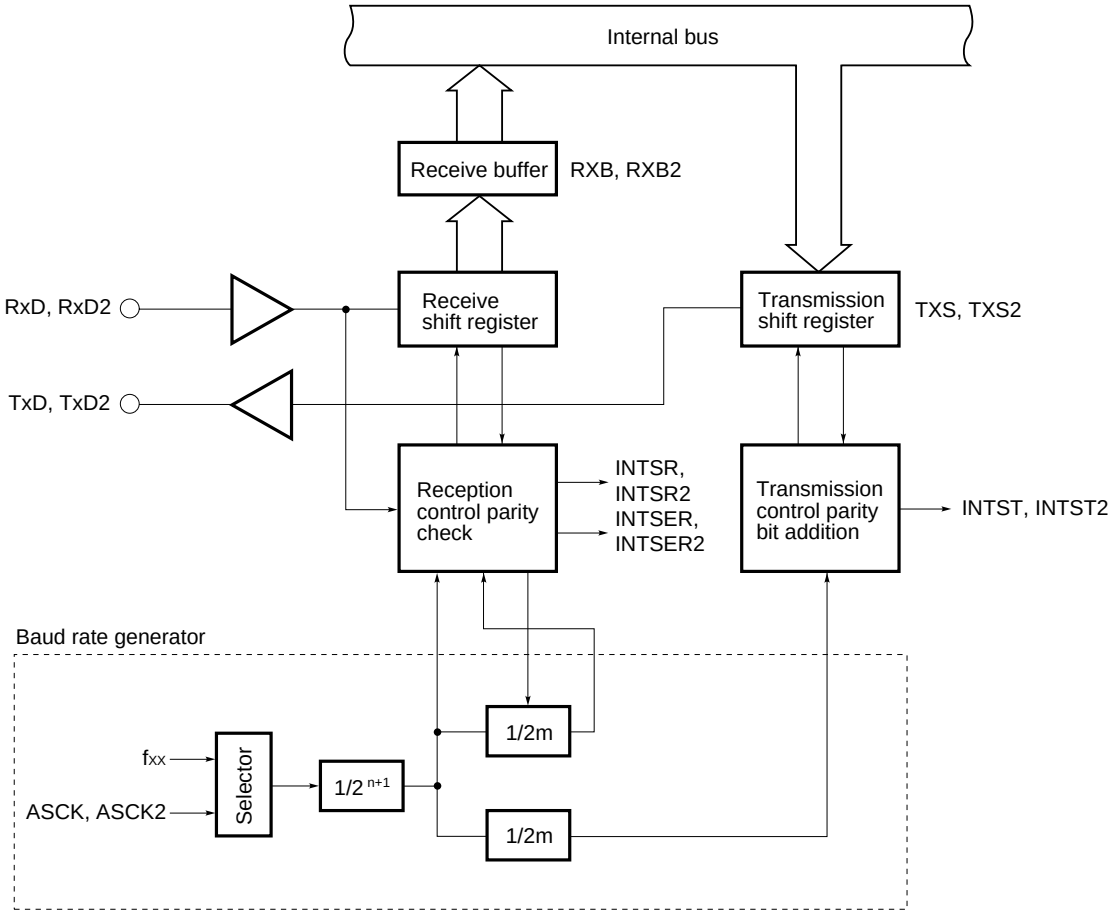
In this mode, 1-byte data is transferred or received after a start bit.

A baud rate generator is incorporated to enable communication at a wide range of baud rates.

A baud rate can be defined by dividing the frequency of a clock signal input to the ASCK pin.

By using the baud rate generator, a baud rate conforming to the MIDI standard (31.25 kbps) can be obtained.

Figure 8-11. Block Diagram of Asynchronous Serial Interface Mode



Remark f_{XX}: Oscillating frequency or external clock input frequency

n = 0 to 11

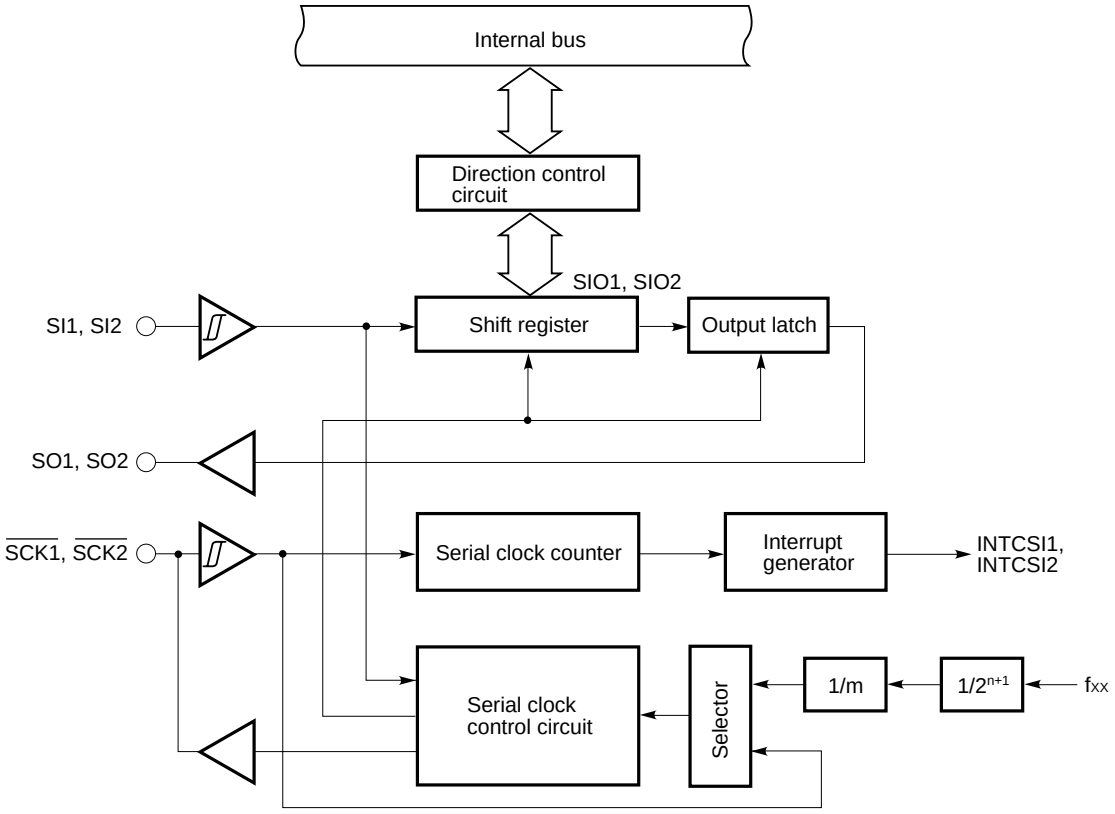
m = 16 to 30

(2) 3-wire serial I/O mode

In this mode, the master device makes the serial clock active to start transmission, then transfers 1-byte data in synchronization with this clock.

This mode is designed for communication with a device incorporating a conventional synchronous serial interface. Basically, three lines are used for communication: the serial clock line ($\overline{SCK}$) and the two serial data lines (SI and SO). In general, a handshake line is required to check the state of communication.

Figure 8-12. Block Diagram of 3-Wire Serial I/O Mode



Remark f_{XX}: Oscillating frequency or external clock input frequency

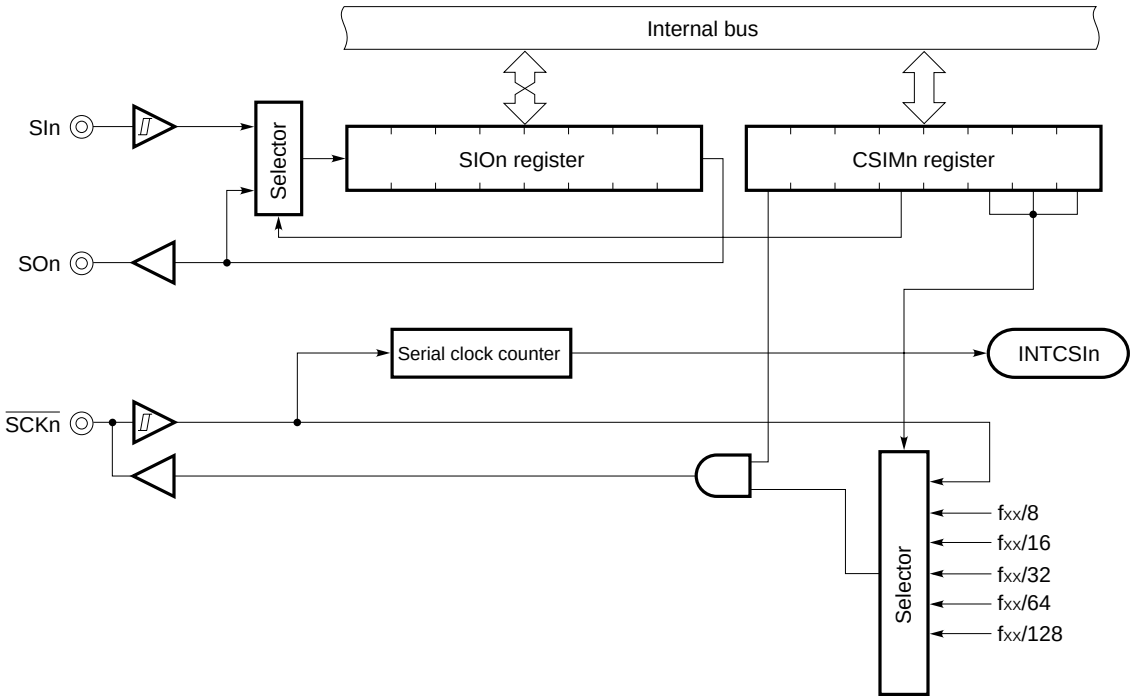
n = 0 to 11

m = 1, 16 to 30

8.8.2 Clocked serial interface (CSI)

With this interface, the master device makes the serial clock active to start transmission, then transfers 1-byte data in synchronization with this clock.

Figure 8-13. Block Diagram of Clocked Serial Interface



Remark fXX: Oscillating frequency or external clock input frequency
n = 0, 3

- **3-wire serial I/O mode**

  This mode is designed for communication with a device incorporating a conventional clocked serial interface. Basically, three lines are used for communication: the serial clock line ($\overline{SCKn}$) and serial data lines (SIn and SOn) (n = 0, 3).

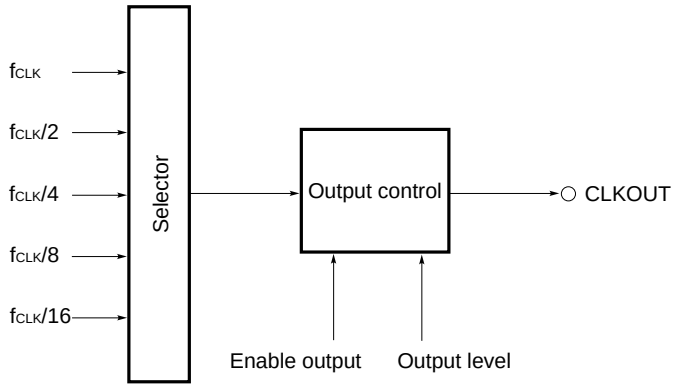
  In general, a handshake line is required to check the state of communication.

8.9 Clock Output Function

The frequency of the CPU clock signal can be divided and output from the system. Moreover, the port can be used as a 1-bit port.

The ASTB pin is also used as the CLKOUT pin, so that when this function is used, the local bus interface cannot be used.

Figure 8-14. Block Diagram of Clock Output Function



8.10 Edge Detection Function

The interrupt input pins (NMI, INTP0 through INTP5) are used not only to input interrupt requests but also to input trigger signals to the internal hardware units. Because these pins operate at the edge of the input signal, they have an edge-detection function incorporated. Moreover, a noise elimination function is also provided to prevent erroneous edge detection caused by noise.

Table 8-4. Noise Elimination Method of Interrupt Input Pins

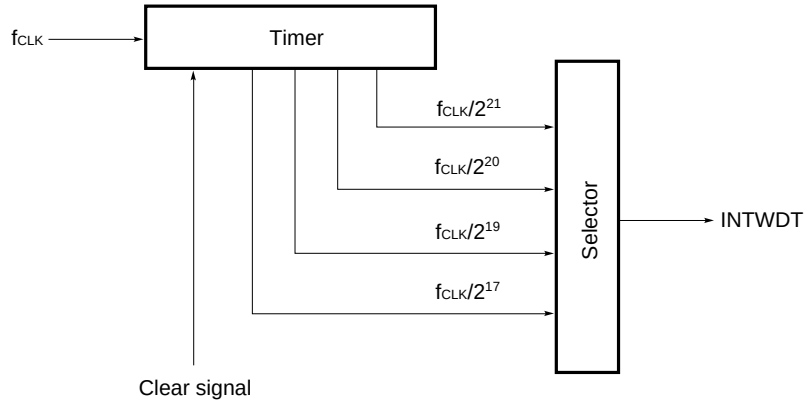
Pin Name	Detectable Edge	Noise Elimination Method
NMI	Rising edge or falling edge	Analog delay
INTP0 to INTP3	Rising edge or falling edge, or both edges	Clock sampling[Note]
INTP4, INTP5		Analog delay

Note INTP0 is used for sampling clock selection.

8.11 Watchdog Timer

A watchdog timer is incorporated to detect a CPU runaway. The watchdog timer, if not cleared by software within a specified interval, generates a non-maskable interrupt request. Furthermore, once watchdog timer operation is enabled, it cannot be disabled by software. The user can specify whether priority is placed on an interrupt request based on the watchdog timer or on an interrupt request based on the NMI pin.

Figure 8-15. Block Diagram of Watchdog Timer



8.12 Simplified IEBus Controller

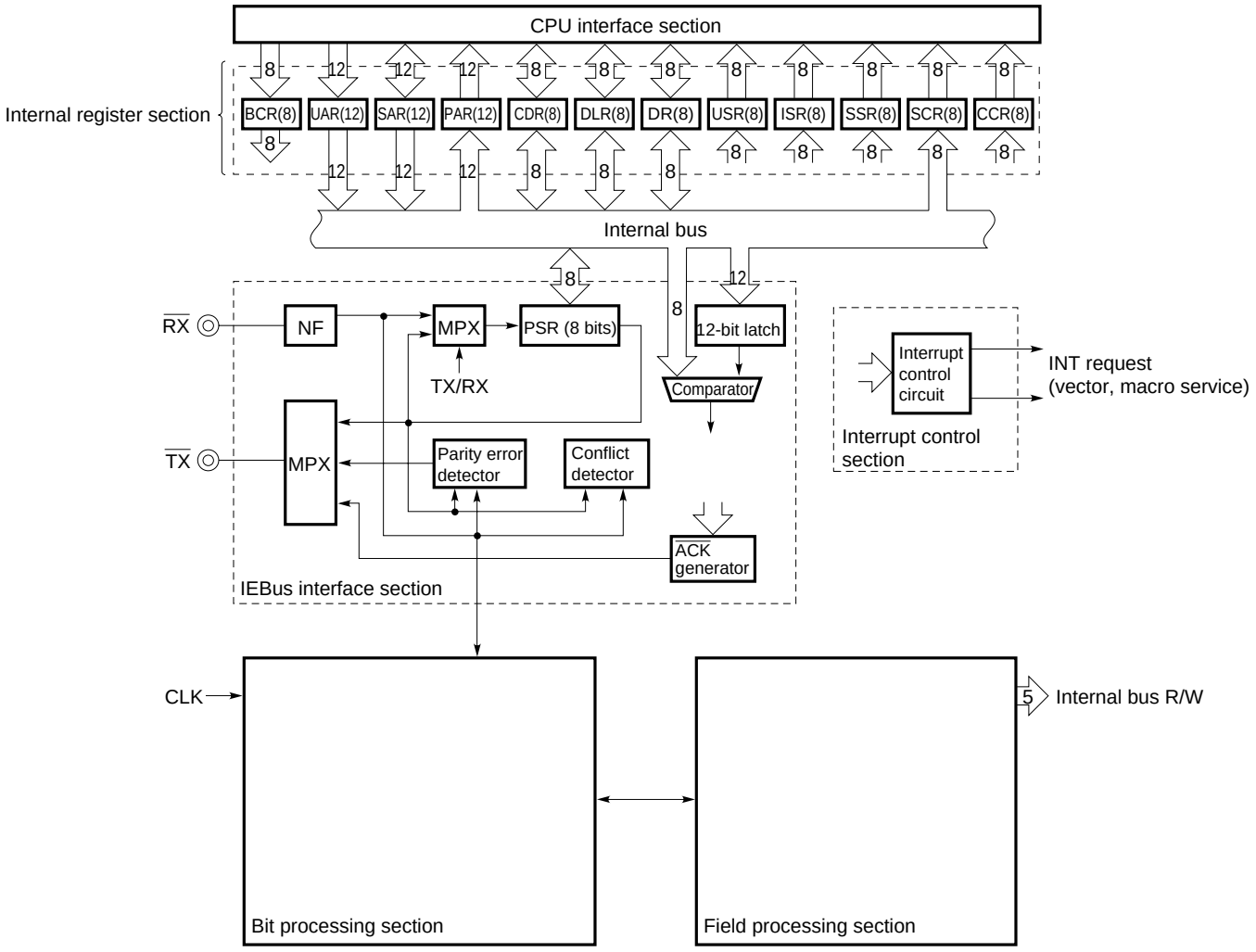
A newly developed IEBus controller is incorporated into the μPD784908. This IEBus controller has fewer functions than the IEBus interface function of previous product (incorporated into the 78K/0).

Table 8-5 compares the previous product and the new, simplified IEBus interface.

Table 8-5. Comparisons between Previous Product and Simplified IEBus Interface

Item	Previous Product (IEBus Incorporated into 78K/0)	Simplified IEBus
Communication mode	Modes 0 to 2	Fixed to mode 1
Internal system clock	6.0 (6.29) MHz	
Internal buffer size	Transmission buffer 33 bytes (FIFO) Reception buffer 40 bytes (FIFO) Up to four frames can be received	Transmission/reception data register 1 byte
CPU processing	Processing before transmission start (data setting) Setting and control of each communication status Data write to the transmission buffer Data read from the reception buffer	Processing before transmission start (data setting) Setting and control of each communication status Data write processing for every byte Data read processing for every byte Transmission control such as slave status Control of multiple frames, remastering request
Hardware processing	Bit processing (modulation/demodulation, error detection) Field processing (generation, control) Detection of arbitration results Parity processing (generation, error detection) ACK/NACK automatic response Automatic data retransmitting Automatic remastering Transmission such as automatic slave status Reception of multiple frames	Bit processing (modulation/demodulation, error detection) Field processing (generation, control) Detection of arbitration results Parity processing (generation, error detection) ACK/NACK automatic response Automatic data retransmitting

Figure 8-16. IEBus Controller



- Hardware configuration and functions

  The internal configuration of the IEBus consists mainly of the following six sections:

  - CPU interface section
  - Interrupt control section
  - Internal register section
  - Bit processing section
  - Field processing section
  - IEBus interface section

<CPU interface section>

Interfaces between the CPU (78K/IV) and the IEBus.

<Interrupt control section>

Passes interrupt request signals from the IEBus to the CPU.

<Internal register section>

Control register which stores the data in each field to control the IEBus.

<Bit processing section>

Generates and resolves the bit timing. Mainly consists of the bit sequence ROM, 8-bit preset timer, and discriminator.

<Field processing section>

Generates each field in the communication frame. Mainly consists of the field sequence ROM, 4-bit down counter, and discriminator.

<IEBus interface section>

Interface section of the external driver/receiver. Mainly consists of the noise filter, shift register, conflict detector, parity detector, parity generator, and $\overline{\text{ACK}}$/NACK generator.

9. INTERRUPT FUNCTION

The three types of interrupt request-response servicing, as shown in Table 9-1 below, can be selected by program.

Table 9-1. Servicing of Interrupt Request

Servicing Mode	Servicing Agent	Servicing	PC and PSW Contents
Vectored interrupt	Software	Branches and executes a servicing routine (servicing is arbitrary).	Saves to and restores from the stack.
Context switching		Automatically switches register banks, and branches and executes a servicing routine (servicing is arbitrary).	Saves to or restores from fixed area in the register bank.
Macro service	Firmware	Executes data transfer between memory and I/O (servicing is fixed).	Maintained

9.1 Interrupt Source

Table 9-2 shows the interrupt sources available. As shown, interrupts are generated by 27 types of sources, execution of the BRK and BRKCS instructions, or an operand error.

Four levels of interrupt servicing priority can be set. Priority levels can be set to nest control during interrupt servicing or to simultaneously generate interrupt requests. However, nested macro services are performed without suspension.

When interrupt requests having the same priority level are generated, they are serviced according to the default priority (fixed) (see **Table 9-2**).

Table 9-2. Interrupt Source

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK instruction	Instruction execution	—	—
		BRKCS instruction	Instruction execution		
		Operand error	When the MOV STBC,#byte, MOV WDM,#byte, or LOCATION instruction is executed, exclusive OR of the byte operand and $\overline{byte}$ does not produce FFH.		
Non-maskable	—	NMI	Detection of edge input on the pin	External	—
		WDT	Watchdog timer overflow	Internal	
Maskable	0 (highest)	INTP0	Detection of edge input on the pin (TM1/TM1W capture trigger)	External	√
	1	INTP1	Detection of edge input on the pin (TM2/TM2W capture trigger)		
	2	INTP2	Detection of edge input on the pin (TM2/TM2W event counter input)		
	3	INTP3	Detection of edge input on the pin (TM0 capture trigger)		
	4	INTC00	TM0-CR00 match signal issued	Internal	√
	5	INTC01	TM0-CR01 match signal issued		
	6	INTC10	TM1-CR10 match signal issued (in 8-bit operation mode) TM1W-CR10W match signal issued (in 16-bit operation mode)		
	7	INTC11	TM1-CR11 match signal issued (in 8-bit operation mode) TM1W-CR11W match signal issued (in 16-bit operation mode)		
	8	INTC20	TM2-CR20 match signal issued (in 8-bit operation mode) TM2W-CR20W match signal issued (in 16-bit operation mode)		
	9	INTC21	TM2-CR21 match signal issued (in 8-bit operation mode) TM2W-CR21W match signal issued (in 16-bit operation mode)		
	10	INTC30	TM3-CR30 match signal issued (in 8-bit operation mode) TM3W-CR30W match signal issued (in 16-bit operation mode)		
	11	INTP4	Detection of edge input on the pin	External	√
	12	INTP5	Detection of edge input on the pin (A/D converter start conversion trigger)		
	13	INTAD	A/D converter processing completed (ADCR transfer)	Internal	√
	14	INTSER	ASI0 reception error		—
	15	INTSR	ASI0 reception completed or CSI1 transfer completed		√
		INTCSI1			
	16	INTST	ASI0 transmission completed		
	17	INTCSI	CSI0 transfer completed		
	18	INTSER2	ASI2 reception error		—
	19	INTSR2	ASI2 reception completed or CSI2 transfer completed		√
		INTCSI2			
	20	INTST2	ASI2 transmission completed		
	21	INTIE1	IEBus data access request		
	22	INTIE2	IEBus communication error and communication start/end		
	23	INTW	Clock timer output		
	24 (lowest)	INTCSI3	CSI3 transfer completed		

Remark ASI: Asynchronous serial interface
CSI: Clocked serial interface

9.2 Vectored Interrupt

When a branch to an interrupt servicing routine occurs, the vector table address corresponding to the interrupt source is used as the branch address.

Interrupt servicing by the CPU consists of the following operations :

- When branching: Saves the CPU status (PC and PSW contents) to the stack.
- When returning: Restores the CPU status (PC and PSW contents) from the stack.

To return control from the servicing routine to the main routine, the RETI instruction is used.

The branch destination addresses must be within the range of 0 to FFFFH.

Table 9-3. Vector Table Address

Interrupt Source	Vector Table Address
BRK instruction	003EH
Operand error	003CH
NMI	0002H
WDT	0004H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	000EH
INTC01	0010H
INTC10	0012H
INTC11	0014H
INTC20	0016H
INTC21	0018H
INTC30	001AH
INTP4	001CH
INTP5	001EH
INTAD	0020H
INTSER	0022H
INTSR	0024H
INTCSI1	
INTST	0026H
INTCSI	0028H
INTSER2	002AH
INTSR2	002CH
INTCSI2	
INTST2	002EH

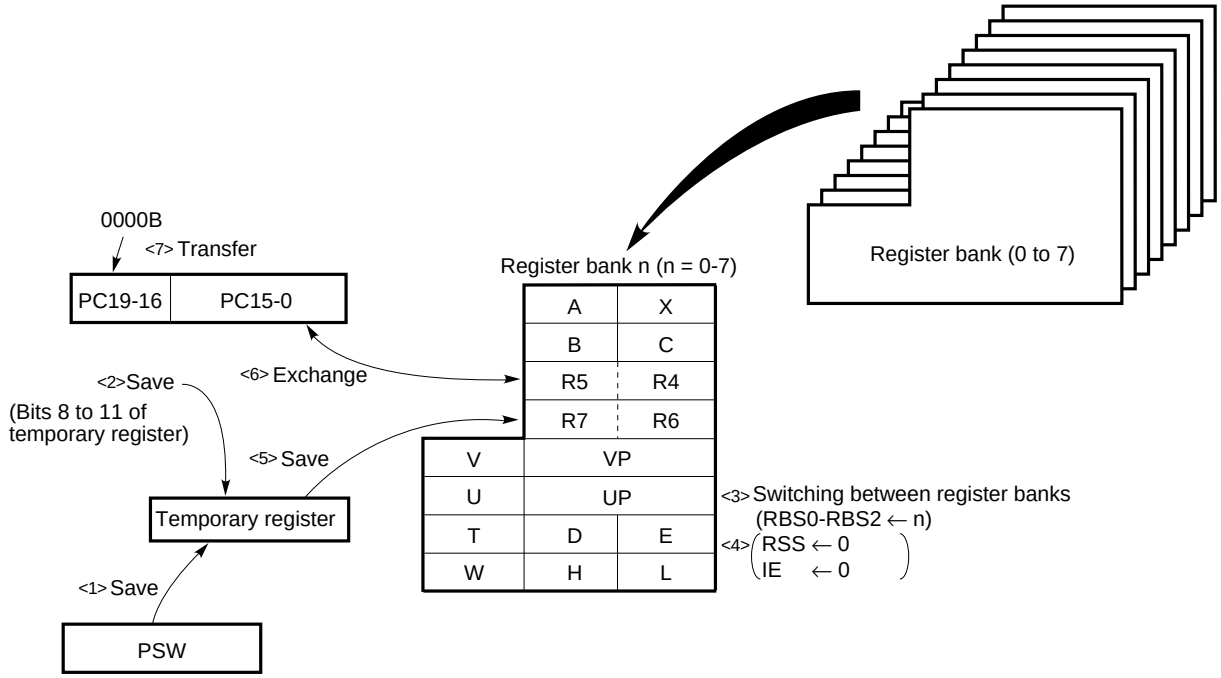
Interrupt Source	Vector Table Address
NTIE1	0032H
INTIE2	0034H
INTW	0036H
INTCSI3	0038H

9.3 Context Switching

When an interrupt request is generated, or when the BRKCS instruction is executed, a predetermined register bank is selected by the hardware. Then, a branch to a vector address stored in that register bank occurs. At the same time, the contents of the current program counter (PC) and program status word (PSW) are stacked in the register bank.

The branch address must be within the range of 0 to FFFFH.

Figure 9-1. Context Switching Operation When Interrupt Request Is Generated

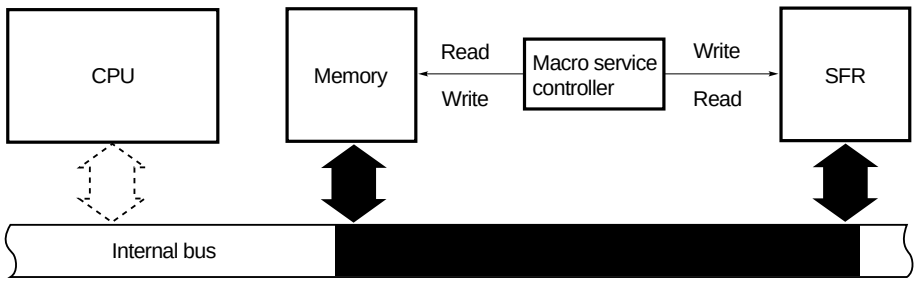


9.4 Macro Service

The macro service function enables data transfer between memory and special function registers (SFRs) without requiring the intervention of the CPU. The macro service controller accesses both memory and SFRs within the same transfer cycle to directly transfer data without having to perform data fetch.

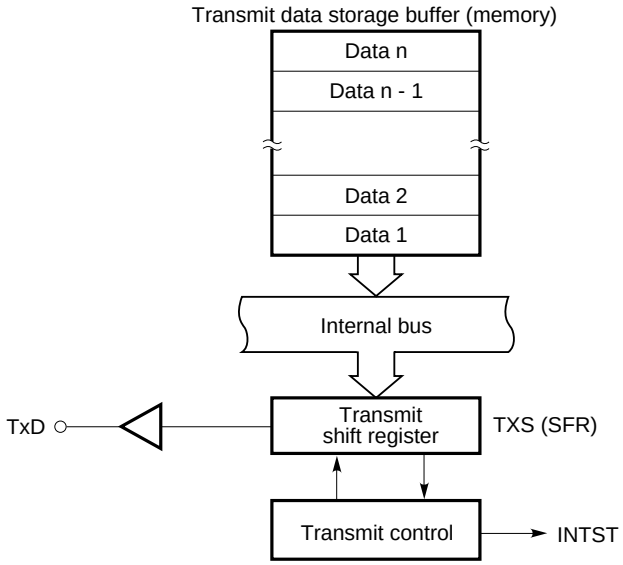
Since the CPU status is neither saved nor restored, nor is data fetch performed, high-speed data transfer is possible.

Figure 9-2. Macro Service



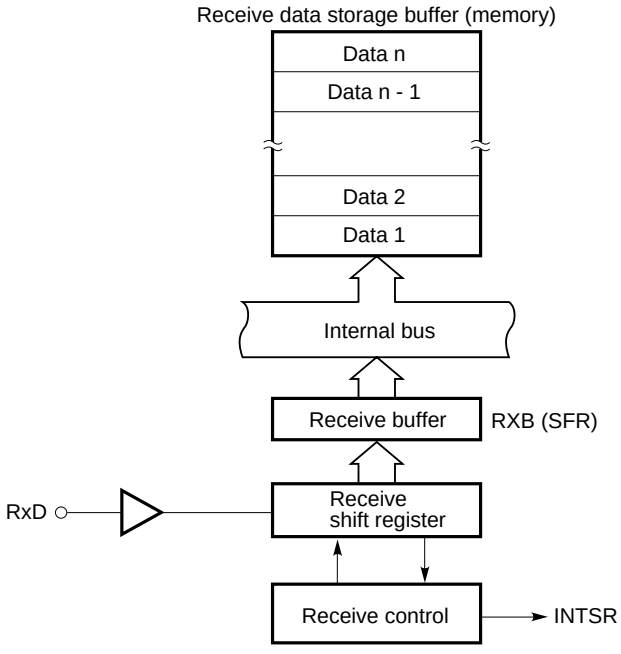
9.5 Examples of Macro Service Applications

(1) Serial interface transmission



Each time macro service request (INTST) is generated, the next transmit data is transferred from memory to TXS. When data n (last byte) has been transferred to TXS (that is, once the transmit data storage buffer becomes empty), vectored interrupt request (INTST) is generated.

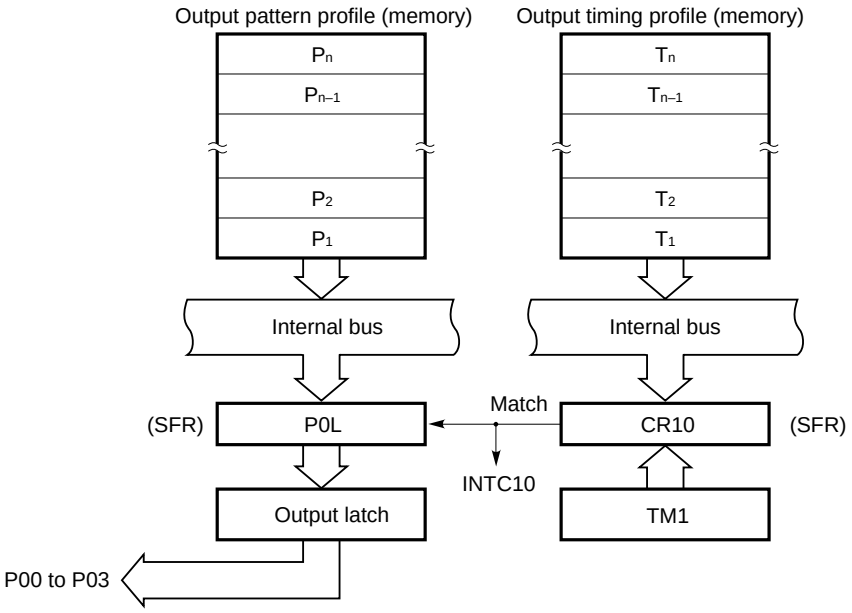
(2) Serial interface reception



Each time macro service request (INTSR) is generated, receive data is transferred from RXB to memory. When data n (last byte) has been transferred to memory (that is, once the receive data storage buffer becomes full), vectored interrupt request (INTSR) is generated.

(3) Real-time output port

INTC10 and INTC11 function as the output triggers for the real-time output ports. For these triggers, the macro service can simultaneously set the next output pattern and interval. Therefore, INTC10 and INTC11 can be used to independently control two stepping motors. They can also be applied to PWM and DC motor control.



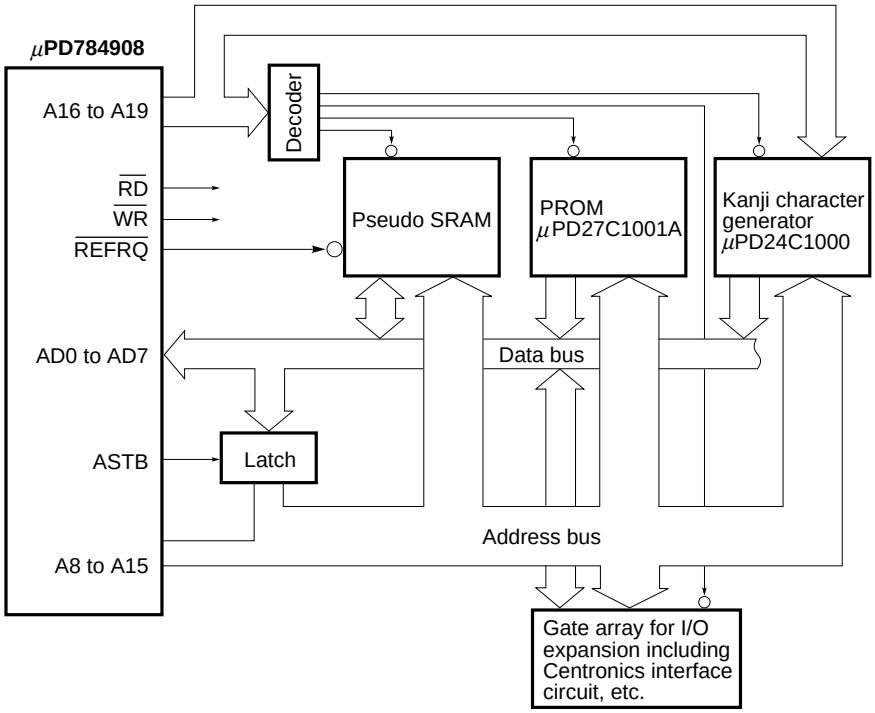
Each time macro service request (INTC10) is generated, a pattern and timing data are transferred to the buffer register (P0L) and compare register (CR10), respectively. When the contents of timer register 1 (TM1) and CR10 match, another INTC10 is generated, and the P0L contents are transferred to the output latch. When Tn (last byte) is transferred to CR10, vectored interrupt request (INTC10) is generated.

For INTC11, the same operation as that performed for INTC10 is performed.

10. LOCAL BUS INTERFACE

The local bus interface enables the connection of external memory and I/O devices (memory mapped I/O) and supports a 1-Mbyte memory space (see **Figure 10-1**).

Figure 10-1. Example of Local Bus Interface



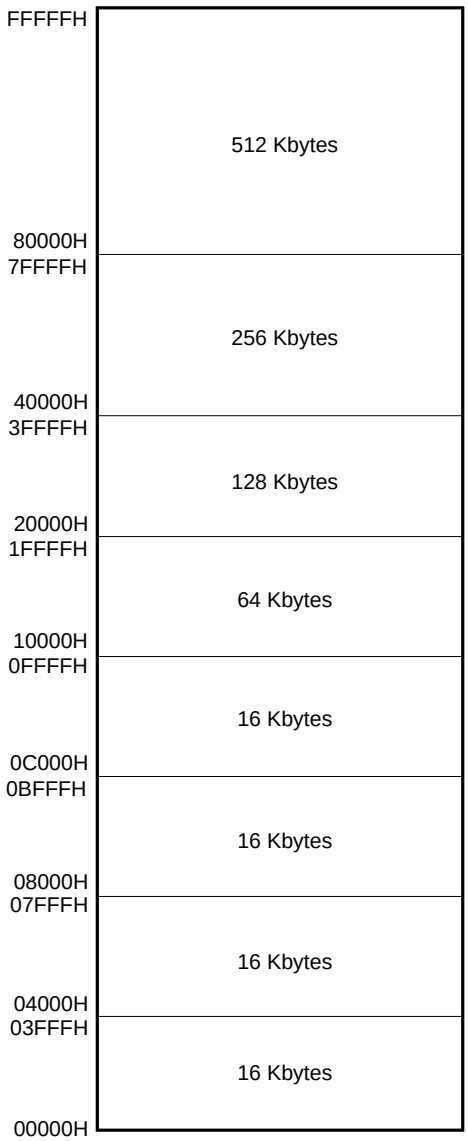
10.1 Memory Expansion

By adding external memory, program memory or data memory can be expanded, 256 bytes at a time, to approximately 1 Mbyte (seven steps).

10.2 Memory Space

The 1-Mbyte memory space is divided into eight spaces, each having a logical address. Each of these spaces can be controlled using the programmable wait and pseudo-static RAM refresh functions.

Figure 10-2. Memory Space



10.3 Programmable Wait

When the memory space is divided into eight spaces, a wait state can be separately inserted for each memory space while the $\overline{RD}$ or $\overline{WR}$ signal is active. This prevents the overall system efficiency from being degraded even when memory devices having different access times are connected.

In addition, an address wait function that extends the ASTB signal active period is provided to ensure the lapse of the address decode time. (This function is set for the entire space.)

10.4 Pseudo-Static RAM Refresh Function

Refresh is performed as follows:

- Pulse refresh
  A bus cycle is inserted where a refresh pulse is output on the $\overline{REFRQ}$ pin at regular intervals. When the memory space is divided into eight, and a specified area is being accessed, refresh pulses can also be output on the $\overline{REFRQ}$ pin as the memory is being accessed. This can prevent the refresh cycle from suspending normal memory access.
- Power-down self-refresh
  In standby mode, a low-level signal is output on the $\overline{REFRQ}$ pin to maintain the contents of pseudo-static RAM.

10.5 Bus Hold Function

A bus hold function is provided to facilitate connection to devices such as a DMA controller. When a bus hold request signal (HLDRQ) is received from an external bus master, the address bus, address/data bus, and ASTB, $\overline{RD}$, and $\overline{WR}$ pins enter the high-impedance state, the bus hold acknowledge signal (HLDAK) is made active, and the bus is released to the external bus master as soon as the current bus cycle is completed.

While the bus hold function is being used, the external wait and pseudo-static RAM refresh functions are disabled.

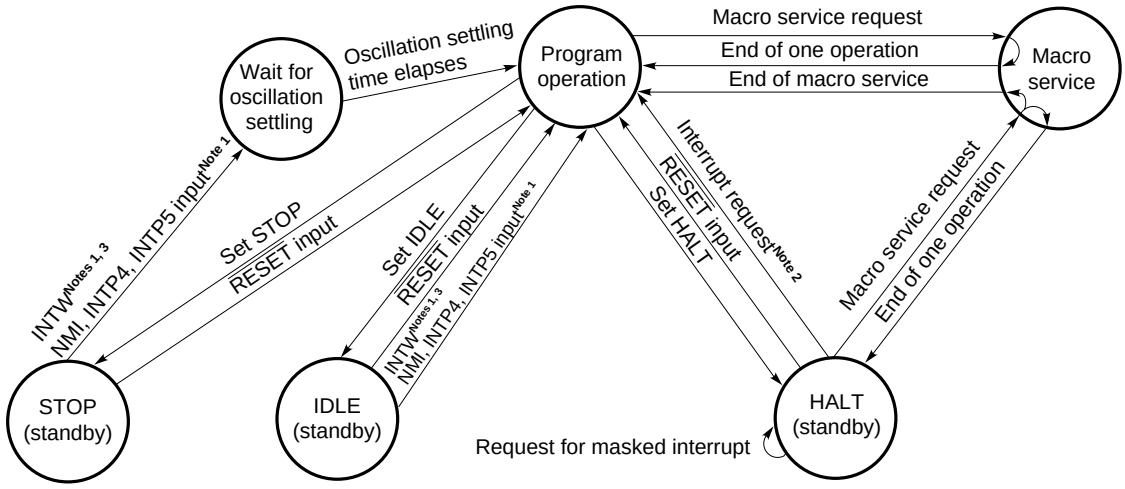
11. STANDBY FUNCTION

This function is to reduce the power consumption of the chip, and can be used in the following modes:

- HALT mode: Stops the operating clock of the CPU. This mode is used in combination with the normal operation mode for intermittent operation to reduce the average power consumption.
- IDLE mode: Stops the entire system with the oscillator continuing operation. The power consumption in this mode is close to that in the STOP mode. However, the time required to restore the normal program operation from this mode is almost the same as that from the HALT mode.
- STOP mode: Stops the oscillator and thereby stops all the internal operations of the chip. Consequently, the power consumption is minimized with only leakage current flowing.

These modes are programmable.
The macro service can be started from the HALT mode.

Figure 11-1. Standby Mode Status Transition



Notes 1. INTW, INTP4, and INTP5 are applied when not masked.
2. Only unmasked interrupt request
3. When the watch clock is operating

Remark NMI is valid only for an external input. The watchdog timer cannot be used for the release of standby (STOP, HALT, or IDLE mode).

12. RESET FUNCTION

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, the internal hardware becomes initialize status (reset status). When the $\overline{\text{RESET}}$ input makes a low-to-high transition, the following data is loaded into the program counter (PC):

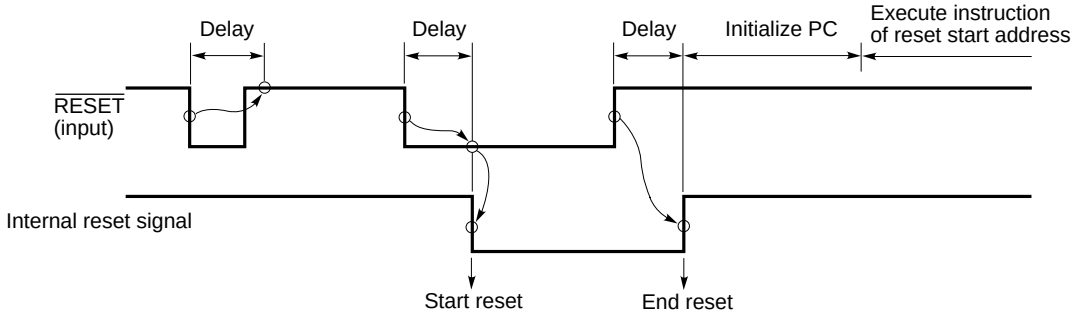
- Low-order 8 bits of the PC: Contents of address 0000H
- Intermediate 8 bits of the PC: Contents of address 0001H
- High-order 4 bits of the PC: 0

The PC contents are used as a branch destination address, and program execution starts from that address. Therefore, a reset start can be performed from an arbitrary address.

The contents of each register can be set by software, as necessary.

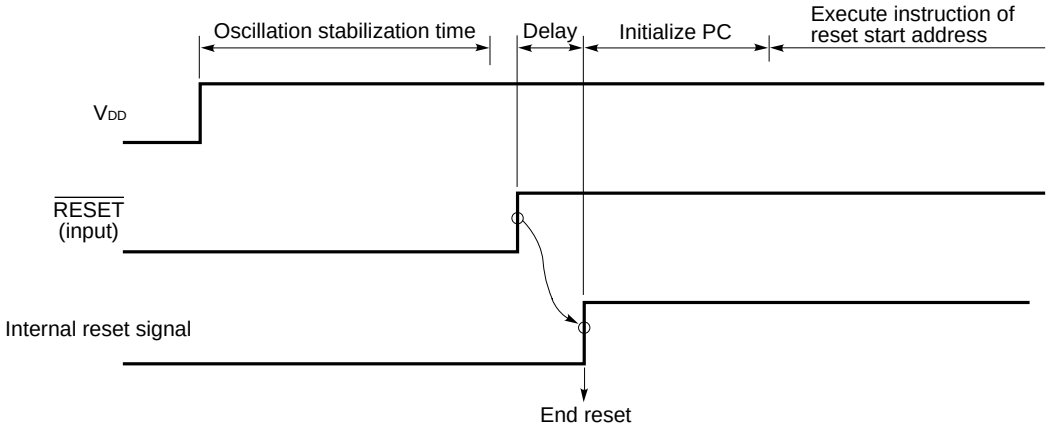
The $\overline{\text{RESET}}$ input circuit incorporates a noise eliminator to prevent malfunctions caused by noise. This noise eliminator is an analog delay sampling circuit.

Figure 12-1. Accepting Reset



For power-on reset, the $\overline{\text{RESET}}$ signal must be held active until the oscillation stabilization time (approximately 40 ms) has elapsed.

Figure 12-2. Power-On Reset



13. REGULATOR

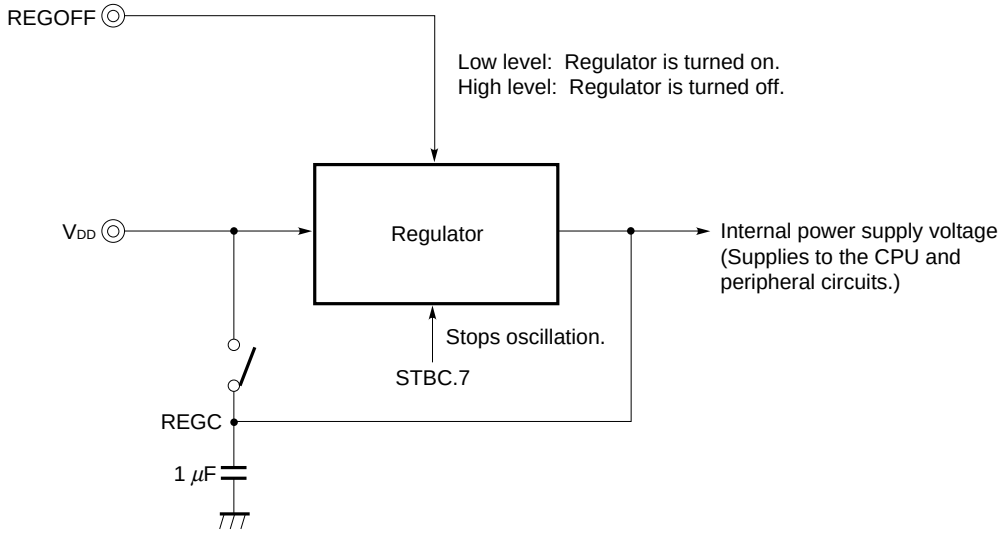
The μPD784908 incorporates a regulator (a circuit which enables low-voltage operation) to reduce the current consumption of the device. To enable or disable the operation of this regulator, specify the input level of the REGOFF pin. To disable the operation of the regulator, input a high level signal to the REGOFF pin. To enable operation, input a low level signal to the REGOFF pin.

When the regulator is turned on, the CPU enters low-power mode. It is recommended to operate this product using this regulator.

★ To stabilize the regulator output voltage, connect a capacitor (of about 1μF) to the REGC pin (stabilizing capacitor connection pin).

When the regulator is stopped, apply the same level as V_{DD} to the REGC pin. Figure 13-1 is a block diagram of the regulator's peripheral circuits.

★ **Figure 13-1. Regulator Peripheral Circuits**



- **Processing for the REGC pin**

When the regulator is operating	Connect a capacitor to stabilize the regulator.
When the regulator is stopped	Supply the power supply voltage.

14. INSTRUCTION SET

(1) 8-bit instructions (The instructions in parentheses are combinations realized by describing A as r)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 14-1. Instruction List by 8-Bit Addressing

1st operand \ 2nd operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None Note 2
A	(MOV) ADD Note 1	(MOV) (XCH) (ADD) Note 1	MOV XCH (ADD) Note 1	(MOV) Note 6 (XCH) Note 6 (ADD) Notes 1, 6	MOV (XCH) (ADD) Note 1	(MOV) (XCH) ADD Note 1	MOV XCH ADD Note 1	MOV	(MOV) (XCH) (ADD) Note 1		
r	MOV ADD Note 1	(MOV) (XCH) (ADD) Note 1	MOV XCH ADD Note 1	MOV XCH ADD Note 1	MOV XCH ADD Note 1	MOV XCH				ROR Note 3	MULU DIVUW INC DEC
saddr	MOV ADD Note 1	(MOV) Note 6 (ADD) Note 1	MOV ADD Note 1	MOV XCH ADD Note 1							INC DEC DBNZ
sfr	MOV ADD Note 1	MOV (ADD) Note 1	MOV ADD Note 1								PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD Note 1	MOV								
mem [saddrp] [%saddrg]		MOV ADD Note 1									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD) Note 1 MOVM Note 4							MOVBK Note 5		

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

2. There is no second operand, or the second operand is not an operand address.

3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.

4. XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVM.

5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.

6. When saddr is saddr2 with this combination, an instruction with a short code exists.

(2) 16-bit instructions (The instructions in parentheses are combinations realized by describing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 14-2. Instruction List by 16-Bit Addressing

1st operand \ 2nd operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None Note 2
AX	(MOVW) ADDW Note 1	(MOVW) (XCHW) (ADD) Note 1	(MOVW) (XCHW) (ADDW) Note 1	(MOVW) Note 3 (XCHW) Note 3 (ADDW) Notes 1,3	MOVW (XCHW) (ADDW) Note 1	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW Note 1	(MOVW) (XCHW) (ADDW) Note 1	MOVW XCHW ADDW Note 1	MOVW XCHW ADDW Note 1	MOVW XCHW ADDW Note 1	MOVW				SHRW SHLW	MULW Note 4 INCW DECW
saddrp	MOVW ADDW Note 1	(MOVW) Note 3 (ADDW) Note 1	MOVW ADDW Note 1	MOVW XCHW ADDW Note 1							INCW DECW
sfrp	MOVW ADDW Note 1	MOVW (ADDW) Note 1	MOVW ADDW Note 1								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. SUBW and CMPW are the same as ADDW.

2. There is no second operand, or the second operand is not an operand address.

3. When saddrp is saddrp2 with this combination, an instruction with a short code exists.

4. MULUW and DIVUX are the same as MULW.

(3) 24-bit instructions (The instructions in parentheses are combinations realized by describing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 14-3. Instruction List by 24-Bit Addressing

1st operand \ 2nd operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note There is no second operand, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 14-4. Bit Manipulation Instruction List by Addressing

2nd operand / 1st operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note There is no second operand, or the second operand is not an operand address.

(5) Call/return instructions and branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 14-5. Instruction List by Call/Return and Branch Instruction Addressing

Instruction address operand	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT EI, DI, SWRS

15. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	AV_{DD}		–0.3 to V_{DD} + 0.3	V
	AV_{SS}		–0.3 to +0.3	V
Input voltage	V_{I1}		–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}		AV_{SS} – 0.3 to AV_{REF1} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin	10	mA
		Total of P00 to P07, P30 to P37, P54 to P57, P60 to P67, and P100 to P107 pins	50	mA
		Total of P10 to P17, P40 to P47, P50 to P53, P70 to P77, P90 to P97, PWM0, PWM1, and $\overline{TX}$ pins	50	mA
Output current, high	I_{OH}	Per pin	–6	mA
		Total of P00 to P07, P30 to P37, P54 to P57, P60 to P67, and P100 to P107 pins	–30	mA
		Total of P10 to P17, P40 to P47, P50 to P53, P70 to P77, P90 to P97, PWM0, PWM1, and $\overline{TX}$ pins	–30	mA
A/D converter reference input voltage	AV_{REF1}		–0.3 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

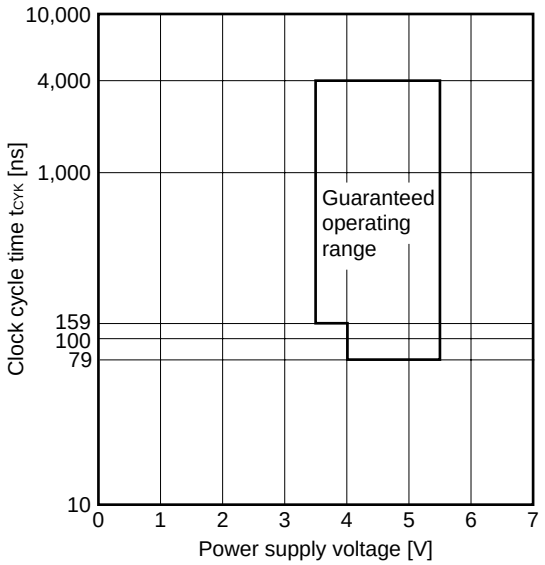
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of a alternate-function pin are the same as those of a port pin.

Operating Conditions

- Operating ambient temperature (T_A): –40°C to +85°C
- Power supply voltage and clock cycle time: see **Figure 15-1**.
- Selection of internal regulator (REGOFF pin: low-level input)

Figure 15-1. Power Supply Voltage and Clock Cycle Time



Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF
I/O capacitance	C_{IO}				15	pF

★ **Main Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Oscillator frequency	f_{XX}	Ceramic resonator or crystal resonator	2	12.58	MHz

Caution When using the clock generator, wire to avoid adverse influence from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Make the ground point of the oscillator capacitor the same potential as V_{SS1}. Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

★ **Remark** Connect a 12.582912 MHz or 6.291456 MHz oscillator to operate the internal clock timer with the main clock.

Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{XT}	Ceramic resonator or crystal resonator	32	32.768	35	kHz
Oscillation stabilization time	t_{SXT}	V_{DD} = 4.5 to 5.5 V		1.2	2	s
					10	s
Oscillation hold voltage	V_{DDXT}		3.5		5.5	V
Watch timer operating voltage	V_{DDW}		3.5		5.5	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, low**Note 5**	V_{IL1}	For pins other than **Notes 1 and 2**	–0.3		$0.3V_{DD}$	V
	V_{IL2}	For pins described in **Note 1**	–0.3		$0.2V_{DD}$	V
	V_{IL3}	V_{DD} = 4.5 to 5.5 V For pins described in **Note 2**	–0.3		+0.8	V
Input voltage, high	V_{IH1}	For pins other than **Notes 1 and 2**	$0.7V_{DD}$		V_{DD} + 0.3	V
	V_{IH2}	For pins described in **Note 1**	$0.8V_{DD}$		V_{DD} + 0.3	V
	V_{IH3}	V_{DD} = 4.5 to 5.5 V For pins described in **Note 2**	2.2		V_{DD} + 0.3	V
Output voltage, low	V_{OL1}	I_{OL} = 20 μA			0.1	V
		I_{OL} = 100 μA			0.2	V
		I_{OL} = 2 mA			0.4	V
	V_{OL2}	I_{OL} = 8 mA For pins described in **Note 4** V_{DD} = 4.5 to 5.5 V			1.0	V
Output voltage, high	V_{OH1}	I_{OH} = –20 μA	V_{DD} – 0.1			V
		I_{OH} = –100 μA	V_{DD} – 0.2			V
		I_{OH} = –2 mA	V_{DD} – 0.4			V
	V_{OH2}	V_{DD} = 4.5 to 5.5 V I_{OH} = –5 mA For pins described in **Note 3**	V_{DD} – 1.0			V

Notes 1. X1, X2, $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$, P33/SO0, P105/$\overline{\text{SCK3}}$, P106/SI3, P107/SO3, XT1, XT2

2. P40/AD0 to P47/AD7, P50/A8 to P57/A15, P60/A16 to P67/$\overline{\text{REFRQ}}$/HLDAK, P00 to P07

3. P00 to P07

4. P10 to P17, P40/AD0 to P47/AD7, P50/A8 to P57/A15

5. Other than pull-up resistors

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Input leakage current	I_{LI1}	0 V ≤ V_I ≤ V_{DD}	For pins other than X1 and XT1			±10	μA
		I_{LI2}		X1 and XT1			±20	μA
	Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
	VDD supply current[Note]	I_{DD1}	Operation mode	f_{XX} = 12.58 MHz V_{DD} = 4.0 to 5.5 V		10	20	mA
★				f_{XX} = 6.29 MHz V_{DD} = 3.5 to 5.5 V		5	10	mA
		I_{DD2}	HALT mode	f_{XX} = 12.58 MHz V_{DD} = 4.0 to 5.5 V f_{CLK} = f_{XX}/8 (STBC = B1H) Peripheral operation stops.		2.0	4.0	mA
★				f_{XX} = 6.29 MHz V_{DD} = 3.5 to 5.5 V f_{CLK} = f_{XX}/8 (STBC = 31H) Peripheral operation stops.		1.2	2.4	mA
		I_{DD3}	IDLE mode	f_{XX} = 12.58 MHz V_{DD} = 4.0 to 5.5 V		0.6	1.2	mA
★				f_{XX} = 6.29 MHz V_{DD} = 3.5 to 5.5 V		0.3	0.6	mA
	Pull-up resistor	R_L	V_I = 0 V	X1 and XT1	15		80	kΩ

Note These values are valid when the internal regulator is ON (REGOFF pin = L level). They do not include the AV_{DD} and AV_{REF1} currents.

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

(1) Read/write operation

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5 + a)T – 11	29		ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5 + a)T – 17	23		ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T – 19	21		ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T – 14	26		ns
Delay from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V	(1 + a)T – 5	74		ns
Address float time (from $\overline{RD}$↓)	t_{FRA}			0		ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V	(2.5 + a + n)T – 37		400	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V	(2 + n)T – 35		283	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V	(1.5 + n)T – 40		238	ns
Delay from ASTB↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V	0.5T – 9	31		ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}			0		ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V	0.5T – 2	38		ns
Delay from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V	0.5T – 9	31		ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5 + n)T – 25	94		ns
Delay from address↓ to $\overline{WR}$↓	t_{DAW}	V_{DD} = 5.0 V	(1 + a)T – 5	74		ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}	V_{DD} = 5.0 V	0.5T – 14	26		ns
Delay from ASTB↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V	0.5T + 15		55	ns
Delay from $\overline{WR}$↓ to data output	t_{DWOD}				15	ns
Delay from ASTB↓ to $\overline{WR}$↓	t_{DSTW}	V_{DD} = 5.0 V	0.5T – 9	31		ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	V_{DD} = 5.0 V	(1.5 + n)T – 20	99		ns
Data hold time (from $\overline{WR}$↑)	t_{HWOD}	V_{DD} = 5.0 V	0.5T – 14	26		ns
Delay from $\overline{WR}$↑ to ASTB↑	t_{DWST}	V_{DD} = 5.0 V	0.5T – 9	31		ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5 + n)T – 25	94		ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)

a: 1 during address wait, otherwise, 0

n: number of wait states ($n \geq 0$)

(2) External wait timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
$\overline{WAIT}$↓ input time from address	t_{DAWT}	V_{DD} = 5.0 V	(2 + a)T – 40		198	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	V_{DD} = 5.0 V	1.5T – 40		79	ns
$\overline{WAIT}$ hold time from ASTB↓	t_{HSTWT}	V_{DD} = 5.0 V	(0.5 + n)T + 5	124		ns
Delay from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V	(1.5 + n)T – 40		238	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWTL}	V_{DD} = 5.0 V	T – 40		39	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓	t_{HRWT}	V_{DD} = 5.0 V	nT + 5	84		ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V	(1 + n)T – 40		198	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	V_{DD} = 5.0 V	0.5T – 5		35	ns
Delay from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V	0.5T	40		ns
Delay from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V	0.5T	40		ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{DWWTL}	V_{DD} = 5.0 V	T – 40		39	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	t_{HWWT}	V_{DD} = 5.0 V	nT + 5	84		ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$↑	t_{DWWTH}	V_{DD} = 5.0 V	(1 + n)T – 40		198	ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)

a: 1 during address wait, otherwise, 0

n: number of wait states ($n \geq 0$)

(3) Bus hold timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Delay from HLDRQ↑ to float	t_{FQHC}	V_{DD} = 5.0 V	(2 + 4 + a + n)T + 50		765	ns
Delay from HLDRQ↑ to HLDAK↑	$t_{DHQHHAH}$	V_{DD} = 5.0 V	(3 + 4 + a + n)T + 30		825	ns
Delay from float to HLDAK↑	t_{DCFHA}	V_{DD} = 5.0 V	T + 30		109	ns
Delay from HLDRQ↓ to HLDAK↓	$t_{DHQLHAL}$	V_{DD} = 5.0 V	2T + 40		199	ns
Delay from HLDRQ↓ to active	t_{DHAC}	V_{DD} = 5.0 V	T – 20	59		ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)
a: 1 during address wait, otherwise, 0
n: number of wait states (n ≥ 0)

(4) Refresh timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Random read/write cycle time	t_{RC}	V_{DD} = 5.0 V	3T	238		ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	V_{DD} = 5.0 V	1.5T – 25	94		ns
Delay from ASTB↓ to $\overline{REFRQ}$	t_{DSTRFQ}	V_{DD} = 5.0 V	0.5T – 9	31		ns
Delay from $\overline{RD}$↑ to $\overline{REFRQ}$	t_{DRRFQ}	V_{DD} = 5.0 V	1.5T – 9	110		ns
Delay from $\overline{WR}$↑ to $\overline{REFRQ}$	t_{DWRFQ}	V_{DD} = 5.0 V	1.5T – 9	110		ns
Delay from $\overline{REFRQ}$↑ to ASTB	t_{DRFQST}	V_{DD} = 5.0 V	0.5T – 9	31		ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	V_{DD} = 5.0 V	1.5T – 25	94		ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)

Serial Operation (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

(1) CSI, CSI3

Parameter	Symbol	Conditions			MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK0}$, $\overline{SCK3}$)	t_{CYSK0}	Input	$f_{CLK} = f_{XX}$		$8/f_{XX}$		ns
			Except $f_{CLK} = f_{XX}$		$4/f_{CLK}$		ns
		Output	Except $f_{CLK} = f_{XX}/8$		$8/f_{XX}$		ns
			$f_{CLK} = f_{XX}/8$		$16/f_{XX}$		ns
Serial clock low-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKL0}	Input	$f_{CLK} = f_{XX}$		$4/f_{XX}$ – 40		ns
			Except $f_{CLK} = f_{XX}$		$2/f_{CLK}$ – 40		
		Output	Except $f_{CLK} = f_{XX}/8$		$4/f_{XX}$ – 40		μs
			$f_{CLK} = f_{XX}/8$		$8/f_{XX}$ – 40		
Serial clock high-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKH0}	Input	$f_{CLK} = f_{XX}$		$4/f_{XX}$ – 40		ns
			Except $f_{CLK} = f_{XX}$		$2/f_{CLK}$ – 40		
		Output	Except $f_{CLK} = f_{XX}/8$		$4/f_{XX}$ – 40		μs
			$f_{CLK} = f_{XX}/8$		$8/f_{XX}$ – 40		
SI0, SI3 setup time (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{SSSK0}				80		ns
SI0, SI3 hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSSK0}	External clock			$1/f_{CLK}$ + 80		ns
		Internal clock			80		
SO0, SO3 output delay time (from $\overline{SCK0}$, $\overline{SCK3}$↓)	t_{DSBSK1}	CMOS push-pull output		External clock	0	$1/f_{CLK}$ + 150	ns
				Internal clock	0	150	ns
	t_{DSBSK2}	Open-drain output R_L = 1 kΩ		External clock	0	$1/f_{CLK}$ + 400	ns
				Internal clock	0	400	ns
SO0, SO3 output hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSBSK}	When data is transferred			$0.5t_{CYSK0}$ – 40		ns

Remarks 1. The values in this table are those when f_{XX} = 12.58 MHz, C_L = 100 pF.

2. f_{CLK}: system clock frequency (selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/4$, and $f_{XX}/8$ by the standby control register (STBC))

★ **3.** f_{XX}: oscillation frequency (f_{XX} = 12.58 MHz or f_{XX} = 6.29 MHz)

(2) IOE1, IOE2 (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	Input	V_{DD} = 4.0 to 5.5 V	640		ns
				1,280		ns
		Output	Internal, divided by 8	T		ns
Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}	Input	V_{DD} = 4.0 to 5.5 V	280		ns
				600		ns
		Output	Internal, divided by 8	0.5T – 40		ns
Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}	Input	V_{DD} = 4.0 to 5.5 V	280		ns
				600		ns
		Output	Internal, divided by 8	0.5T – 40		ns
SI1, SI2 setup time (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}			40		ns
SI1, SI2 hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}			40		ns
SO1, SO2 output delay time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{DSOSK}			0	50	ns
SO1, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK}	When data is transferred		$0.5t_{CYSK1}$ – 40		ns

Remarks 1. The values in this table are those when C_L = 100 pF.

2. T: serial clock cycle set by software. The minimum value is $8/f_{XX}$.

(3) UART, UART2 (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASCK clock input cycle time	t_{CYASK}	V_{DD} = 4.5 to 5.5 V	160		ns
			320		ns
ASCK clock low-level width	t_{WASKL}	V_{DD} = 4.5 to 5.5 V	65		ns
			120		ns
ASCK clock high-level width	t_{WASKH}	V_{DD} = 4.5 to 5.5 V	65		ns
			120		ns

Clock Output Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
	CLKOUT cycle time	t_{CYCL}	nT	79	32,000	ns
	CLKOUT low-level width	t_{CLL}	V_{DD} = 4.0 to 5.5 V, 0.5T – 10	30		ns
			0.5T – 20	20		ns
	CLKOUT high-levell width	t_{CLH}	V_{DD} = 4.0 to 5.5 V, 0.5T – 10	30		ns
			0.5T – 20	20		ns
	CLKOUT rising time	t_{CLR}	V_{DD} = 4.0 to 5.5 V		10	ns
★			V_{DD} = 3.5 to 4.0 V	0.3	20	ns
	CLKOUT falling time	t_{CLF}	V_{DD} = 4.0 to 5.5 V		10	ns
★			V_{DD} = 3.5 to 4.0 V	0.3	20	ns

Remark n: Dividing ratio set by software in the CPU (n = 1, 2, 4, 8, and 16)
T: t_{CYK} (system clock cycle time)

Other Operations (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 low-level width	t_{WIT0L}		$4t_{CYSMP}$		ns
INTP0 high-level width	t_{WIT0H}		$4t_{CYSMP}$		ns
INTP1 to INTP3 and CI low-level width	t_{WIT1L}		$4t_{CYCPU}$		ns
INTP1 to INTP3 and CI high-level width	t_{WIT1H}		$4t_{CYCPU}$		ns
INTP4 and INTP5 low-level width	t_{WIT2L}		10		μs
INTP4 and INTP5 high-level width	t_{WIT2H}		10		μs
$\overline{\text{RESET}}$ low-level width**Note**	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

Note When the power is ON, secure the oscillation stabilization wait time with the $\overline{\text{RESET}}$ low-level width.

Remark t_{CYSMP}: sampling clock set by software
t_{CYCPU}: CPU operation clock set by software in the CPU

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = 3.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8			bit
Total error**Note**		IEAD = 00H				0.6	%
			FR = 1			1.5	%
		IEAD = 01H	V_{DD} = 4.5 to 5.5 V		1	2.2	%
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	FR = 1 120/f_{CLK}		9.5		480	μs
		FR = 0 240/f_{CLK}		19.1		960	μs
Sampling time	t_{SAMP}	FR = 1 18/f_{CLK}		1.4		72	μs
		FR = 0 36/f_{CLK}		2.9		144	μs
Analog input impedance	R_{AN}				1,000		MΩ
AV_{REF1} impedance	R_{REF1}			3	10		kΩ
AV_{DD} power supply current	AI_{DD1}	CS = 1			2.0	5.0	mA
	AI_{DD2}	CS = 0, STOP mode			1.0	20	μA

Note Quantization error is not included. This parameter is indicated as the ratio to the full-scale value.

Caution To execute the conversion by the A/D converter set port 7, multiplexed with the A/D input lines, to output mode to prevent data from being inverted.

Remark f_{CLK}: system clock frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

IEBus Controller Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus standard frequency**Note 1**	f_S	Transfer speed: mode 1	6.20	6.29	6.39	MHz
Driver delay time (from $\overline{TX}$ output to bus line)**Note 2**	t_{DTX}	C_L = 50 pF**Note 3**			1.5	μs
Receiver delay time (from bus line to $\overline{RX}$ input)**Note 2**	t_{DRX}				0.7	μs
Transmission delay on bus**Note 2**	t_{DBUS}				0.85	μs

Notes 1. The value conforms to the IEBus standard. The IEBus controller is operable within the range of the oscillator frequency of oscillator characteristics.

2. IEBus system clock: The value is measured when f_X = 6.29 MHz.

3. C is the load capacitance of $\overline{TX}$ output line.

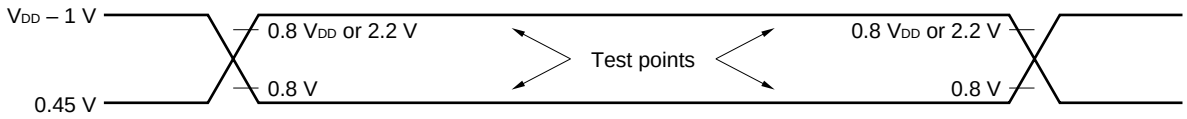
Data Retention Characteristics (T_A = –40 to +85°C)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Data retention voltage	V_{DDDR}	STOP mode		2.5		5.5	V
	Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V, AV_{REF} = 0 V **Note 1**		2	10	μA
★				V_{DDDR} = 3.5 to 5.5 V, AV_{REF} = 0 V **Note 1**		10	50	μA
	V_{DD} rising time	t_{RVD}			200			μs
	V_{DD} falling time	t_{FVD}			200			μs
	V_{DD} hold time (from STOP mode setting)	t_{HVD}			0		0.6	ms
	STOP clear signal input time	t_{DREL}			0			ms
	Oscillation settling time	t_{WAIT}	Crystal resonator		30			ms
			Ceramic resonator		5		0.1V_{DDDR}	ms
	Input low voltage	V_{IL}	Specific pins **Note 2**		0		V_{DDDR}	V
	Input high voltage	V_{IH}			0.9V_{DDDR}			V

Notes 1. Valid when input voltages to the pins described in Note 2 satisfy V_{IL} or V_{IH} in the above table.

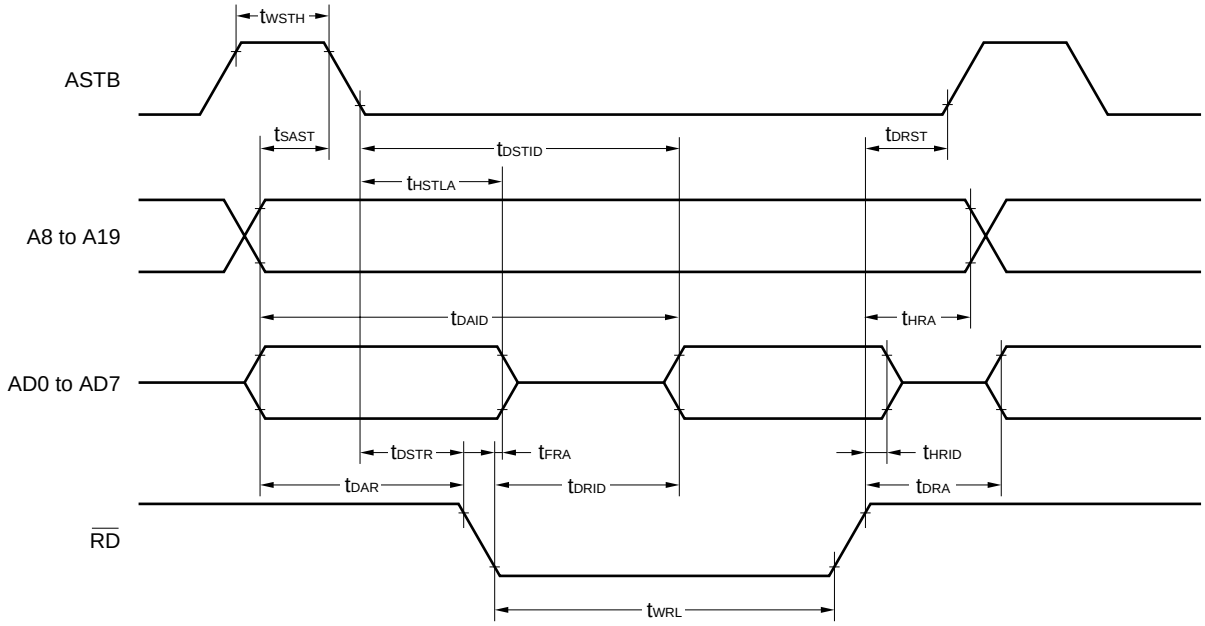
2. $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$, P33/SO0, P105/$\overline{\text{SCK3}}$, P106/SI3, and P107/SO3 pins

AC Timing Test Points

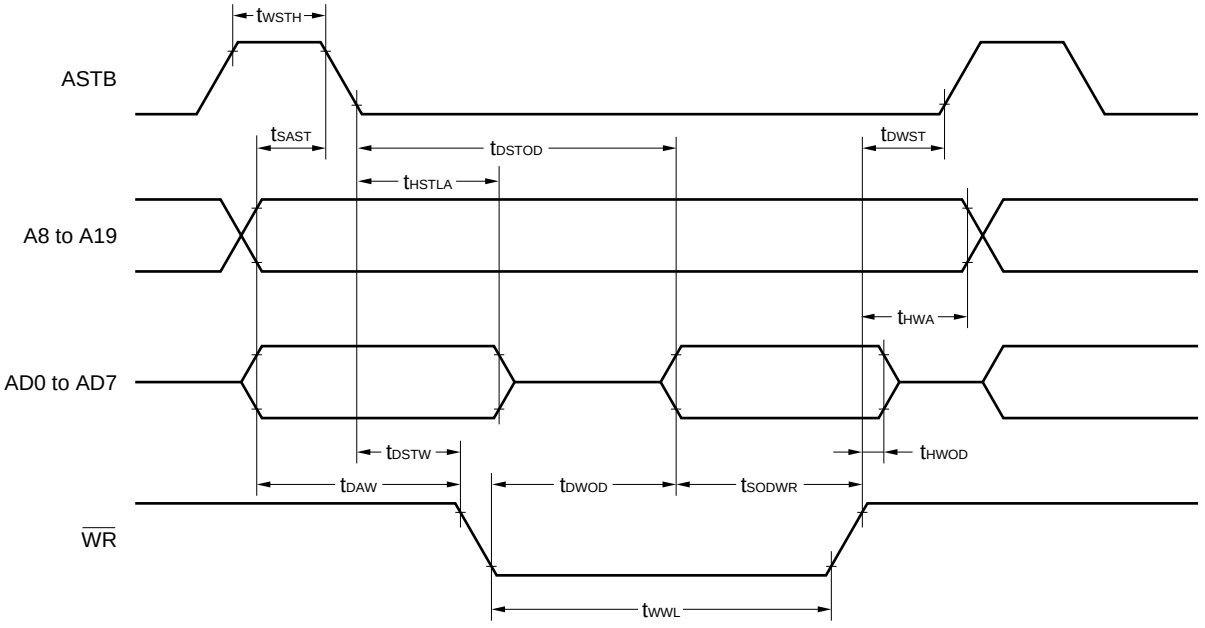


Timing Waveform

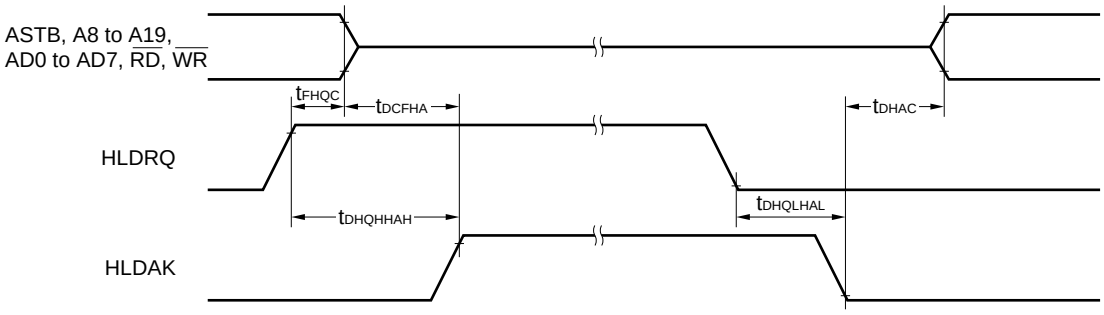
(1) Read operation



(2) Write operation

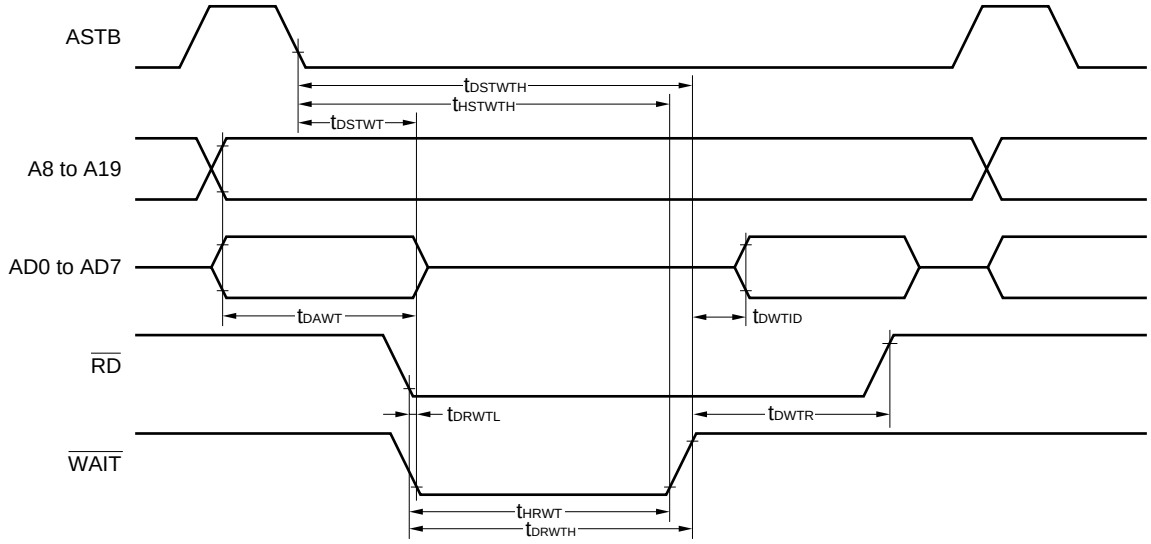


Hold Timing

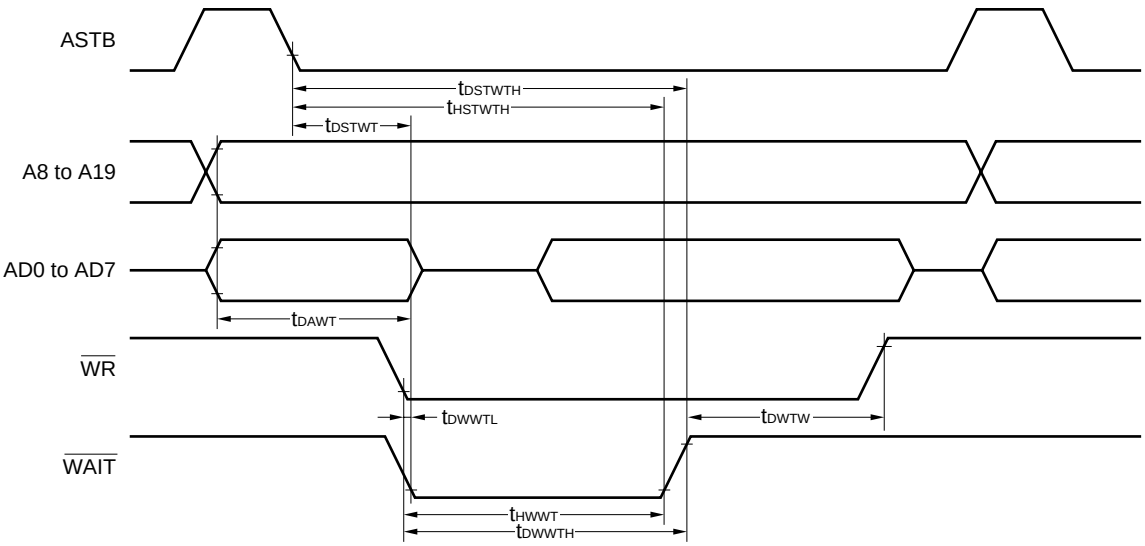


External Wait Signal Input Timing

(1) Read operation

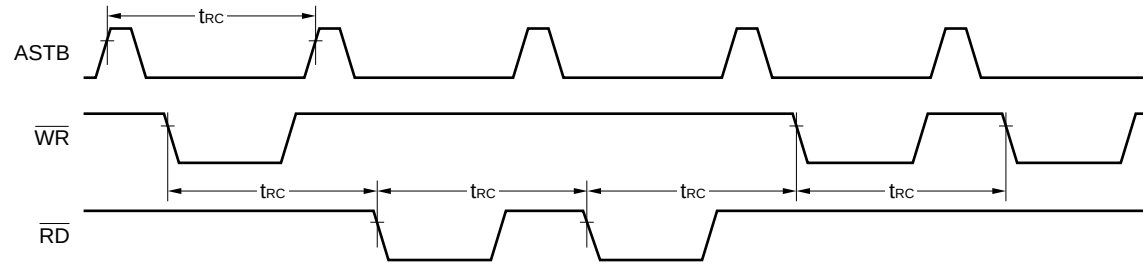


(2) Write operation

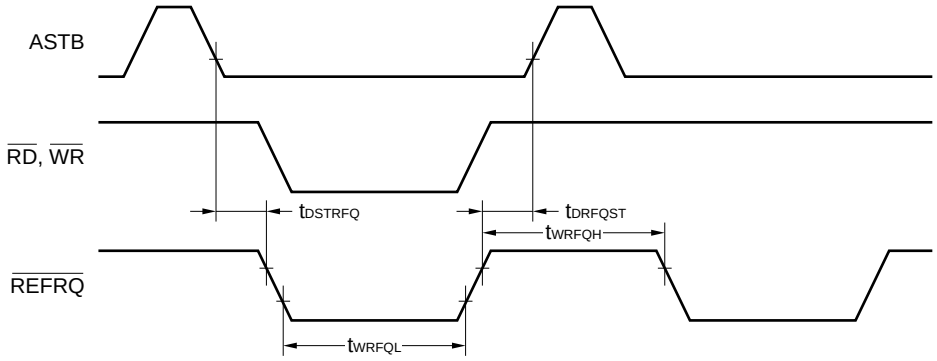


Refresh Timing Waveform

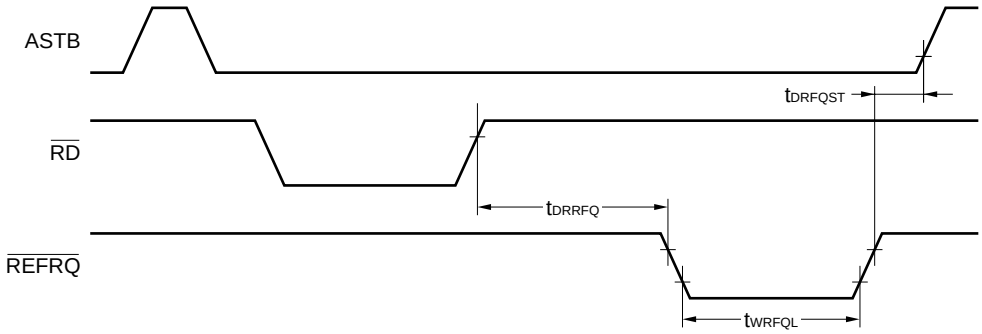
(1) Random read/write cycle



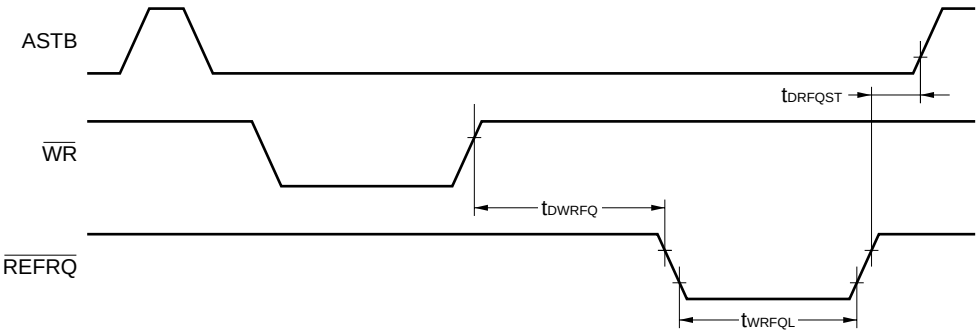
(2) When refresh memory is accessed for a read and write at the same time



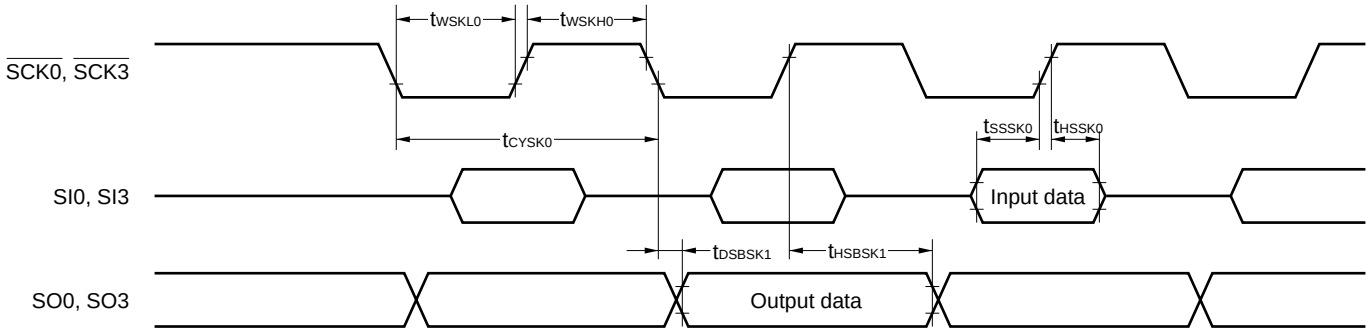
(3) Refresh after a read



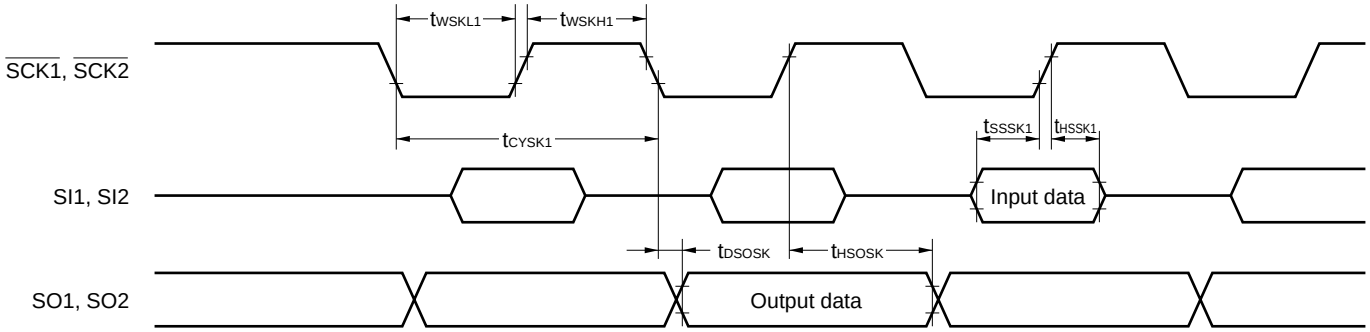
(4) Refresh after a write



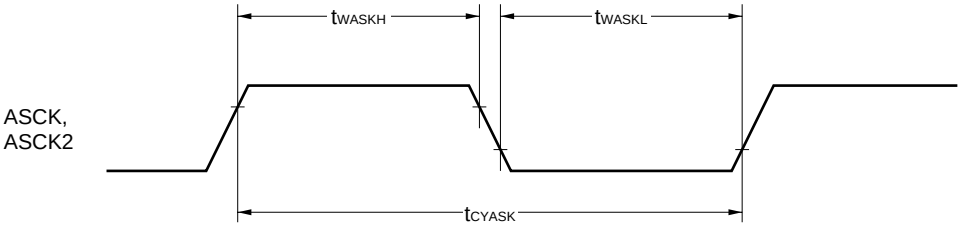
Serial Operation (CSI, CSI3)



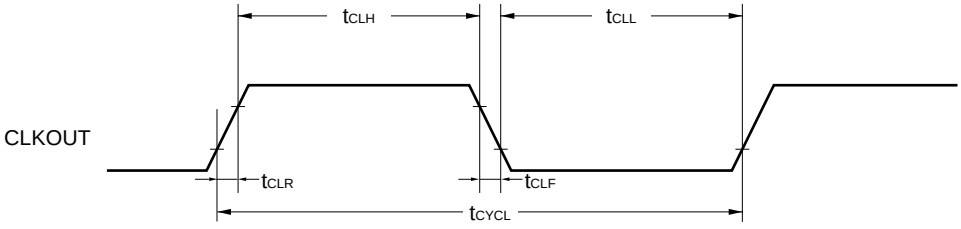
Serial Operation (IOE1, IOE2)



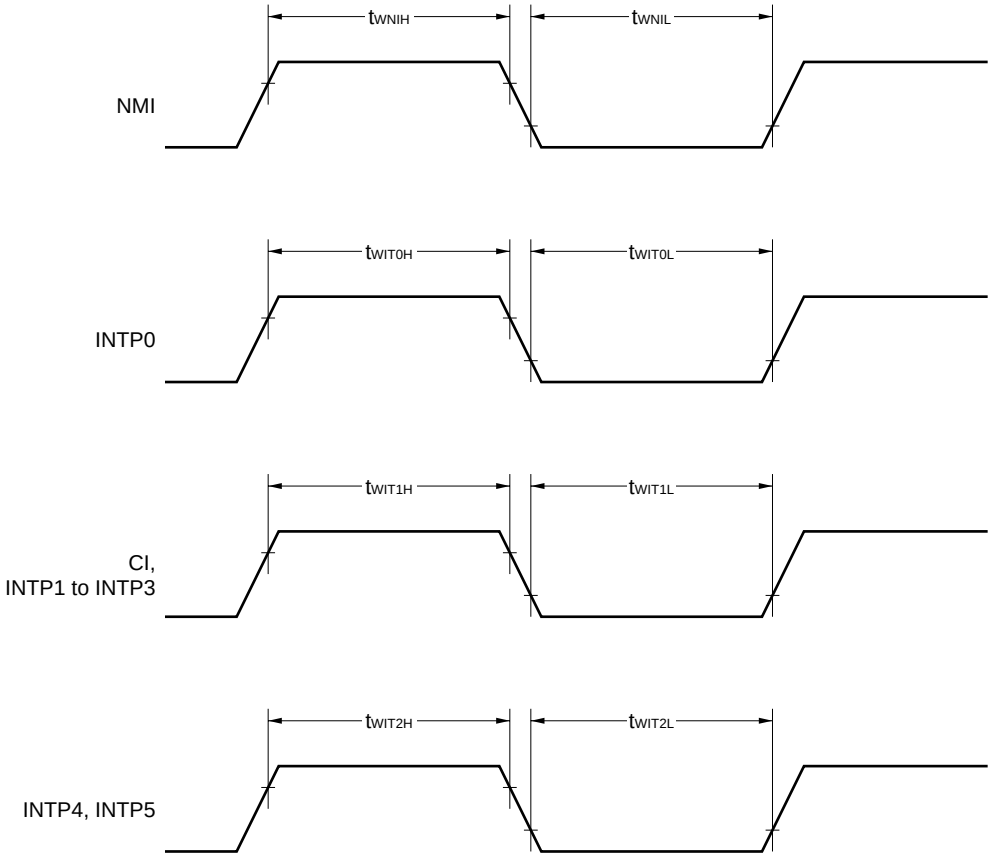
Serial Operation (UART, UART2)



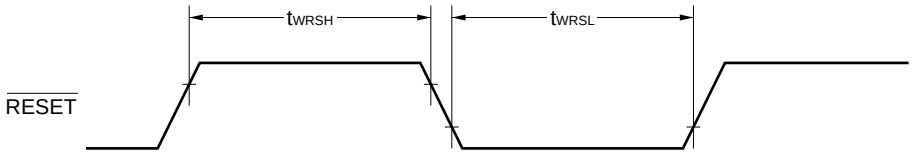
Clock Output Timing



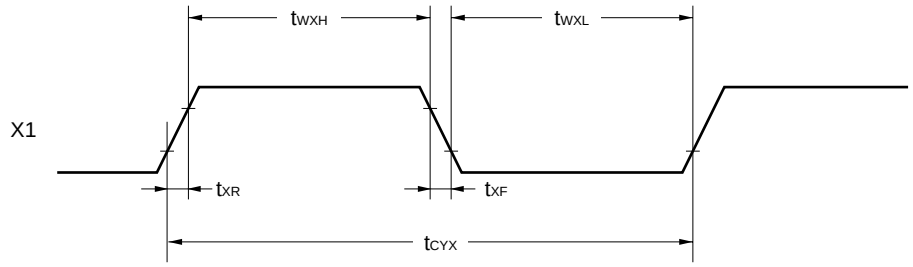
Interrupt Request Input Timing



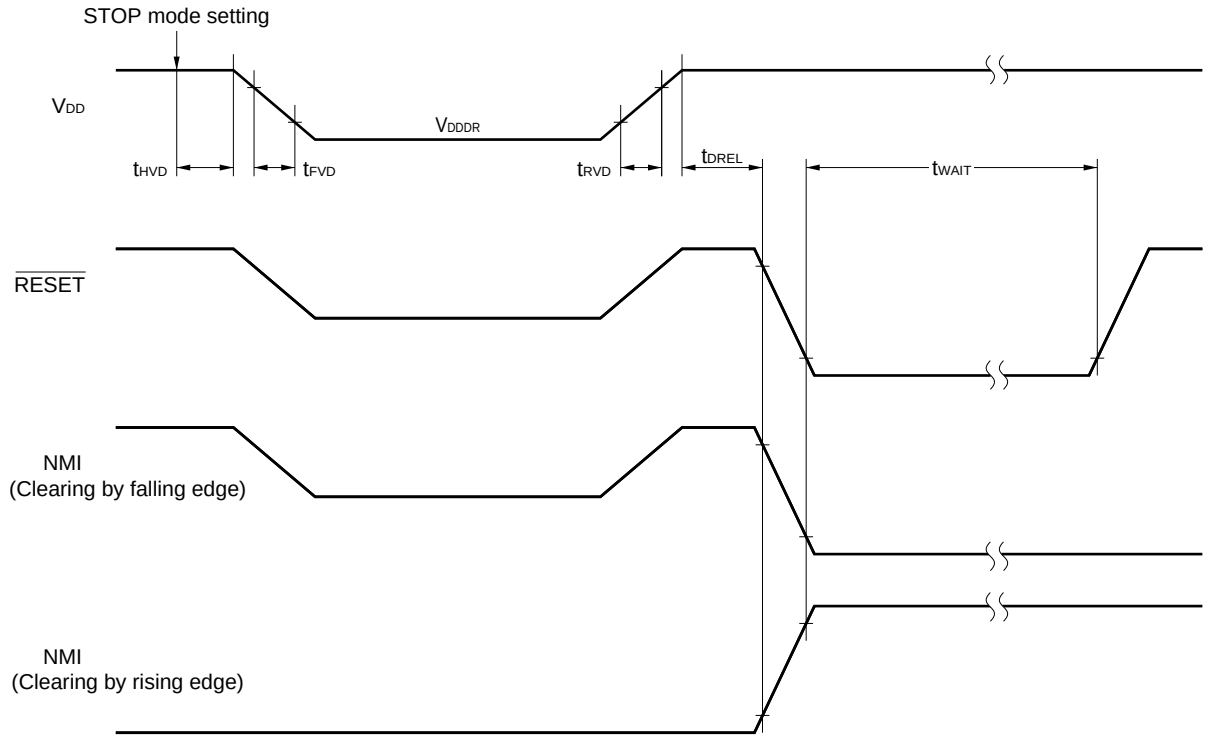
Reset Input Timing



External Clock Timing

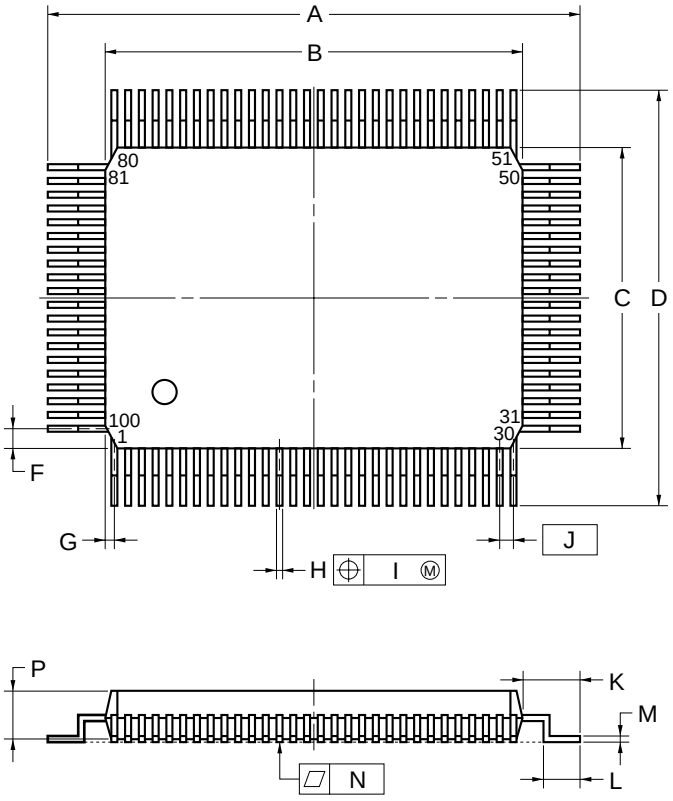


Data Retention Characteristics

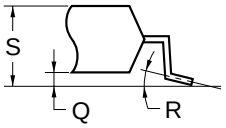


16. PACKAGE DRAWING

100 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

17. RECOMMENDED SOLDERING CONDITIONS

The μPD784908 should be soldered under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 17-1. Soldering Conditions for Surface Mount Type

μPD784907GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD784908GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C Time: 30 seconds max. (210°C or higher) Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C Time: 40 seconds or max. (200°C or higher) Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max. Time: 10 seconds max. Count : 1 Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating method	Pin temperature: 300°C Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784908.
Also refer to **(5) Cautions on using development tools**.

(1) Language processing software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784908	Device file for μPD784908 Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) PROM write tools

PG-1500	PROM programmer
PA-78P4908GF	Programmer adapter, connects to PG-1500
PG-1500 controller	Control program for PG-1500

(3) Debugging tools

- **When using the in-circuit emulator IE-78K4-NS**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
★ IE-70000-98-IF-C	Interface adapter when a PC-9800 Series computer (except notebook type) is used as the host machine (C bus supported)
★ IE-70000-CD-IF-A	PC card and interface cable when a notebook type is used as the host machine (PCMCIA socket supported)
★ IE-70000-PC-IF-C	Interface adapter when an IBM PC/AT™ or compatible is used as the host machine (ISA bus supported)
★ IE-70000-PCI-IF	Adapter when a PC that incorporates a PCI bus is used as the host machine
IE-784908-NS-EM1	Emulation board to emulate μPD784908 Subseries
NP-100GF**Note**	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be mounted on target system board made for 100-pin plastic QFP (GF-3BA type). Used in LCC mode.
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784908	Device file for μPD784908 Subseries

Note Under development

- **When using the in-circuit emulator IE-784000-R**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-C	Interface adapter when a PC-9800 Series computer (except notebook type) is used as the host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when an IBM PC/AT or compatible is used as the host machine (ISA bus supported)
★ IE-70000-PCI-IF	Adapter when a PC that incorporates a PCI bus is used as the host machine
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
IE-784908-NS-EM1 IE-784908-R-EM1	Emulation board to emulate μPD784908 Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX2	Conversion board for emulation probes required to use the IE-784908-NS-EM1 on the IE-784000-R. The board is not needed when the conventional product IE-784908-R-EM1 is used.
EP-78064-GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be mounted on target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784908	Device file for μPD784908 Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on using development tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784908.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784908.
- The NP-100GF is a product made by Naito Densei Machidaseisakusho Co., Ltd. (+81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- The host machines and OSs suitable for each software are as follows.

Host Machine [OS] / Software	PC	EWS
	PC-9800 Series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	√**Note**	√
CC78K4	√**Note**	√
PG-1500 controller	√**Note**	—
ID78K4-NS	√	—
ID78K4	√	√
SM78K4	√	—
RX78K/IV	√**Note**	√
MX78K4	√**Note**	√

Note DOS-based software

APPENDIX B RELATED DOCUMENTS

Documents related to devices

Document Name	Document No.	
	Japanese	English
μPD784907, 784908 Data Sheet	U11680J	This manual
μPD78P4908 Data Sheet	U11681J	U11681E
μPD784908 Subseries User's Manual Hardware	U11787J	U11787E
μPD784908 Subseries Special Function Register Table	U11589J	—
78K/IV Series User's Manual Instructions	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	—
78K/IV Series Instruction Set	U10595J	—
78K/IV Series Application Note Software Basics	U10095J	U10095E

Documents related to development tools (User's Manual)

	Document Name		Document No.	
			Japanese	English
	RA78K4 Assembler Package	Language	U11162J	U11162E
		Operation	U11334J	U11334E
	RA78K4 Structured Assembler Preprocessor		U11743J	U11743E
	CC78K4 C Compiler	Language	U11571J	U11571E
		Operation	U11572J	U11572E
	PG-1500 PROM Programmer		U11940J	U11940E
	PG-1500 Controller PC-9800 Series (MS-DOS™) Based		EEU-704	EEU-1291
	PG-1500 Controller IBM PC Series (PC DOS™) Based		EEU-5008	U10540E
★	IE-78K4-NS		U13356J	U13356E
	IE-784000-R		U12903J	U12903E
	IE-784908-R-EM1		U11876J	—
★	IE-784908-NS-EM1		U13743J	Under preparation
	EP-78064		EEU-934	EEU-1469
	SM78K4 System Simulator Windows Based	Reference	U10093J	U10093E
	SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
	ID78K4-NS Integrated Debugger PC Based	Reference	U12796J	U12796E
	ID78K4 Integrated Debugger Windows Based	Reference	U10440J	U10440E
	ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Based	Reference	U11960J	U11960E

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

Documents related to embedded software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamental	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	—
78K/IV Series OS MX78K4	Fundamental	U11779J	—

Other documents

Document Name	Document No.	
	Japanese	English
★ NEC IC PACKAGE MANUAL (CD-ROM)	—	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Devices	—	MEI-1202
Guide to Microcontroller-Related Products by Third Parties	U11416J	—

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Tel: 01908-691-133
Fax: 01908-670-290

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Fax: 08-63 80 388

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Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

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Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

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