NEC

MOS INTEGRATED CIRCUIT

μPD78C14(A)

8-BIT SINGLE-CHIP MICROCONTROLLER (WITH A/D CONVERTER)

The μPD78C14(A) is a single-chip, CMOS 8-bit microcontroller in which a 16-bit ALU, a ROM, a RAM, an A/D converter, a multifunction timer/event counter, and a serial interface are all integrated. Moreover, a 48-Kbyte external expansion memory (ROM/RAM) can be connected.

Since the μPD78C14(A) uses the CMOS construction, its operations are performed with low power consumption. By using the standby function, functions such as data retention are performed with lower power consumption.

For details on functions, refer to the User's Manual listed below. Please read it before starting design work.

87AD series μPD78C18 User's Manual: IEU-1314

FEATURES

- ○ High reliability as compared with μPD78C14
- ○ 159 instructions: 87AD instruction set
  Multiply and divide instructions, 16-bit arithmetic operation instructions
- ○ Instruction cycle: 0.8 μs at 15 MHz
- ○ Internal ROM: 16384 W x 8
- ○ Internal RAM: 256 W x 8
- ○ Direct addressing to an external memory (ROM/RAM) up to 64 Kbytes
- ○ Highly accurate 8-bit A/D converter: Eight analog inputs
- ○ General-purpose serial interface: Asynchronous, synchronous, and I/O interface modes
- ○ Multifunction 16-bit timer/event counter
- ○ Two 8-bit timers
- ○ I/O lines: 44
- ○ Interrupt functions: Three external, eight internal
  - Non-maskable interrupt: 1
  - Maskable interrupts: 10
- ○ Zero-cross detection function (two inputs)
- ○ Standby functions: HALT mode, Hardware/software STOP mode

ORDERING INFORMATION

Part number	Package	Quality grade
μPD78C14G(A)-xxx-36	64-pin plastic QUIP	Special
μPD78C14GF(A)-xxx-3BE	64-pin plastic QFP (14 x 20 mm)	Special
μPD78C14L(A)-xxx	68-pin plastic QFJ (950 x 950 mil)	Special

Remark xxx is a ROM code suffix.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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Date Published May 1995 P
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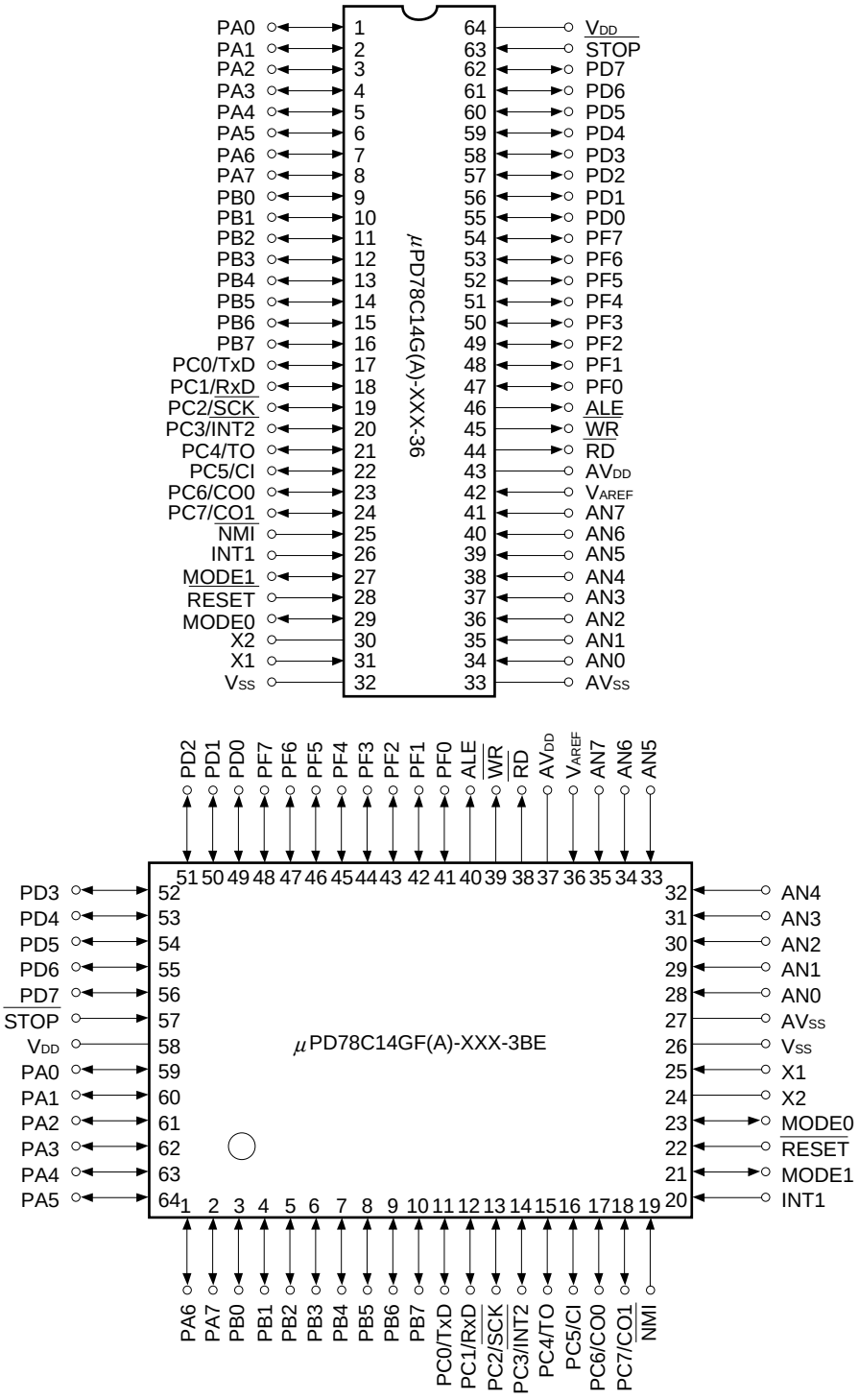
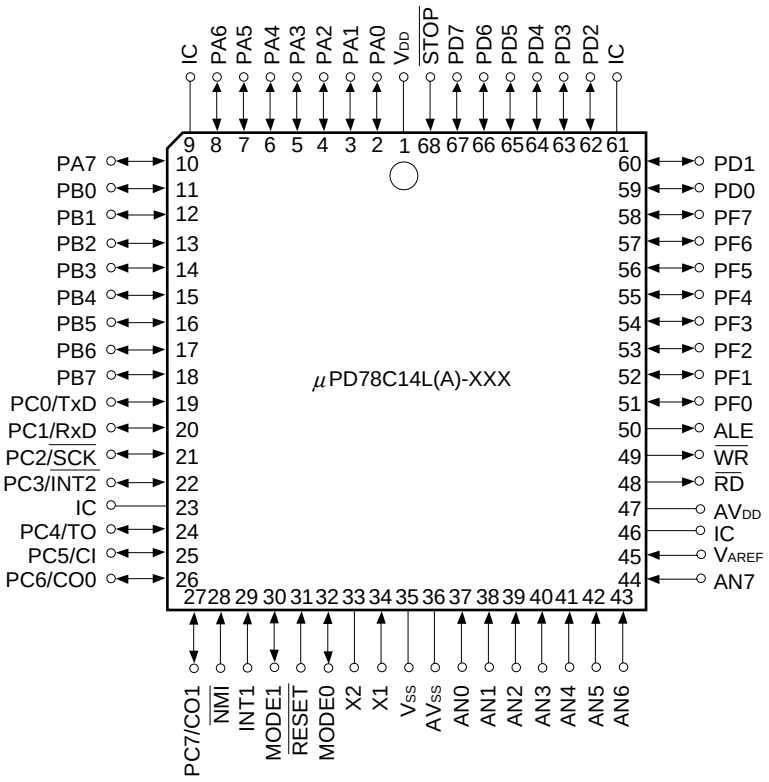
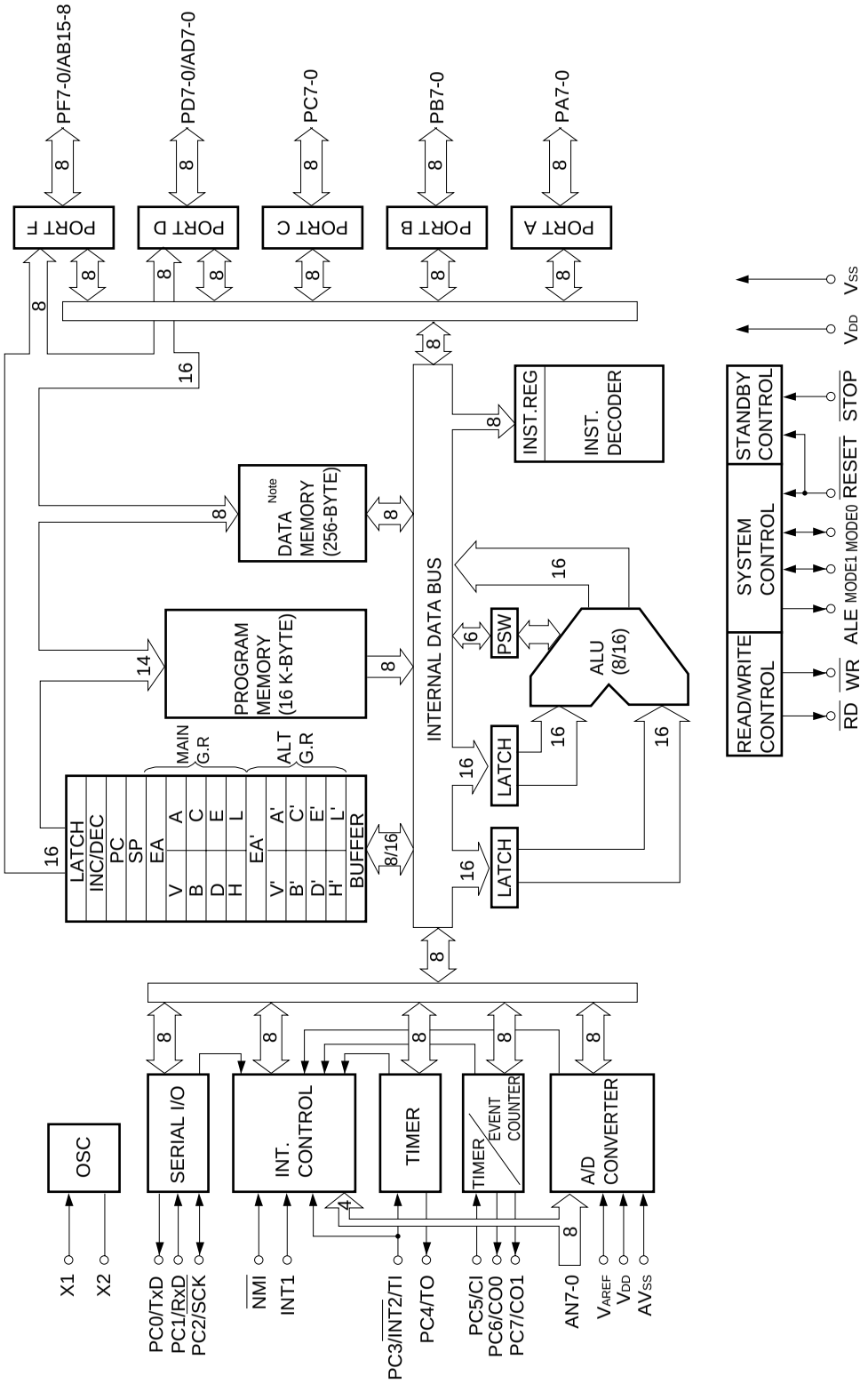
The mark ✱ shows revised points.

Pin Configuration (Top View)




IC
PA6
PA5
PA4
PA3
PA2
PA1
PA0
VDD
STOP
PD7
PD6
PD5
PD4
PD3
PD2
IC
9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
PA7 10
PB0 11
PB1 12
PB2 13
PB3 14
PB4 15
PB5 16
PB6 17
PB7 18
PC0/TxD 19
PC1/RxD 20
PC2/SCK 21
PC3/INT2 22
IC 23
PC4/TO 24
PC5/CI 25
PC6/CO0 26
60 PD1
59 PD0
58 PF7
57 PF6
56 PF5
55 PF4
54 PF3
53 PF2
52 PF1
51 PF0
50 ALE
49 WR
48 RD
47 AVDD
46 IC
45 VAREF
44 AN7
μPD78C14L(A)-XXX
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
PC7/CO1
NMI
INT1
MODE1
RESET
MODE0
X2
X1
VSS
AVSS
AN0
AN1
AN2
AN3
AN4
AN5
AN6

Block Diagram



Note DATA MEMORY can only be used when RAE bit of MM register is set to 1.
External memory is necessary when 0 is set.

CONTENTS

1. DIFFERENCES BETWEEN μPD78C14(A) AND μPD78C14

Part number / Item	μPD78C14(A)	μPD78C14
Quality grade	Special	Standard
Electrical specifications	Input leakage current (AN7-0; ±1 μA (MAX.)	Input leakage current AN7-0; ±10 μA (MAX.)
Package	• 64-pin plastic QUIP • 64-pin plastic QFP (14 x 20 mm, thickness: 2.05 mm) • 68-pin plastic QFJ	• 64-pin plastic shrink DIP • 64-pin plastic QUIP • 64-pin plastic QUIP (straight) • 64-pin plastic QFP (14 x 20 mm, thickness: 2.05 mm) • 64-pin plastic QFP (14 x 20 mm, thickness: 2.70 mm) • 68-pin plastic QFJ

2. PIN FUNCTIONS

2.1 Pin Function List

Pin	Input/Output	Function	
PA7-PA0 (Port A)	Input/Output	These 8 pins constitute an 8-bit I/O port and input/output can be specified in bit units.	
PB7-PB0 (Port B)	Input/Output	These 8 pins constitute an 8-bit I/O port and input/output can be specified in bit units.	
PC0/TxD	Input/Output, Output	Port C These 8 pins constitute an 8-bit I/O port and input/output can be specified in bit units.	Transmit Data This pin outputs serial data.
PC1/RxD	Input/Output, Input		Receive Data This pin inputs serial data.
PC2/$\overline{\text{SCK}}$	Input/Output, Input/Output		Serial Clock This pin inputs/outputs serial clock. It becomes an output pin when an internal clock is used or an input pin when an external clock is used.
PC3/$\overline{\text{INT2}}$/TI	Input/Output, Input, Input		Interrupt Request/Timer Input This pin inputs edge triggering (falling edge) maskable interrupt or external clock for timer. This pin is also shared with zero-cross detection pin for AC input.
PC4/TO	Input/Output, Output		Timer Output This pin outputs square waves in which one cycle of the internal clock forms a half cycle, indicating the timer's counting time.
PC5/CI	Input/Output, Input		Counter Input This pin inputs external pulse for timer/event counter.
PC6/CO0 PC7/CO1	Input/Output, Output		Counter Output 0,1 This pin outputs programmable square wave by timer/event counter.
PD7-PD0/ AD7-AD0	Input/Output, Input/Output	Port D These 8 pins constitute an 8-bit I/O port and input/output can be specified in byte units.	Address/Data Bus These pins function as multiplexed address/data bus when using an external memory.
PF7-PF0/ AB15-AB8	Input/Output, Output	Port F These 8 pins constitute an 8-bit I/O port and input/output can be specified in bit units.	Address Bus These pins function as address bus when using an external memory.
$\overline{\text{WR}}$ (Write Strobe)	Output	This is a strobe signal output to write data in external memory. This signal becomes high level except during the data write machine cycle for external memory. This signal becomes output high impedance when the $\overline{\text{RESET}}$ signal is low or in the hardware STOP mode.	

(Continued)

Pin	Input/Output	Function
$\overline{RD}$ (Read Strobe)	Output	This is a strobe signal output to read data from external memory. This signal becomes high level except during the data read machine cycle for external memory. This signal becomes output high impedance when the $\overline{RESET}$ signal is low or in the hardware STOP mode.
ALE (Address Latch Enable)	Output	This is a strobe signal to externally latch the low-order address information output to pins PD7-PD0 to access the external memory. This signal becomes output high impedance when the $\overline{RESET}$ signal is low or in the hardware STOP mode.
MODE0 MODE1 (Mode)	Input/Output	Set the MODE0 pin to 0 (low level) and MODE1 pin to 1 (high level)[Note]. When both pins MODE0 and MODE1 are set to 1[Note], these pins synchronize to the ALE and a control signal is output.
$\overline{NMI}$ (Non-Maskable Interrupt)	Input	This pin inputs the edge triggering (falling edge) nonmaskable interrupt.
INT1 (Interrupt Request)	Input	This pin inputs edge triggering (rising edge) maskable interrupt. This pin is also shared with zero-cross detection pin for AC input.
AN7-AN0 (Analog Input)	Input	These eight pins input analog signals for the A/D converter. Pins AN7-AN4 can be used as edge detection (falling edge) input.
V_{AREF} (Reference Voltage)	Input	This pin inputs the reference voltage for the A/D converter and controls the operation for the A/D converter.
AV_{DD} (Analog V_{DD})		Power supply pin for the A/D converter
AV_{SS} (Analog V_{SS})		Ground pin for the A/D converter
X1, X2 (Crystal)		These are crystal connecting pins for the system clock oscillation. When a clock is externally supplied, input it through pin X1. Input the clock to X1 and its reverse phase to X2.
$\overline{RESET}$ (Reset)	Input	This pin inputs the active-low reset input signal.
$\overline{STOP}$ (Stop)	Input	This pin inputs control signal of the hardware STOP mode. When the low level of this signal is input, the oscillator stops to operate.
V_{DD}		Positive power supply pin
V_{SS}		Ground pin

Note Pull-up with the following external resistor:

$4\ (k\Omega) \leq R \leq 0.4\ t_{CYC}\ (k\Omega)$ t_{CYC} (unit: ns)

Example $4\ (k\Omega) \leq R \leq 26\ (k\Omega)$: $t_{CYC} = 66$ (ns) at 15 MHz

$4\ (k\Omega) \leq R \leq 33\ (k\Omega)$: $t_{CYC} = 83$ (ns) at 12 MHz

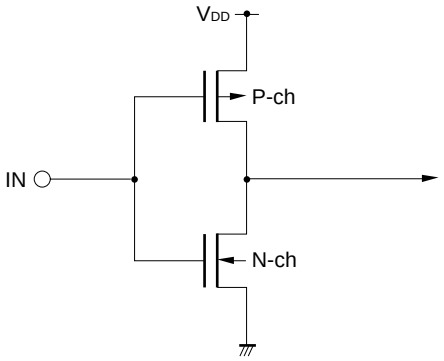
2.2 Pin Input/Output Circuits

Schematic input/output circuits of the pins are shown in Table 2-1 and figures from (1) to (11).

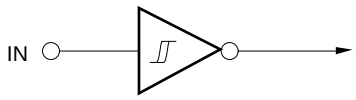
Table 2-1. Name of Type No.

Pin	Type No.	Pin	Type No.
PA0-7	5	$\overline{\text{RESET}}$	2
PB0-7	5	$\overline{\text{RD}}$	4
PC0-1	5	$\overline{\text{WR}}$	4
PC2/$\overline{\text{SCK}}$	8	ALE	4
PC3/$\overline{\text{INT2}}$	10	$\overline{\text{STOP}}$	2
PC4-7	5	MODE0	11
PD0-7	5	MODE1	11
PF0-7	5	AN0-3	7
$\overline{\text{NMI}}$	2	AN4-7	12
INT1	9	V_{AREF}	13

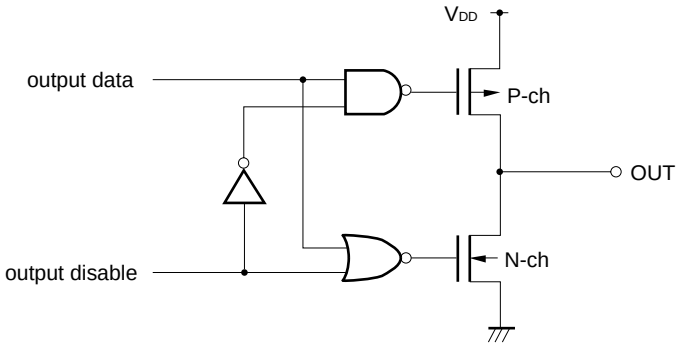
(1) Type 1



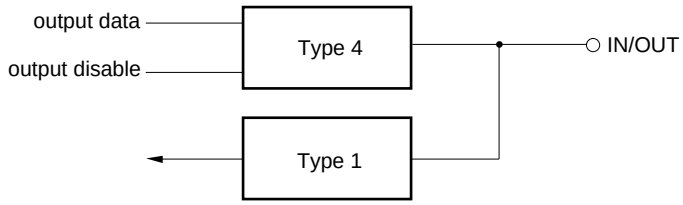
(2) Type 2



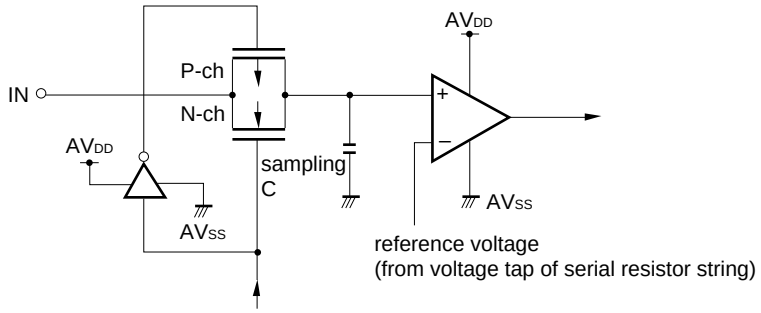
(3) Type 4



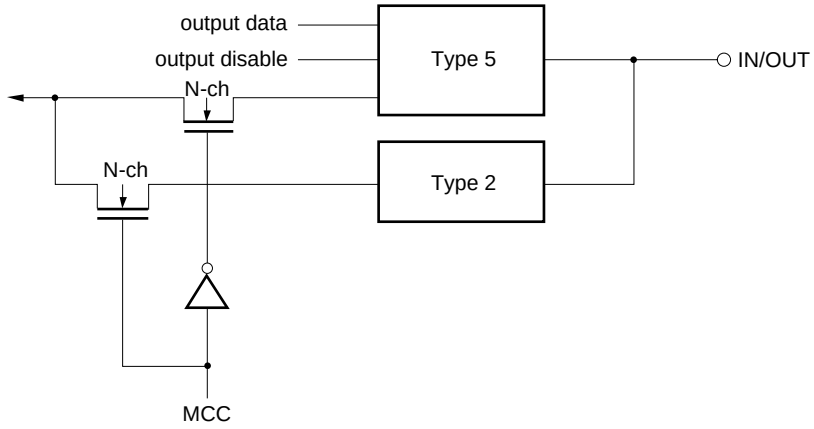
(4) Type 5



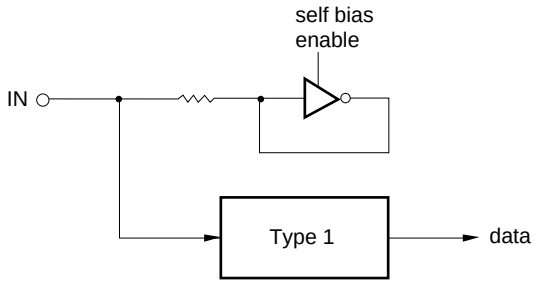
(5) Type 7



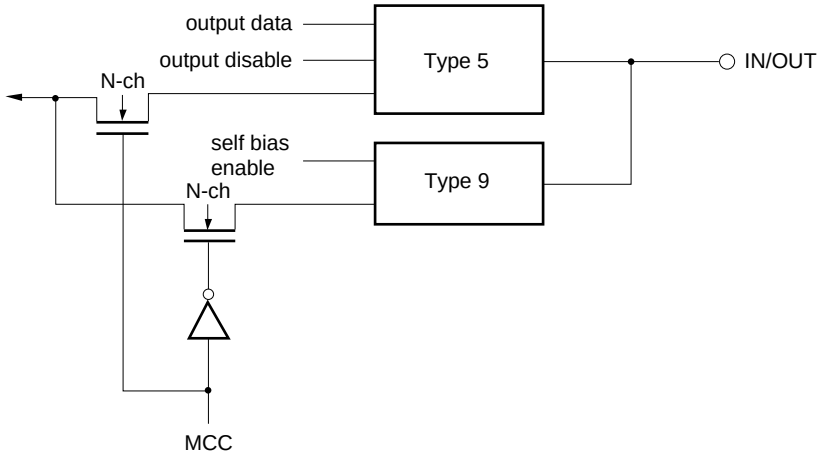
(6) Type 8



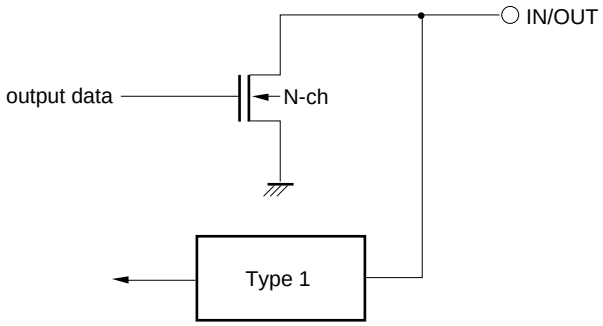
(7) Type 9



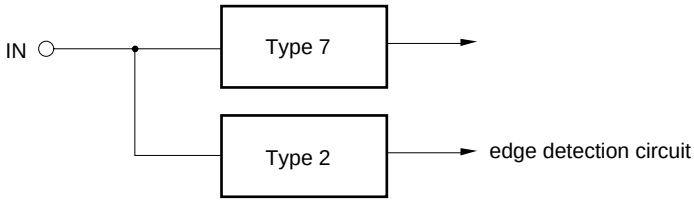
(8) Type 10



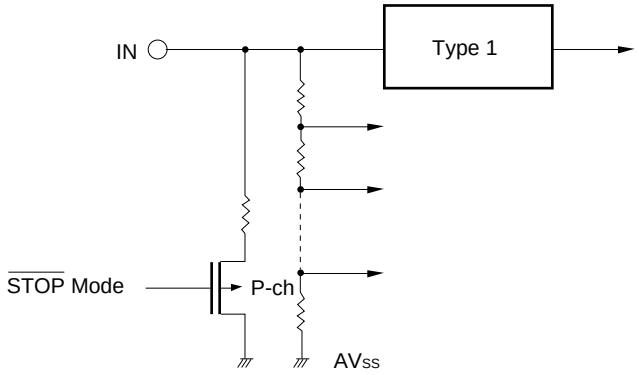
(9) Type 11



(10) Type 12



(11) Type 13



2.3 Recommended Connections for Unused Pins

Pin	Recommended connection
PA7-0 PB7-0 PC7-0 PD7-0 PF7-0	Connect to V_{DD} or V_{SS} via resistor.
$\overline{RD}$ $\overline{WR}$ ALE	Leave unconnected.
$\overline{STOP}$	V_{DD}
INT1, $\overline{NMI}$	Connect to V_{DD} or V_{SS}.
AV_{DD}	Connect to V_{DD}.
V_{AREF} AV_{SS}	Connect to V_{SS}.
AN7-0	Connect to AV_{SS} or AV_{DD}.

3. INSTRUCTION SET

3.1 Operand Expression Format/Description Method

Expression format	Description method
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, ZCM
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D–, H–
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D–, H–, D+byte, H+A, H+B, H+EA, H+byte
rpa3	D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8-bit immediate data
word	16-bit immediate data
byte	8-bit immediate data
bit	3-bit immediate data
f	CY, HC, Z
irf	NMI [Note], FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, OV, AN4, AN5, AN6, AN7, SB

Note NMI can be also described as FNMI.

Remarks

1. sr to sr4 (special register)

PA	: PORT A	ETMM	: TIMER/EVENT
PB	: PORT B		COUNTER MODE
PC	: PORT C	EOM	: TIMER/EVENT
PD	: PORT D		COUNTER OUTPUT
PF	: PORT F		MODE
MA	: MODE A	ANM	: A/D CHANNEL MODE
MB	: MODE B	CR0	: A/D CONVERSION
MC	: MODE C	to	RESULT 0 to 3
MCC	: MODE CONTROL C	CR3	
MF	: MODE F	TXB	: Tx BUFFER
MM	: MEMORY MAPPING	RXB	: Rx BUFFER
TM0	: TIMER REG0	SMH	: SERIAL MODE High
TM1	: TIMER REG1	SML	: SERIAL MODE Low
TMM	: TIMER MODE	MKH	: MASK High
ETM0	: TIMER/EVENT	MKL	: MASK Low
	COUNTER REG0	ZCM	: ZERO CROSS MODE
ETM1	: TIMER/EVENT		
	COUNTER REG1		
ECNT	: TIMER/EVENT		
	COUNTER UPCOUNTER		
ECPT	: TIMER/EVENT		
	COUNTER CAPTURE		

2. rp to rp3 (register pair)

SP	: STACK POINTER
B	: BC
D	: DE
H	: HL
V	: VA
EA	: EXTENDED ACCUMULATOR

3. rpa to rpa3 (rp addressing)

B	: (BC)
D	: (DE)
H	: (HL)
D+	: (DE)+
H+	: (HL)+
D–	: (DE)–
H–	: (HL)–
D++	: (DE)++
H++	: (HL)++
D+byte	: (DE+byte)
H+A	: (HL+A)
H+B	: (HL+B)
H+EA	: (HL+EA)
H+byte	: (HL+byte)

4. f (flag)

CY	: CARRY
HC	: HALF CARRY
Z	: ZERO

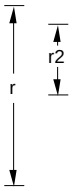
5. irf (interrupt flag)

NMI	: NMI INPUT
FT0	: INTFT0
FT1	: INTFT1
F1	: INTF1
F2	: INTF2
FE0	: INTFE0
FE1	: INTFE1
FEIN	: INTFEIN
FAD	: INTFAD
FSR	: INTFSR
FST	: INTFST
ER	: ERROR
OV	: OVERFLOW
AN4	: ANALOG INPUT
to	4 to 7
AN7	
SB	: STANDBY

3.2 Instruction Code Description

r

R_2	R_1	R_0	reg
0	0	0	V
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

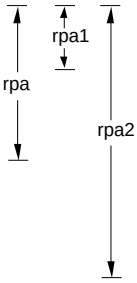


r1

T_2	T_1	T_0	reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

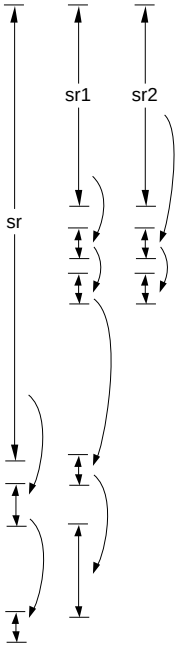
rpa

A_3	A_2	A_1	A_0	addressing
0	0	0	0	——
0	0	0	1	(BC)
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DE)^+$
0	1	0	1	$(HL)^+$
0	1	1	0	$(DE)^-$
0	1	1	1	$(HL)^-$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)



sr

S_5	S_4	S_3	S_2	S_1	S_0	Special-reg
0	0	0	0	0	0	PA
0	0	0	0	0	1	PB
0	0	0	0	1	0	PC
0	0	0	0	1	1	PD
0	0	0	1	0	1	PF
0	0	0	1	1	0	MKH
0	0	0	1	1	1	MKL
0	0	1	0	0	0	ANM
0	0	1	0	0	1	SMH
0	0	1	0	1	0	SML
0	0	1	0	1	1	EOM
0	0	1	1	0	0	ETMM
0	0	1	1	0	1	TMM
0	1	0	0	0	0	MM
0	1	0	0	0	1	MCC
0	1	0	0	1	0	MA
0	1	0	0	1	1	MB
0	1	0	1	0	0	MC
0	1	0	1	1	1	MF
0	1	1	0	0	0	TXB
0	1	1	0	0	1	RXB
0	1	1	0	1	0	TM0
0	1	1	0	1	1	TM1
1	0	0	0	0	0	CR0
1	0	0	0	0	1	CR1
1	0	0	0	1	0	CR2
1	0	0	0	1	1	CR3
1	0	1	0	0	0	ZCM



rpa3

C_3	C_2	C_1	C_0	addressing
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DE)^{++}$
0	1	0	1	$(HL)^{++}$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)

irf

I_4	I_3	I_2	I_1	I_0	INTF
0	0	0	0	0	NMI
0	0	0	0	1	FT0
0	0	0	1	0	FT1
0	0	0	1	1	F1
0	0	1	0	0	F2
0	0	1	0	1	FE0
0	0	1	1	0	FE1
0	0	1	1	1	FEIN
0	1	0	0	0	FAD
0	1	0	0	1	FSR
0	1	0	1	0	FST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

sr3

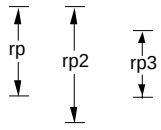
U_0	Special-reg
0	ETM0
1	ETM1

sr4

V_0	Special-reg
0	ECNT
1	ECPT

rp

P_2	P_1	P_0	reg-pair
0	0	0	SP
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA



rp1

Q_2	Q_1	Q_0	reg-pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

f

F_2	F_1	F_0	flag
0	0	0	—
0	1	0	CY
0	1	1	HC
1	0	0	Z

3.3 Instruction Execution Time

In the following table, one state consists of three clock cycles. So, when the 15 MHz clock is used, one state becomes 200 ns (= 3 x 1/15 μs). Execution time of the 4-state instruction, the shortest instruction, becomes 0.8 μs.

Instruction group	Mnemonic		Operand	Instruction code B1	B2	B3	B4	State	Operation	Skip condition
8-bit data transfer	MOV		r1, A	0 0 0 1 1 T_2 T_1 T_0				4	r1 ← A	
			A, r1	0 0 0 0 1 T_2 T_1 T_0				4	A ← r1	
		*	sr, A	0 1 0 0 1 1 0 1	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		*	A, sr1	0 1 0 0 1 1 0 0	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
			r, word	0 1 1 1 0 0 0 0	0 1 1 0 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	0 1 1 1 0 0 0 0	0 1 1 1 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
	MVI	*	r, byte	0 1 1 0 1 R_2 R_1 R_0	← Data →			7	r ← byte	
			sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 0 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	0 1 1 1 0 0 0 1	← Offset →	Data		13	(V. wa) ← byte	
	MVIX	*	rpa1, byte	0 1 0 0 1 0 A_1 A_0	← Data →			10	(rpa1) ← byte	
	STAW	*	wa	0 1 1 0 0 0 1 1	← Offset →			10	(V. wa) ← A	
	LDAW	*	wa	0 0 0 0 0 0 0 1	← Offset →			10	A ← (V. wa)	
	STAX	*	rpa2	A_3 0 1 1 1 A_2 A_1 A_0	Data[Note 1]			[Note 3] 7/13	(rpa2) ← A	
	LDAX	*	rpa2	A_3 0 1 0 1 A_2 A_1 A_0	Data[Note 1]			[Note 3] 7/13	A ← (rpa2)	
	EXX			0 0 0 1 0 0 0 1				4	{B ↔ B', C ↔ C', D ↔ D' E ↔ E', H ↔ H', L ↔ L'	
	EXA			0 0 0 1 0 0 0 0				4	V, A ↔ V', A', EA ↔ EA'	
	EXH			0 1 0 1 0 0 0 0				4	H, L ↔ H', L'	
	BLOCK			0 0 1 1 0 0 0 1				13 (C+1)	$(DE)^+$ ← $(HL)^+$, C ← C–1 End if borrow	
16-bit data transfer	DMOV		rp3, EA	1 0 1 1 0 1 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	1 0 1 0 0 1 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	State	Operation	Skip condition
16-bit data transfer	DMOV	sr3, EA	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0			14	sr3 ← EA	
		EA, sr4	↓	1 1 0 0 0 0 0 V_0			14	EA ← sr4	
	SBCD	word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 0	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED	word	↓	0 0 1 0 1 1 1 0	↓	↓	20	(word) ← E, (word+1) ← D	
	SHLD	word	↓	0 0 1 1 1 1 1 0	↓	↓	20	(word) ← L, (word+1) ← H	
	SSPD	word	↓	0 0 0 0 1 1 1 0	↓	↓	20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX	rpa3	0 1 0 0 1 0 0 0	1 0 0 1 C_3 C_2 C_1 C_0	Data Note 2		Note 3 14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD	word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 1	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED	word	↓	0 0 1 0 1 1 1 1	↓	↓	20	E ← (word), D ← (word+1)	
	LHLD	word	↓	0 0 1 1 1 1 1 1	↓	↓	20	L ← (word), H ← (word+1)	
	LSPD	word	↓	0 0 0 0 1 1 1 1	↓	↓	20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX	rpa3	0 1 0 0 1 0 0 0	1 0 0 0 C_3 C_2 C_1 C_0	Data Note 2		Note 3 14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH	rp1	1 0 1 1 0 Q_2 Q_1 Q_0				13	(SP–1)← $rp1_H$, (SP–2)← $rp1_L$ SP ← SP–2	
	POP	rp1	1 0 1 0 0 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI *	rp2, word	0 P_2 P_1 P_0 0 1 0 0	← Low Byte →	High Byte		10	rp2 ← word	
	TABLE		0 1 0 0 1 0 0 0	1 0 1 0 1 0 0 0			17	C ← (PC+3+A) B ← (PC+3+A+1)	
8-bit arithmetic operation (register)	ADD	A, r	0 1 1 0 0 0 0 0	1 1 0 0 0 R_2 R_1 R_0			8	A ← A+r	
		r, A	↓	0 1 0 0			8	r ← r+A	
	ADC	A, r	↓	1 1 0 1			8	A ← A+r+CY	
		r, A	↓	0 1 0 1			8	r ← r+A+CY	

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	State	Operation	Skip condition
8-bit arithmetic operation (register)	ADDNC	A, r	0 1 1 0 0 0 0 0	1 0 1 0 0 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		0 0 1 0			8	r ← r+A	No Carry
	SUB	A, r		1 1 1 0			8	A ← A–r	
		r, A		0 1 1 0			8	r ← r–A	
	SBB	A, r		1 1 1 1			8	A ← A–r–CY	
		r, A		0 1 1 1			8	r ← r–A–CY	
	SUBNB	A, r		1 0 1 1			8	A ← A–r	No Borrow
		r, A		0 0 1 1			8	r ← r–A	No Borrow
	ANA	A, r		1 0 0 0 1 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		0 0 0 0			8	r ← r ∧ A	
	ORA	A, r		1 0 0 1			8	A ← A ∨ r	
		r, A		0 0 0 1			8	r ← r ∨ A	
	XRA	A, r		1 0 0 1 0 R_2 R_1 R_0			8	A ← A ∀ r	
		r, A		0 0 0 1			8	r ← r ∀ A	
	GTA	A, r		1 0 1 0 1 R_2 R_1 R_0			8	A–r–1	No Borrow
		r, A		0 0 1 0			8	r–A–1	No Borrow
	LTA	A, r		1 0 1 1			8	A–r	Borrow
		r, A		0 0 1 1			8	r–A	Borrow
	NEA	A, r		1 1 1 0			8	A–r	No Zero
		r, A		0 1 1 0			8	r–A	No Zero

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	State	Operation	Skip condition
8-bit arithmetic operation (register)	EQA	A, r	0 1 1 0 0 0 0 0	1 1 1 1 1 R_2 R_1 R_0			8	A–r	Zero
		r, A	↓	0 1 1 1			8	r–A	Zero
	ONA	A, r	↓	1 1 0 0			8	A∧r	No Zero
	OFFA	A, r	↓	1 1 0 1			8	A∧r	Zero
8-bit arithmetic operation (memory)	ADDX	rpa	0 1 1 1 0 0 0 0	1 1 0 0 0 A_2 A_1 A_0			11	A ← A+(rpa)	
	ADCX	rpa	↓	1 1 0 1			11	A ← A+(rpa)+CY	
	ADDNCX	rpa	↓	1 0 1 0			11	A ← A+(rpa)	No Carry
	SUBX	rpa	↓	1 1 1 0			11	A ← A–(rpa)	
	SBBX	rpa	↓	1 1 1 1			11	A ← A–(rpa)–CY	
	SUBNBX	rpa	↓	1 0 1 1			11	A ← A–(rpa)	No Borrow
	ANAX	rpa	↓	1 0 0 0 1 A_2 A_1 A_0			11	A ← A∧(rpa)	
	ORAX	rpa	↓	1 0 0 1			11	A ← A∨(rpa)	
	XRAX	rpa	↓	1 0 0 1 0 A_2 A_1 A_0			11	A ← A∀(rpa)	
	GTAX	rpa	↓	1 0 1 0 1 A_2 A_1 A_0			11	A–(rpa)–1	No Borrow
	LTAX	rpa	↓	1 0 1 1			11	A–(rpa)	Borrow
	NEAX	rpa	↓	1 1 1 0			11	A–(rpa)	No Zero
	EQAX	rpa	↓	1 1 1 1			11	A–(rpa)	Zero
	ONAX	rpa	↓	1 1 0 0			11	A∧(rpa)	No Zero
	OFFAX	rpa	↓	1 1 0 1			11	A∧(rpa)	Zero

Instruction group	Mnemonic		Operand	Instruction code B1	B2	B3	B4	State	Operation	Skip condition
Arithmetic operation of immediate data	ADI	*	A, byte	0 1 0 0 0 1 1 0	← Data →			7	A ← A+byte	
			r, byte	0 1 1 1 0 1 0 0	0 1 0 0 0 R_2 R_1 R_0	Data		11	r ← r+byte	
			sr2, byte	0 1 1 0 ↓	S_3 1 0 0 0 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI	*	A, byte	0 1 0 1 0 1 1 0	← Data →			7	A ← A+byte+CY	
			r, byte	0 1 1 1 0 1 0 0	0 1 0 1 0 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
			sr2, byte	0 1 1 0 ↓	S_3 1 0 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC	*	A, byte	0 0 1 0 0 1 1 0	← Data →			7	A ← A+byte	No Carry
			r, byte	0 1 1 1 0 1 0 0	0 0 1 0 0 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
			sr2, byte	0 1 1 0 ↓	S_3 0 1 0 0 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI	*	A, byte	0 1 1 0 0 1 1 0	← Data →			7	A ← A–byte	
			r, byte	0 1 1 1 0 1 0 0	0 1 1 0 0 R_2 R_1 R_0	Data		11	r ← r–byte	
			sr2, byte	0 1 1 0 ↓	S_3 1 1 0 0 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	
	SBI	*	A, byte	0 1 1 1 0 1 1 0	← Data →			7	A ← A–byte–CY	
			r, byte	0 1 1 1 0 1 0 0	0 1 1 1 0 R_2 R_1 R_0	Data		11	r ← r–byte–CY	
			sr2, byte	0 1 1 0 ↓	S_3 1 1 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte–CY	
	SUINB	*	A, byte	0 0 1 1 0 1 1 0	← Data →			7	A ← A–byte	No Borrow
			r, byte	0 1 1 1 0 1 0 0	0 0 1 1 0 R_2 R_1 R_0	Data		11	r ← r–byte	No Borrow
			sr2, byte	0 1 1 0 ↓	S_3 0 1 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	No Borrow
	ANI	*	A, byte	0 0 0 0 0 1 1 1	← Data →			7	A← A ∧ byte	
			r, byte	0 1 1 1 0 1 0 0	0 0 0 0 1 R_2 R_1 R_0	Data		11	r ← r ∧ byte	

Instruction group	Mnemonic		Operand	Instruction code B1	B2	B3	B4	State	Operation	Skip condition
Arithmetic operation of immediate data	ANI		sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 1 S_2 S_1 S_0	Data		20	sr2 ← sr2 ∧ byte	
	ORI	*	A, byte	0 0 0 1 0 1 1 1	← Data →			7	A ← A ∨ byte	
			r, byte	0 1 1 1 0 1 0 0	0 0 0 1 1 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
			sr2, byte	0 1 1 0 ↓	S_3 0 0 1 1 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI	*	A, byte	0 0 0 1 0 1 1 0	← Data →			7	A ← A ∨̄ byte	
			r, byte	0 1 1 1 0 1 0 0	0 0 0 1 0 R_2 R_1 R_0	Data		11	r ← r ∨̄ byte	
			sr2, byte	0 1 1 0 ↓	S_3 0 0 1 0 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨̄ byte	
	GTI	*	A, byte	0 0 1 0 0 1 1 1	← Data →			7	A–byte–1	No Borrow
			r, byte	0 1 1 1 0 1 0 0	0 0 1 0 1 R_2 R_1 R_0	Data		11	r–byte–1	No Borrow
			sr2, byte	0 1 1 0 ↓	S_3 0 1 0 1 S_2 S_1 S_0	↓		14	sr2–byte–1	No Borrow
	LTI	*	A, byte	0 0 1 1 0 1 1 1	← Data →			7	A–byte	Borrow
			r, byte	0 1 1 1 0 1 0 0	0 0 1 1 1 R_2 R_1 R_0	Data		11	r–byte	Borrow
			sr2, byte	0 1 1 0 ↓	S_3 0 1 1 1 S_2 S_1 S_0	↓		14	sr2–byte	Borrow
	NEI	*	A, byte	0 1 1 0 0 1 1 1	← Data →			7	A–byte	No Zero
			r, byte	0 1 1 1 0 1 0 0	0 1 1 0 1 R_2 R_1 R_0	Data		11	r–byte	No Zero
			sr2, byte	0 1 1 0 ↓	S_3 1 1 0 1 S_2 S_1 S_0	↓		14	sr2–byte	No Zero
	EQI	*	A, byte	0 1 1 1 0 1 1 1	← Data →			7	A–byte	Zero
			r, byte	0 1 1 1 0 1 0 0	0 1 1 1 1 R_2 R_1 R_0	Data		11	r–byte	Zero
			sr2, byte	0 1 1 0 ↓	S_3 1 1 1 1 S_2 S_1 S_0	↓		14	sr2–byte	Zero

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	State	Operation	Skip condition
Arithmetic operation of immediate data	ONI *	A, byte	0 1 0 0 0 1 1 1	← Data →			7	A ∧ byte	No Zero
		r, byte	0 1 1 1 0 1 0 0	0 1 0 0 1 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
		sr2, byte	0 1 1 0 ↓	S_3 1 0 0 1 S_2 S_1 S_0	↓		14	sr2 ∧ byte	No Zero
	OFFI *	A, byte	0 1 0 1 0 1 1 1	← Data →			7	A ∧ byte	Zero
		r, byte	0 1 1 1 0 1 0 0	0 1 0 1 1 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
		sr2, byte	0 1 1 0 ↓	S_3 1 0 1 1 S_2 S_1 S_0	↓		14	sr2 ∧ byte	Zero
Arithmetic operation of working register	ADDW	wa	0 1 1 1 0 1 0 0	1 1 0 0 0 0 0 0	offset		14	A ← A+(V.wa)	
	ADCW	wa	↓ ↓ ↓	1 1 0 1 ↓	↓ ↓		14	A ← A+(V.wa)+CY	
	ADDNCW	wa	↓ ↓ ↓	1 0 1 0 ↓	↓ ↓		14	A ← A+(V.wa)	No Carry
	SUBW	wa	↓ ↓ ↓	1 1 1 0 ↓	↓ ↓		14	A ← A–(V.wa)	
	SBBW	wa	↓ ↓ ↓	1 1 1 1 ↓	↓ ↓		14	A ← A–(V.wa)–CY	
	SUBNBW	wa	↓ ↓ ↓	1 0 1 1 ↓	↓ ↓		14	A ← A–(V.wa)	No Borrow
	ANAW	wa	↓ ↓ ↓	1 0 0 0 1 0 0 0	↓ ↓		14	A ← A ∧ (V.wa)	
	ORAW	wa	↓ ↓ ↓	1 0 0 1 ↓	↓ ↓		14	A ← A ∨ (V.wa)	
	XRAW	wa	↓ ↓ ↓	1 0 0 1 0 0 0 0	↓ ↓		14	A ← A ∀ (V.wa)	
	GTAW	wa	↓ ↓ ↓	1 0 1 0 1 0 0 0	↓ ↓		14	A–(V.wa)–1	No Borrow
	LTAW	wa	↓ ↓ ↓	1 0 1 1 ↓	↓ ↓		14	A–(V.wa)	Borrow
	NEAW	wa	↓ ↓ ↓	1 1 1 0 ↓	↓ ↓		14	A–(V.wa)	No Zero
	EQAW	wa	↓ ↓ ↓	1 1 1 1 ↓	↓ ↓		14	A–(V.wa)	Zero
	ONAW	wa	↓ ↓ ↓	1 1 0 0 ↓	↓ ↓		14	A ∧ (V.wa)	No Zero

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	State	Operation	Skip condition
Arithmetic operation of working register	OFFAW	wa	0 1 1 1 0 1 0 0	1 1 0 1 1 0 0 0	Offset		14	A ∧ (V.wa)	Zero
	ANIW *	wa, byte	0 0 0 0 0 1 0 1	← Offset →	Data		19	(V.wa) ← (V.wa) ∧ byte	
	ORIW *	wa, byte	0 0 0 1				19	(V.wa) ← (V.wa) ∨ byte	
	GTIW *	wa, byte	0 0 1 0				13	(V.wa)–byte–1	No Borrow
	LTIW *	wa, byte	0 0 1 1				13	(V.wa)–byte	Borrow
	NEIW *	wa, byte	0 1 1 0				13	(V.wa)–byte	No Zero
	EQIW *	wa, byte	0 1 1 1				13	(V.wa)–byte	Zero
	ONIW *	wa, byte	0 1 0 0				13	(V.wa) ∧ byte	No Zero
	OFFIW *	wa, byte	0 1 0 1				13	(V.wa) ∧ byte	Zero
16-bit arithmetic operation	EADD	EA, r2	0 1 1 1 0 0 0 0	0 1 0 0 0 0 R_1 R_0			11	EA ← EA+r2	
	DADD	EA, rp3	0 1 0 0	1 1 0 0 0 1 P_1 P_0			11	EA ← EA+rp3	
	DADC	EA, rp3		1 1 0 1			11	EA ← EA+rp3+CY	
	DADDNC	EA, rp3		1 0 1 0			11	EA ← EA+rp3	No Carry
	ESUB	EA, r2	0 0 0 0	0 1 1 0 0 0 R_1 R_0			11	EA ← EA–r2	
	DSUB	EA, rp3	0 1 0 0	1 1 1 0 0 1 P_1 P_0			11	EA ← EA–rp3	
	DSBB	EA, rp3		1 1 1 1			11	EA ← EA–rp3–CY	
	DSUBNB	EA, rp3		1 0 1 1			11	EA ← EA–rp3	No Borrow
	DAN	EA, rp3		1 0 0 0 1 1 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1 0 0 1			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		1 0 0 1 0 1 P_1 P_0			11	EA ← EA ∀ rp3	

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	State	Operation	Skip condition
16-bit arithmetic operation	DGT	EA, rp3	0 1 1 1 0 1 0 0	1 0 1 0 1 1 P_1 P_0			11	EA–rp3–1	No Borrow
	DLT	EA, rp3	↓	1 0 1 1			11	EA–rp3	Borrow
	DNE	EA, rp3	↓	1 1 1 0			11	EA–rp3	No Zero
	DEQ	EA, rp3	↓	1 1 1 1			11	EA–rp3	Zero
	DON	EA, rp3	↓	1 1 0 0			11	EA∧rp3	No Zero
	DOFF	EA, rp3	↓	1 1 0 1			11	EA∧rp3	Zero
Multiply/divide	MUL	r2	0 1 0 0 1 0 0 0	0 0 1 0 1 1 R_1 R_0			32	EA ← A×r2	
	DIV	r2	↓	0 0 1 1			59	EA ← EA÷r2, r2 ← The Remainder	
Decrement/Increment	INR	r2	0 1 0 0 0 0 R_1 R_0				4	r2 ← r2+1	Carry
	INRW *	wa	0 0 1 0 0 0 0 0	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	0 0 P_1 P_0 0 0 1 0				7	rp ← rp+1	
		EA	1 0 1 0 1 0 0 0				7	EA ← EA+1	
	DCR	r2	0 1 0 1 0 0 R_1 R_0				4	r2 ← r2–1	Borrow
	DCRW *	wa	0 0 1 1 0 0 0 0	← Offset →			16	(V.wa) ← (V.wa)–1	Borrow
	DCX	rp	0 0 P_1 P_0 0 0 1 1				7	rp ← rp–1	
		EA	1 0 1 0 1 0 0 1				7	EA ← EA–1	
Other arithmetic operation	DAA		0 1 1 0 0 0 0 1				4	Decimal Adjust Accumulator	
	STC		0 1 0 0 1 0 0 0	0 0 1 0 1 0 1 1			8	CY ← 1	
	CLC		↓	0 0 1 0 1 0 1 0			8	CY ← 0	
	NEGA		↓	0 0 1 1 1 0 1 0			8	A ← $\overline{A}$+1	

Instruction group	Mnemonic	Operand	Instruction code B1	Instruction code B2	Instruction code B3	Instruction code B4	State	Operation	Skip condition
Rotation shift	RLD		0 1 0 0 1 0 0 0	0 0 1 1 1 0 0 0			17	Rotate Left Digit	
	RRD			1 0 0 1			17	Rotate Right Digit	
	RLL	r2		0 1 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		0 0 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		0 0 1 0 0 1 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		0 0 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		0 0 0 0 0 1 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		0 0 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA		1 0 1 1 0 1 0 0			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0 0 0 0			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA		1 0 1 0 0 0 1 0 0			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0 0 0 0			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	
Jump	JMP *	word	0 1 0 1 0 1 0 0	← Low Adrs →	High Adrs		10	PC ← word	
	JB		0 0 1 0 0 0 0 1				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
	JR	word	1 1 ← jdisp 1 →				10	PC ← PC+1+jdisp 1	
	JRE *	word	0 1 0 0 1 1 1 ←	jdisp →			10	PC ← PC+2+jdisp	
	JEA		0 1 0 0 1 0 0 0	0 0 1 0 1 0 0 0			8	PC ← EA	
Call	CALL *	word	0 1 0 0 0 0 0 0	← Low Adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$ PC ← word, SP ← SP–2	
	CALB		0 1 0 0 1 0 0 0	0 0 1 0 1 0 0 1			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$ $PC_H \leftarrow B$, $PC_L \leftarrow C$, SP ← SP–2	
	CALF *	word	0 1 1 1 1 ←	fa →			13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$ $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow fa$, SP ← SP–2	

Instruction group	Mnemonic	Operand	Instruction code B1	B2	B3	B4	State	Operation	Skip condition
Call	CALT	word	1 0 0 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, $SP \leftarrow SP-2$	
	SOFT1		0 1 1 1 0 0 1 0				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, $PC \leftarrow 0060H$, $SP \leftarrow SP-3$	
Return	RET		1 0 1 1 1 0 0 0				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	
	RETS		↓ 1 0 0 1				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, $SP \leftarrow SP+2$ $PC \leftarrow PC+n$	Unconditional
	RETI		0 1 1 0 0 0 1 0				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2)$, $SP \leftarrow SP+3$	
Skip	BIT *	bit, wa	0 1 0 1 1 B_2 B_1 B_0	← Offset →			10	Skip if (V.wa) bit = 1	(V.wa) bit = 1
	SK	f	0 1 0 0 1 0 0 0	0 0 0 0 1 F_2 F_1 F_0			8	Skip if f = 1	f = 1
	SKN	f	↓	0 0 0 1 ↓			8	Skip if f = 0	f = 0
	SKIT	irf	↓	0 1 0 I_4 I_3 I_2 I_1 I_0			8	Skip if irf = 1, then reset irf	irf = 1
	SKNIT	irf	↓	0 1 1 I_4 I_3 I_2 I_1 I_0			8	Skip if irf = 0 Reset irf, if irf = 1	irf = 0
CPU operation	NOP		0 0 0 0 0 0 0 0				4	No Operation	
	EI		1 0 1 0 1 0 1 0				4	Enable Interrupt	
	DI		1 0 1 1 1 0 1 0				4	Disable Interrupt	
	HLT		0 1 0 0 1 0 0 0	0 0 1 1 1 0 1 1			12	Set Halt Mode	
	STOP		0 1 0 0 1 0 0 0	1 0 1 1 1 0 1 1			12	Set Stop Mode	

Notes 1. B2 (Data) is applied for rpa2 = D + byte or H + byte.
2. B3 (Data) is applied for rpa3 = D + byte or H + byte.
3. In the "state" column, data to the right of the slash applies when rpa2 or rpa3 is D + byte, H + A, H + B, H + EA, or H + byte.

Remark When the instructions below are skipped, the number of idle states is as listed below and differs from the number of execution states.

1-byte instruction	: 4-state	3-byte instruction (with *)	: 10-state
2-byte (with *)	: 7-state	3-byte	: 11-state
2-byte	: 8-state	4-byte	: 14-state

4. LIST OF MODE REGISTERS

Name of mode register		Read/Write	Function
MA	MODE A	W	Specifies input/output of Port A in bit units
MB	MODE B	W	Specifies input/output of Port B in bit units
MCC	MODE CONTROL C	W	Specifies port/control mode of Port C in bit units
MC	MODE C	W	Specifies input/output of Port C set in the port mode in bit units
MM	MEMORY MAPPING	W	Specifies port/expansion mode of Ports D and F
MF	MODE F	W	Specifies input/output of Port F set in the port mode in bit units
TMM	Timer mode	R/W	Specifies operation mode of the timer
ETMM	Timer/Event Counter Mode	W	Specifies operation mode of the Timer Event Counter
EOM	Timer/Event Counter Output Mode	R/W	Controls output level of CO0 and CO1
SML	Serial Mode	W	Specifies operation mode of the serial interface
SMH		R/W	
MKL	Interrupt Mask	R/W	Specifies interrupt request enable/disable
MKH			
ANM	A/D Channel Mode	R/W	Specifies operation mode of the A/D converter
ZCM	Zero-cross Mode	W	Specifies operation mode of the zero-cross detection circuit

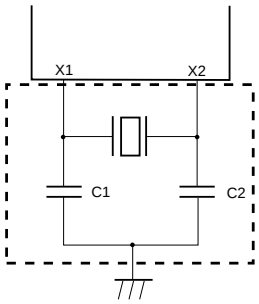
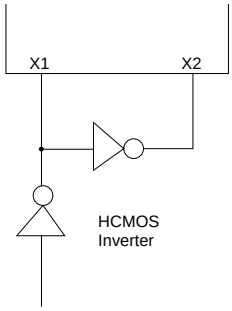
5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 ˚C)

Parameter	Symbol	Test Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input Voltage	V_I		–0.5 to V_{DD} + 0.5	V
Output Voltage	V_O		–0.5 to V_{DD} + 0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	–2.0	mA
		All Output Pin Total	–50	mA
A/D Converter Reference Input Voltage	V_{AREF}		–0.5 to AV_{DD} + 0.3	V
Operating Ambient Temperature	T_A		–40 to +85	˚C
Storage Temperature	T_{stg}		–65 to +150	˚C

* **Caution If any of the parameters exceeds the absolute maximum ratings even for a moment, this may damage product quality. The absolute maximum ratings are values that may physically damage the product. You must use the product within the specified ratings.**

Oscillation Characteristics (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

Resonator	Recommended Circuits	Parameter	Test Conditions	MIN.	MAX.	UNIT
Ceramic Resonator or Crystal Resonator[Note]		Oscillation Frequency (fxx)	A/D Converter Not used	4	15	MHz
			A/D Converter Used	5.8	15	MHz
External Clock		X1 Input Frequency (fx)	A/D Converter Not used	4	15	MHz
			A/D Converter Used	5.8	15	MHz
		X1 Input Rise, Fall Time (t_r, t_f)		0	20	ns
		X1 Input High, Low Level Width ($t_{øH}$, $t_{øL}$)		20	250	ns

Cautions 1. Oscillator circuit should be in the nearest area from X1 and X2 pins.

2. Do not place other signal lines within the area enclosed with broken lines.

Note For a crystal resonator, the following external capacitances are recommended: C1 = C2 = 10 pF

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_C = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured pins returned to 0 V			20	pF
I/O Capacitance	C_{IO}				20	pF

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Condition		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN7 to AN4		0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN7 to AN4		0		$0.2V_{DD}$	V
Input High Voltage	V_{IH1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN7 to AN4, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN7 to AN4, X1, X2		$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
Output High Voltage	V_{OH}	I_{OH} = –1.0 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Input Current	I_I	INT1 [Note 1], TI (PC3) [Note 2]; 0 V ≤ V_I ≤ V_{DD}				±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), AN7 to AN0; 0 V ≤ V_I ≤ V_{DD}				±10	μA
		AN7 to AN0; 0 V ≤ V_I ≤ V_{DD}				±1	μA
Output Leakage Current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
AV_{DD} Supply Current	AI_{DD1}	Operation Mode f_{xx} = 15 MHz			0.5	1.3	mA
	AI_{DD2}	STOP Mode			10	20	μA
V_{DD} Supply Current	I_{DD1}	Operation mode f_{xx} = 15 MHz			16	30	mA
	I_{DD2}	HALT Mode f_{xx} = 15 MHz			8	15	mA
Data Retention Voltage	V_{DDDR}	Hardware/Software STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	Hardware/Software STOP Mode [Note 3]	V_{DDDR} = 2.5 V		1	15	μA
			V_{DDDR} = 5 V ± 10 %		10	50	μA

Notes 1. When self-bias is generated by ZCM register.

2. When set in the control mode by MCC register and self-bias is generated by ZCM register.

3. When self-bias is not generated.

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V)

READ/WRITE OPERATION:

Parameter	Symbol	Test Condition	MIN.	MAX.	UNIT
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup Time to ALE	t_{AL}	f_{xx} = 15 MHz, C_L = 150 pF	30		ns
Address Hold Time after ALE ↓	t_{LA}		35		ns
Address → $\overline{RD}$ ↓ Delay Time	t_{AR}		100		ns
$\overline{RD}$ ↓ → Address Floating Time	t_{AFR}	C_L = 150 pF		20	ns
Address → Data Input Time	t_{AD}	f_{xx} = 15 MHz, CL = 150 pF		250	ns
ALE ↓ → Data Input Time	t_{LDR}			135	ns
$\overline{RD}$ ↓ → Data Input Time	t_{RD}			120	ns
ALE ↓ → RD ↓ Delay Time	t_{LR}		15		ns
Data Hold Time after RD ↑	t_{RDH}	C_L = 150 pF	0		ns
$\overline{RD}$ ↑ → ALE ↑ Delay Time	t_{RL}	f_{xx} = 15 MHz, C_L = 150 pF	80		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read f_{xx} = 15 MHz, C_L = 150 pF	215		ns
		OP code Fetch f_{xx} = 15 MHz, C_L = 150 pF	415		ns
ALE Width High	t_{LL}	f_{xx} = 15 MHz, C_L = 150 pF	90		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	f_{xx} = 15 MHz	30		ns
$\overline{M1}$ Hold Time after ALE ↓	t_{LM}		35		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}		30		ns
$\overline{IO}$/M Hold Time after ALE ↓	t_{LI}		35		ns
Address → $\overline{WR}$ ↓ Delay Time	t_{AW}	f_{xx} = 15 MHz, C_L = 150 pF	100		ns
ALE ↓ → Data Output Time	t_{LDW}			180	ns
$\overline{WR}$ ↓ → Data Output Time	t_{WD}	C_L = 150 pF		100	ns
ALE ↓ → $\overline{WR}$ ↓ Delay Time	t_{LW}	f_{xx} = 15 MHz, C_L = 150 pF	15		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}		165		ns
Data Hold Time after $\overline{WR}$ ↑	t_{WDH}		60		ns
$\overline{WR}$ ↑ → ALE ↑ Delay Time	t_{WL}		80		ns
$\overline{WR}$ Width Low	t_{WW}		215		ns

SERIAL OPERATION:

Parameter	Symbol	Test Condition		MIN.	MAX.	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	**Note 1**	800		ns
			Note 2	400		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	**Note 1**	335		ns
			Note 2	160		ns
		$\overline{SCK}$ Output		700		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	**Note 1**	335		ns
			Note 2	160		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	**Note 1**		80		ns
RxD Hold Time After $\overline{SCK}$ ↑	t_{KRX}	**Note 1**		80		ns
$\overline{SCK}$ ↓ → TxD Delay Time	t_{KTX}	**Note 1**			210	ns

Notes 1. In case of x1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.

2. In case of x16 or x64 clock rate in asynchronous mode.

Remark The numeric values in the table apply when f_{XX} = 15 MHz, C_L = 150 pF.

ZERO-CROSS CHARACTERISTICS:

Parameter	Symbol	Test Condition	MIN.	MAX.	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{P-P}
Zero-Cross Accuracy	A_{ZX}	60-Hz Sine Wave		±135	mV
Zero-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATION:

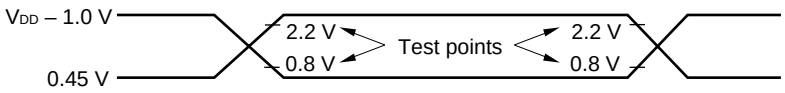
Parameter	Symbol	Test Condition	MIN.	MAX.	UNIT
TI Width High, Low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI Width High, Low	t_{CI1H}, t_{CI1L}	Event Counter Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ Width High, Low	t_{NIH}, t_{NIL}		10		μs
INT1 Width High, Low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ Width High, Low	t_{I2H}, t_{I2L}		36		t_{CYC}
AN7-4 Width High, Low	t_{ANH}, t_{ANL}		36		t_{CYC}
$\overline{RESET}$ Width High, Low	t_{RSH}, t_{RSL}		10		μs

A/D CONVERTER CHARACTERISTICS: (T_A = –40 to +85 ˚C, V_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute Accuracy [Note]		3.4 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.8 %	FSR
		4.0 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.6 %	FSR
		T_A = –10 to +70 ˚C, 4.0 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 170 ns			±0.4 %	FSR
Conversion time	t_{CONV}	66 ns ≤ t_{CYC} ≤ 110 ns	576			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 170 ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66 ns ≤ t_{CYC} ≤ 110 ns	96			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 170 ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}	AN7-0 (include unused pins)	0		V_{AREF}	V
Analog Input Impedance	R_{AN}			50		MΩ *
Reference Voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} Current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} Supply Current	AI_{DD1}	Operation mode, f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note Except quantization error (i.e. ±1/2 LSB).

AC TIMING TEST POINTS



AC CHARACTERISTIC CALCULATING EXPRESSION depending on t_{CYC}

Symbol	Calculating Expression	MIN./MAX.	UNIT
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (Data Read)	MIN.	ns
	7T – 50 (OP Code Fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{ML}	2T – 100	MIN.	ns
t_{LM}	T – 30	MIN.	ns
t_{IL}	2T – 100	MIN.	ns
t_{LI}	T – 30	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 100	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	6T ($\overline{SCK}$ Input) Note 1 /12T ($\overline{SCK}$ Input) Note 2	MIN.	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	2.5T + 5 ($\overline{SCK}$ Input) Note 1 /5T + 5 ($\overline{SCK}$ Input) Note 2	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		
t_{KKH}	2.5T + 5 ($\overline{SCK}$ Input) Note 1 /5T + 5 ($\overline{SCK}$ Input) Note 2	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		

Notes 1. In case of x16 or x64 clock rate in asynchronous mode.

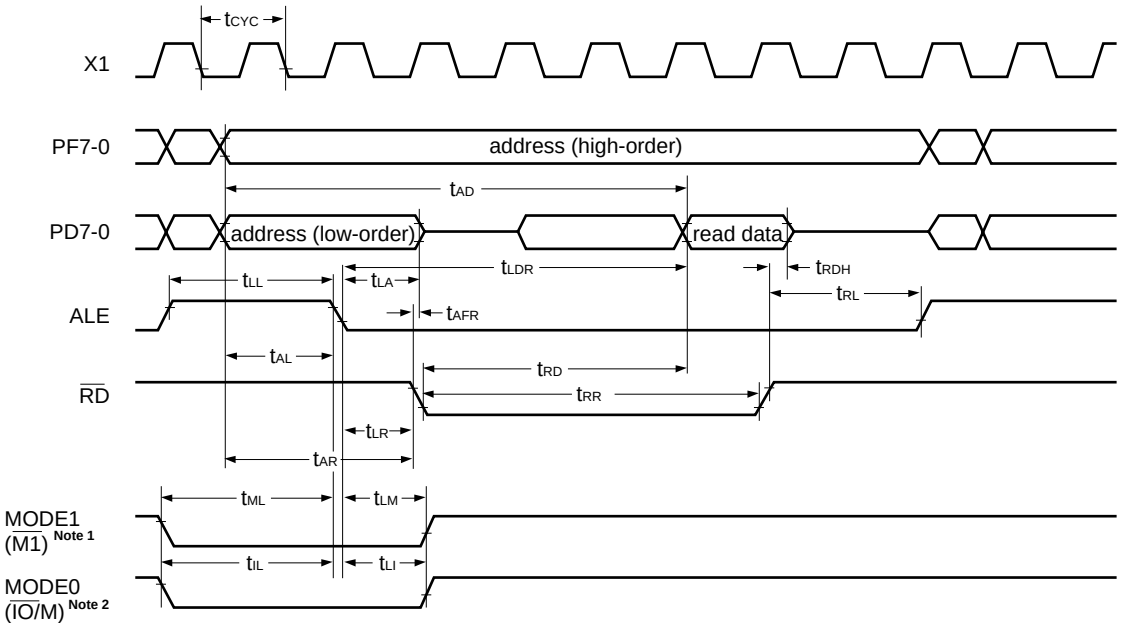
2. In case of x1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.

Remarks 1. $T = t_{CYC} = 1/f_{XX}$

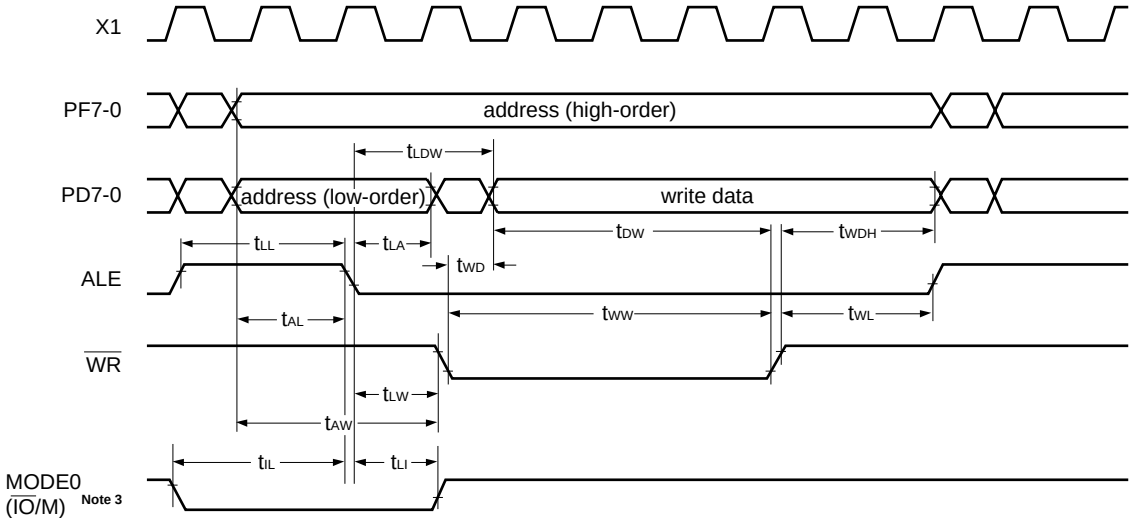
2. Symbols that cannot be found in this table do not depend on the oscillation frequency (f_{XX}).

Timing Waveform

Read Operation



Write Operation

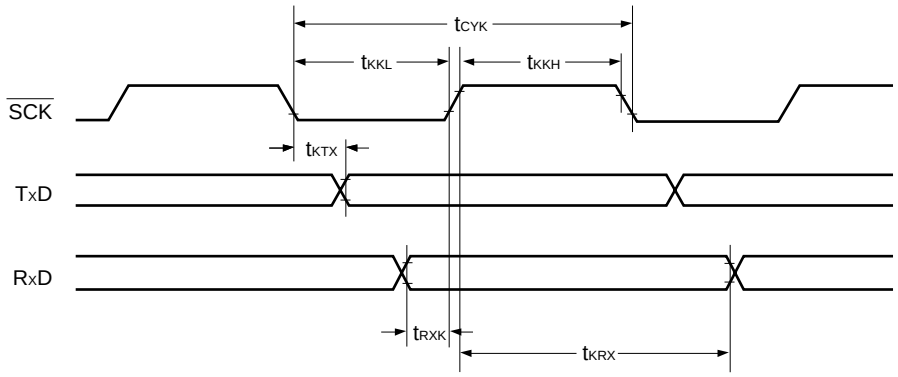


Notes 1. M1 signal is output to MODE1 pin at first OP code fetch cycle if MODE1 pin is pulled up.

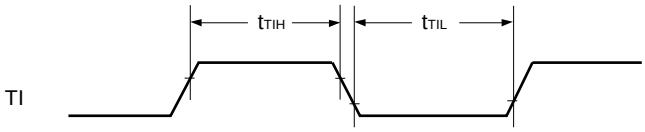
2. IO/M signal is output to MODE0 pin at sr to sr2 register read cycle if MODE0 pin is pulled up.

3. IO/M signal is output to MODE0 pin at sr to sr2 register write cycle if MODE0 pin is pulled up.

Serial Operation

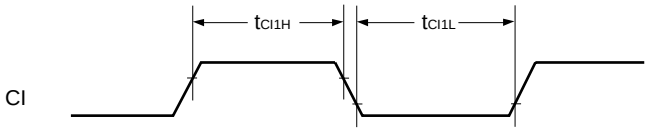


Timer Input Timing

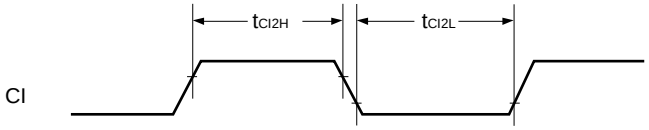


Timer/Event Counter Input Timing

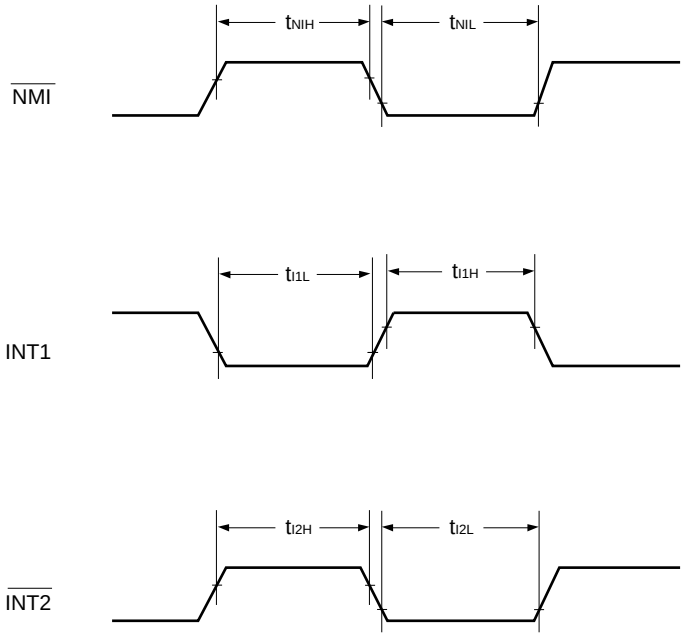
Event Counter Mode



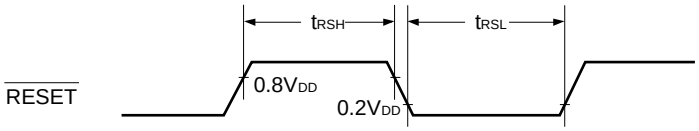
Pulse Width Measurement Mode



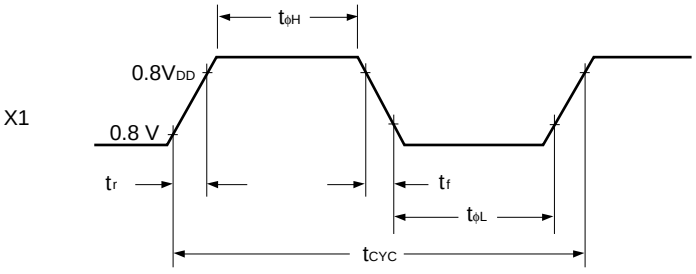
Interrupt Input Timing



RESET Input Timing



External Clock Timing

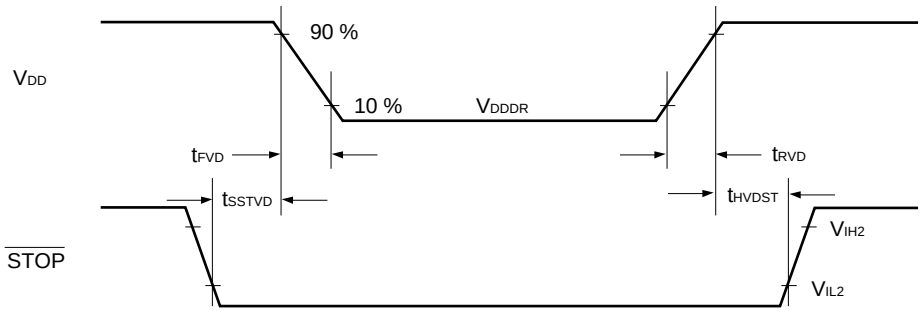


Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.5		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.5 V		1	15	μA
*		V_{DDDR} = 5 V ± 10 %		10	50	μA
V_{DD} rise, fall time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ setup time to V_{DD}	t_{SSTVD}		12T[Note] + 0.5			μs
$\overline{STOP}$ hold time to V_{DD}	t_{HVDST}		12T[Note] + 0.5			μs

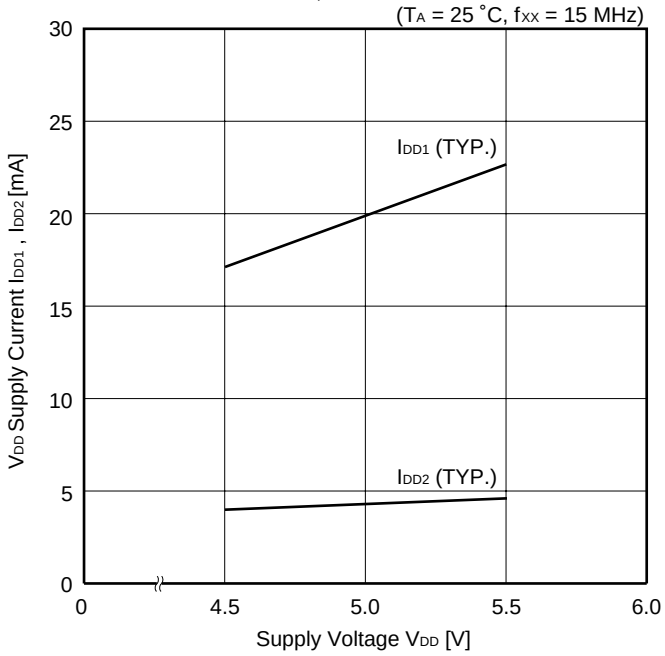
Note T = t_{CYC} = 1/f_{xx}

Data Retention Timing

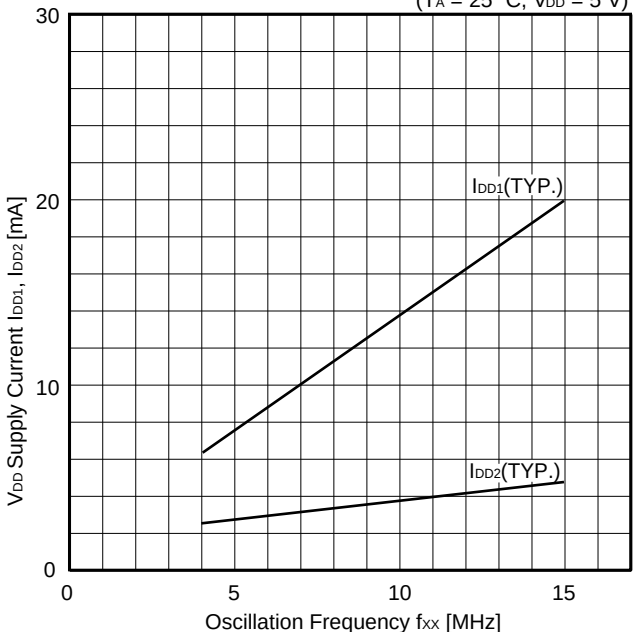


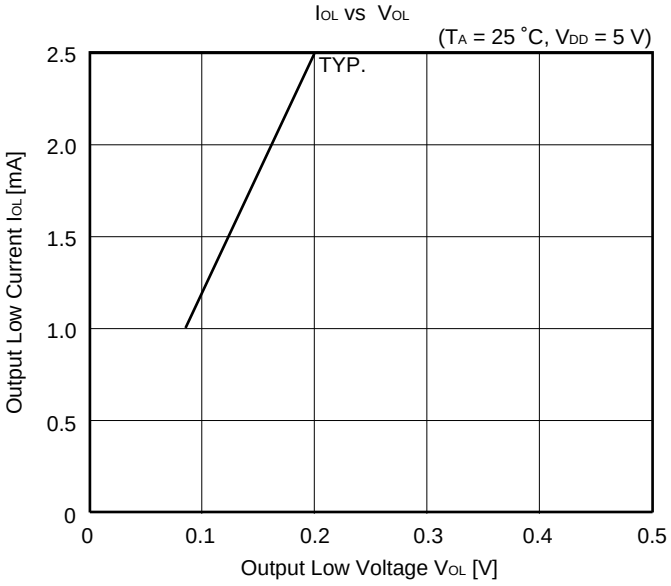
6. CHARACTERISTIC CURVES (reference value)

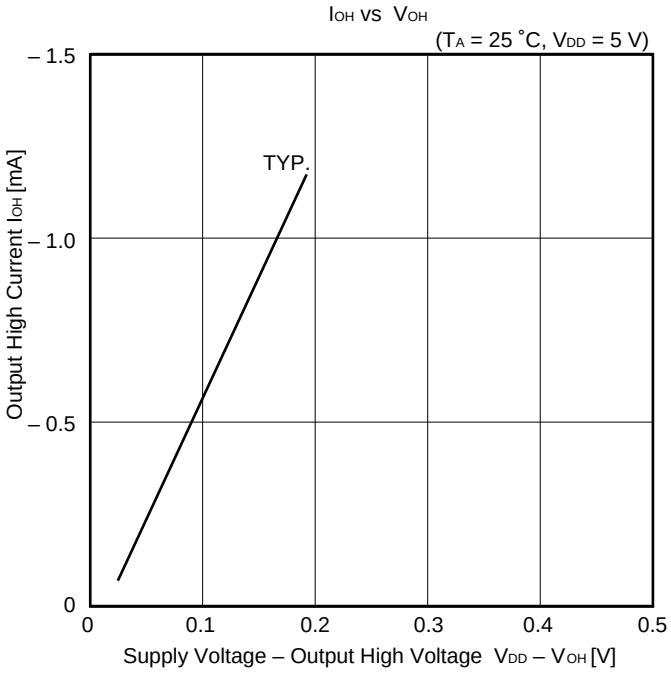
I_{DD1}, I_{DD2} vs V_{DD}
(T_A = 25 ˚C, f_{XX} = 15 MHz)

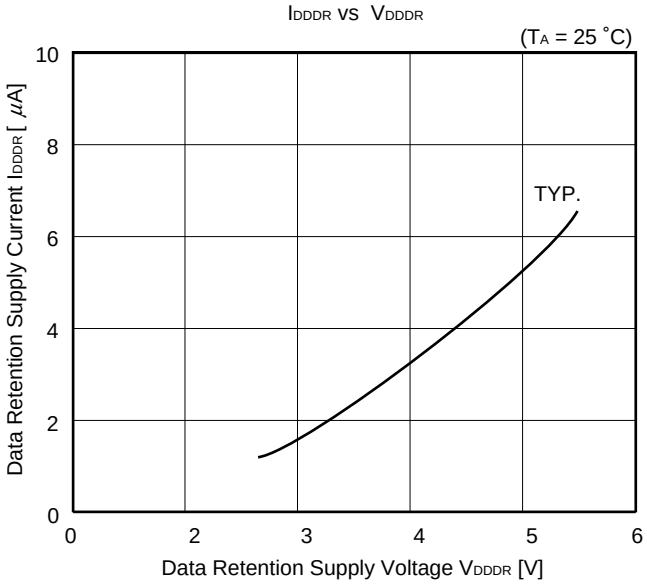


I_{DD1}, I_{DD2} vs f_{XX}
(T_A = 25 ˚C, V_{DD} = 5 V)



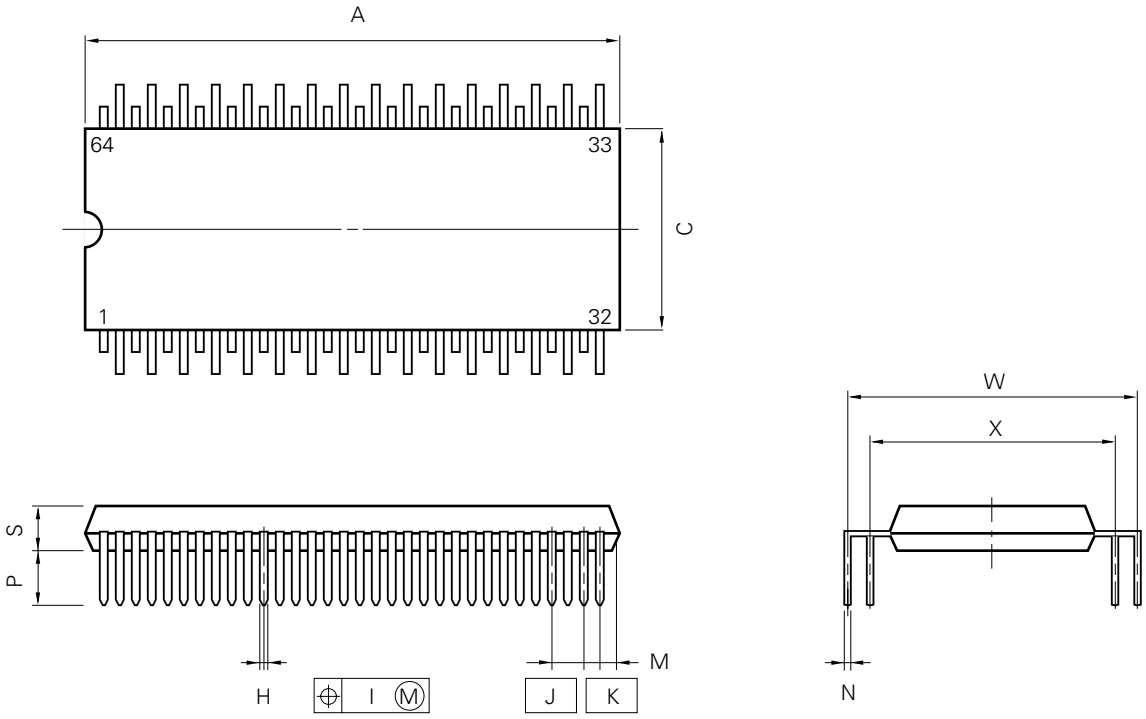

IOL vs VOL
(TA = 25 ˚C, VDD = 5 V)
TYP.
Output Low Current IOL [mA]
2.5
2.0
1.5
1.0
0.5
0
0
0.1
0.2
0.3
0.4
0.5
Output Low Voltage VOL [V]


IOH vs VOH
(TA = 25 ˚C, VDD = 5 V)
TYP.
Output High Current IOH [mA]
– 1.5
– 1.0
– 0.5
0
0
0.1
0.2
0.3
0.4
0.5
Supply Voltage – Output High Voltage VDD – VOH [V]


IDDDR vs VDDDR
(TA = 25 ˚C)
Data Retention Supply Current IDDDR [μA]
10
8
6
4
2
0
TYP.
0
2
3
4
5
6
Data Retention Supply Voltage VDDDR [V]

7. PACKAGE DRAWINGS

64 PIN PLASTIC QUIP



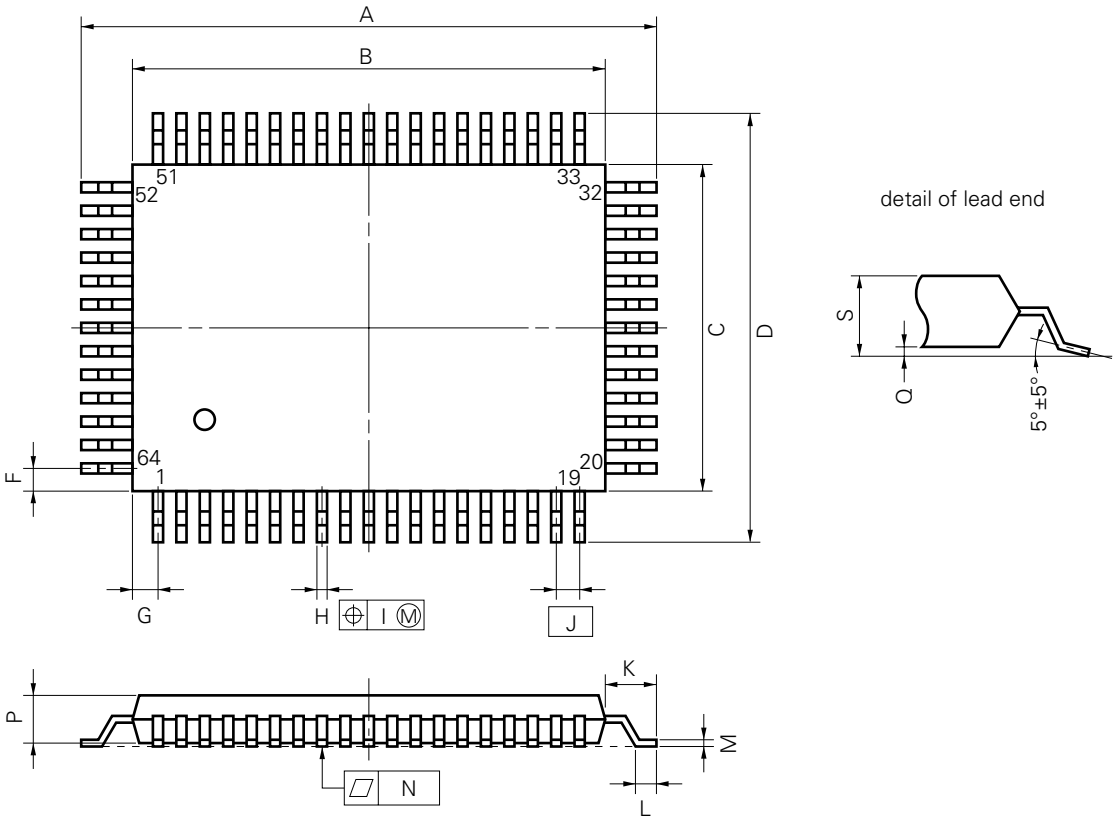
P64GQ-100-36

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm1.05}$	$0.950^{\pm0.042}$
X	$19.05^{\pm1.05}$	$0.750^{\pm0.042}$

64 PIN PLASTIC QFP (14×20)



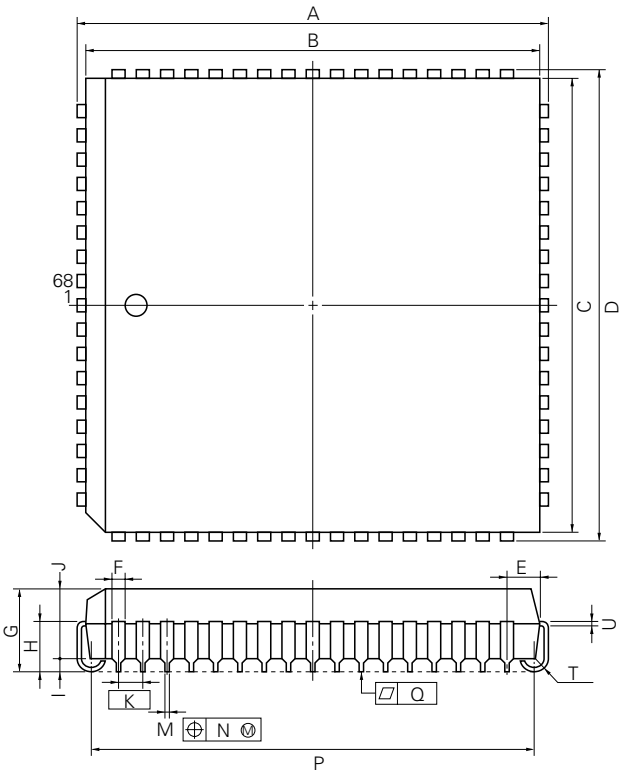
P64GF-100-3B8,3BE,3BR-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

68 PIN PLASTIC QFJ (□950 mil)



P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

8. RECOMMENDED SOLDERING CONDITIONS *

Solder the μPD78C14(A) under the recommended conditions listed below.

For details of the recommended conditions for soldering, please refer to **Semiconductor Device Mounting Technology Manual (IEI-1207)**.

Consult an NEC sales representative about soldering methods and soldering conditions other than listed below.

Table 8-1. Soldering Conditions for Surface Mount Type

(1) μPD78C14GF(A)-xxx-3BE: 64-pin plastic QFP (14 x 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 ˚C, Time: Within 30 s (at 210 ˚C or higher), Count: Twice or less <Attention> (1) Perform the second reflow when the device temperature has come down to the room temperature from the heating from the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 ˚C, Time: Within 40 s (at 200 ˚C or higher), Count: Twice or less <Attention> (1) Perform the second reflow when the device temperature has come down to the room temperature from the heating from the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	VP15-00-2
Wave soldering	Soldering bath temperature: 260 ˚C or less, Time: Within 10 s, Count: Once, Preheating temperature: 120 ˚C MAX. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 ˚C or less, Time: Within 3 s (per pin row)	—

Caution Do not use several soldering methods together (except partial heating).

(2) μPD78C14L (A)-xxx: 68-pin plastic QFJ (950 x 950 mil)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 ˚C, Time: Within 30 s (at 210 ˚C or higher), Count: Once, Maximum number of days: Seven Note (after seven days, prebaking at 125 ˚C is required for 10 hours)	IR30-107-1
VPS	Package peak temperature: 215 ˚C, Time: Within 40 s (at 200 ˚C or higher), Count: Once, Maximum number of days: Seven Note (after seven days, prebaking at 125 ˚C is required for 10 hours)	VP15-107-1
Partial heating	Pin temperature: 300 ˚C or less, Time: Within 3 s (per pin row)	—

Note Number of storage days under the storage conditions of 25 ˚C and 65 % RH or less after the dry pack is opened.

Caution Do not use several soldering methods together (except partial heating).

Table 8-2. Soldering Conditions for Hole-Through Type

μPD78C14G(A)-xxx-36: 64-pin plastic QUIP

Soldering Method	Soldering Conditions
Wave Soldering (pin part only)	Soldering bath temperature: 260 °C or less, Time: Within 10 s
Partial heating	Pin temperature: 300 °C or less, Time: Within 3 s (per pin row)

Caution Apply wave soldering only to pins and be careful not to bring solder directly in contact with the package.

APPENDIX DEVELOPMENT TOOLS *

The following development tools are provided for system development using the μPD78C14(A):

Language processor

87AD series relocatable assembler (RA87)	This relocatable assembler is a program which converts a program written in mnemonics into object code that can be executed by microcontroller. In addition, it contains the automatic function of symbol table generation and branch instruction optimization processing.			
	Host machine			Ordering code (product name)
		OS	Distribution media	
	PC-9800 series	MS-DOS™ (Ver. 2.11 to Ver. 5.00A Note)	3.5-inch 2HD	μS5A13RA87
			5-inch 2HD	μS5A10RA87
	IBM PC/AT™	PC DOS™ (Ver. 3.1)	3.5-inch 2HC	μS7B13RA87
			5-inch 2HC	μS7B10RA87

PROM write tools

Hard-ware	PG-1500	PG-1500 is a PROM programmer which enables you to program single chip microcontrollers containing PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256 Kbits to 4 Mbits.		
	PA-78CP14GQ	PROM programmer adapter for the μPD78CP14(A) and connected to PG-1500 for use.		
Soft-ware	PG-1500 controller	PG-1500 and a host machine are connected by a serial or parallel interface and PG-1500 is controlled on the host machine.		
		Host machine		Ordering code (product name)
		OS	Distribution media	
		PC-9800 series	MS-DOS (Ver. 2.11 to Ver. 5.00A Note)	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT	PC DOS (Ver. 3.1)	3.5-inch 2HD	μS7B13PG1500
				5-inch 2HC	μS7B10PG1500

Note Ver. 5.00/500A have task swap function. However, this function is not supported by this software.

Remark Operations of the assembler and PG-1500 controller are guaranteed only on the host machines under the operating systems listed above.

Debugging tools

In-circuit emulator (IE-78C11-M) is provided for μPD78C14(A) program debugging tools. The system configuration is listed below:

<table>
<tr><td>Hard-
ware</td><td>IE-78C11-M</td><td colspan="4">IE-78C11-M is an in-circuit emulator for the 87AD series.
IE-78C11-M can be connected to a host machine efficient debugging.</td></tr>
<tr><td rowspan="5">Soft-
ware</td><td rowspan="5">IE-78C11-M
control program
(IE controller)</td><td colspan="4">IE-78C11-M and a host machine are connected by RS-232-C and IE-78C11-M is controlled on the host machine.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td rowspan="2">Ordering code
(product name)</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td>MS-DOS
(Ver. 2.11 to Ver. 3.30D)</td><td>3.5-inch 2HD</td><td>μS5A13IE78C11</td></tr>
<tr><td>PC-9800 series</td><td>MS-DOS
(Ver. 2.11 to Ver. 3.30D)</td><td>5-inch 2HD</td><td>μS5A10IE78C11</td></tr>
<tr><td>IBM PC/AT</td><td>PC DOS
(Ver. 3.1)</td><td>5-inch 2HC</td><td>μS7B10IE78C11</td></tr>
</table>

Remark Operation of IE controller is guaranteed only on the host machine under the operating systems listed above.

NOTES FOR CMOS DEVICES

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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