DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
μPD78F4046

16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F4046 is a product of the μPD784046 Subseries in the 78K/IV Series.

The μPD78F4046 has flash memory in place of the internal ROM of the μPD784046. The incorporation of flash memory allows a program to be written or erased while mounted on the target board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784046 Subseries User's Manual	**Hardware:**	**U11515E**
78K/IV Series User's Manual	**Instruction:**	**U10905E**

FEATURES

- 78K/IV Series
- Pin compatible with μPD784044, 784046 (except V_{PP} pin)
- Flash memory: 64 KB
- Internal RAM: 2048 bytes
- Operable with the same supply voltage as that of the mask ROM version: V_{DD} = 4.5 to 5.5 V

APPLICATIONS

- Water heaters, vending machines, etc.
- FA fields such as robots, automated machine tools, etc.

ORDERING INFORMATION

Part Number	Package
μPD78F4046GC-3B9	80-pin plastic QFP (14 × 14 mm)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

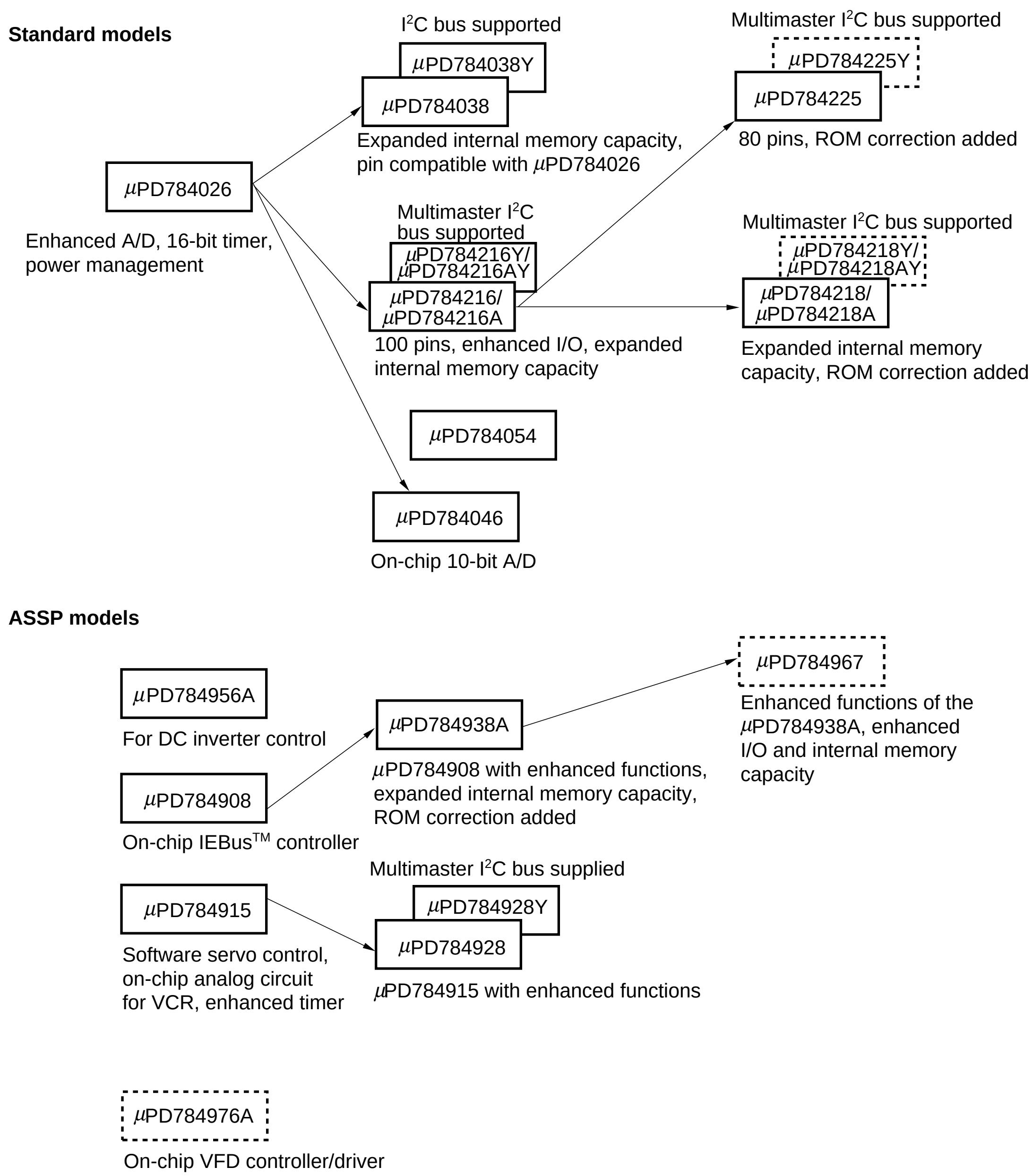
Document No. U11447EJ2V0DS00 (2nd edition)
Date Published August 2000 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

78K/IV SERIES LINEUP

[ ] : Products in mass production

[- - -] : Products under development



OVERVIEW OF FUNCTIONS

Item		Function
Number of basic instructions (mnemonics)		113
General-purpose registers		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)
Minimum instruction execution time		125 ns (@16 MHz operation with internal clock)
Internal memory	Flash memory	64 KB
	RAM	2048 bytes
Memory space		1 MB with program/data combined
I/O ports	Total	65
	Input	17
	I/O	48
Pins with ancillary functions[Note]	Pins with pull-up resistors	29
Real-time output port		4 bits × 1
Timers		Timer 0: (16 bits) Timer counter × 1 Capture/compare register × 4 Pulse output • Toggle output • Set/reset output
		Timer 1: (16 bits) Timer counter × 1 Compare register × 2 Pulse output • Toggle output • Set/reset output
		Timer/event counter 2: (16 bits) Timer counter × 1 Compare register × 2 Pulse output • Toggle output • PWM/PPG output
		Timer/event counter 3: (16 bits) Timer counter × 1 Compare register × 2 Pulse output • Toggle output • PWM/PPG output
		Timer 4: (16 bits) Timer counter × 1 Compare register × 2 Pulse output • Real-time output (4 bits × 1)
A/D converter		10-bit resolution × 16 channels
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (with baud rate generator)
Watchdog timer		1 channel
Interrupts	Sources	27 (internal: 23, external: 8 (internal/external: 4)) + BRK instruction
	Software	BRK instruction
	Non-maskable	Internal: 1, external: 1
	Maskable	Internal: 22, external: 7 (internal/external: 4)
		• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching
Bus sizing		8-bit/16-bit external data bus width selectable
Standby		HALT/STOP/IDLE modes
Supply voltage		V_{DD} = 4.5 to 5.5 V
Package		80-pin plastic QFP (14 × 14 mm)

Note The pins with ancillary functions are included in the I/O pins.

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1. DIFFERENCES AMONG μPD784046 SUBSERIES

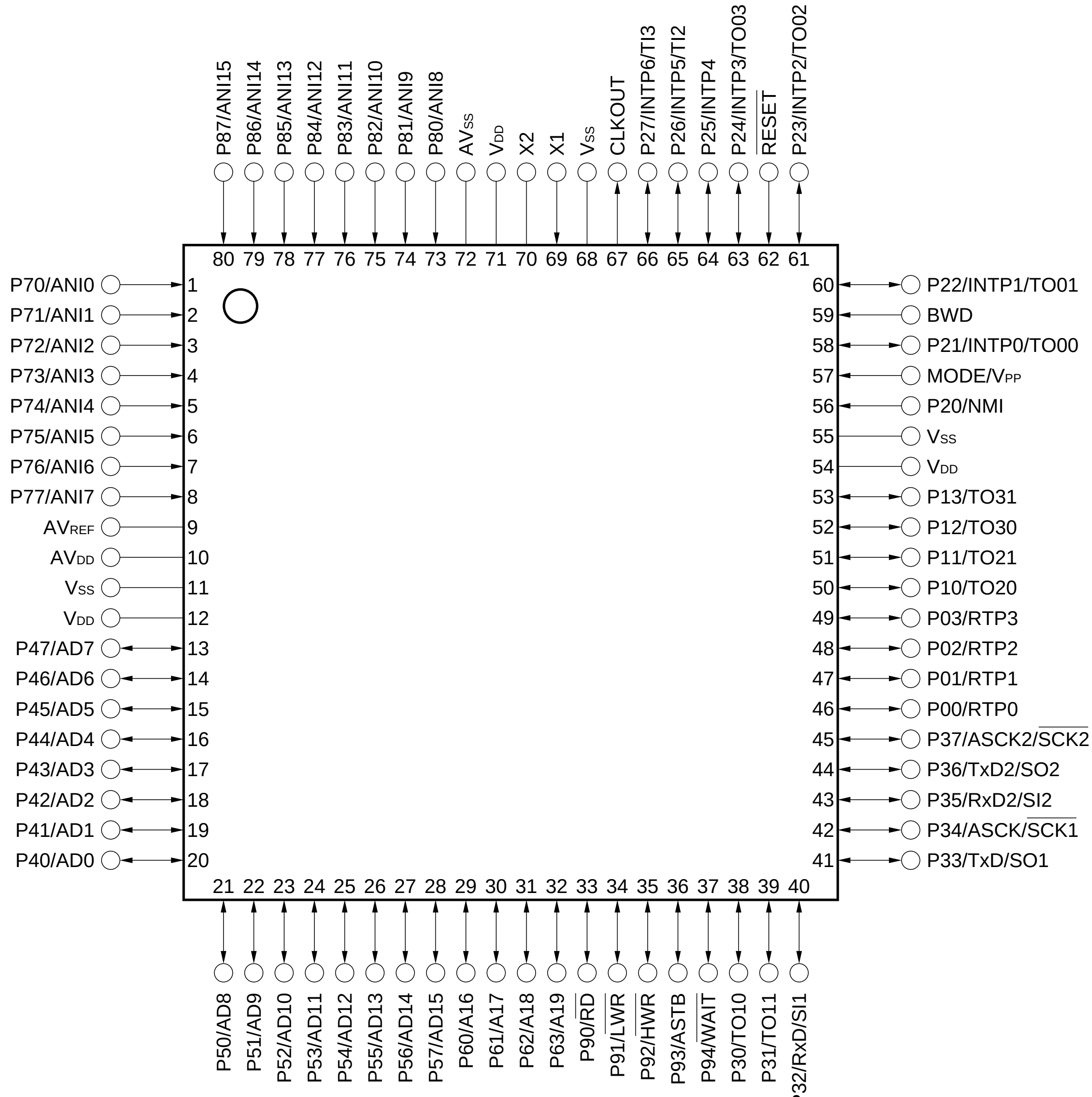
The only difference between the μPD784044 and μPD784046 is the internal memory capacity.
The μPD78F4046 is a version of the μPD784046 with the internal ROM replaced by flash memory.
The differences are shown in Table 1-1.

Table 1-1. Differences Among μPD784046 Subseries

Item \ Part Number	μPD784044	μPD784046	μPD78F4046
Internal ROM	32 KB (mask ROM)	64 KB (mask ROM)	64 KB (flash memory)
Internal RAM	1024 bytes	2048 bytes	
Function of pin 57	MODE		MODE/V_{PP}

2. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD78F4046GC-3B9

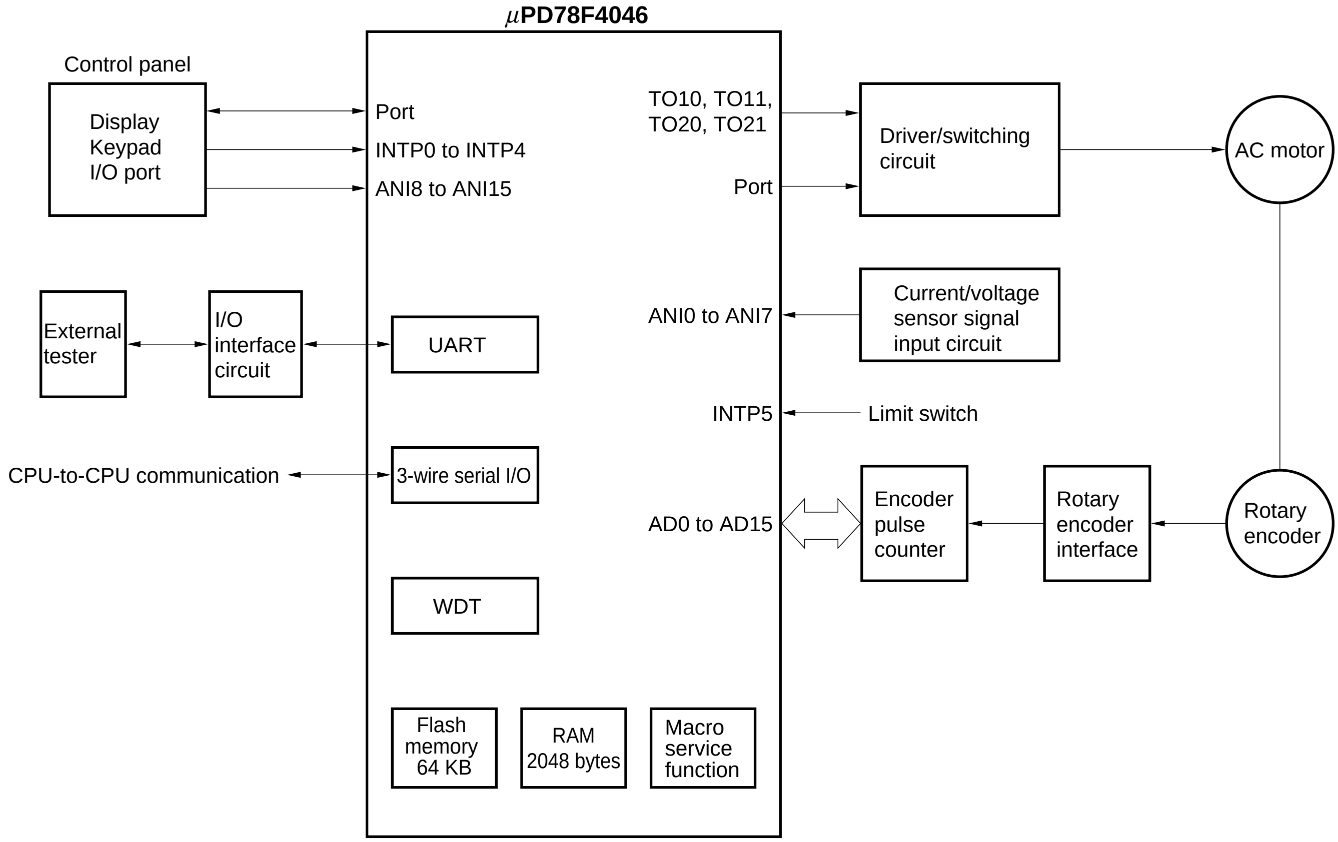


Caution Connect the MODE/V_{PP} pin directly to V_{SS} in normal operation mode.

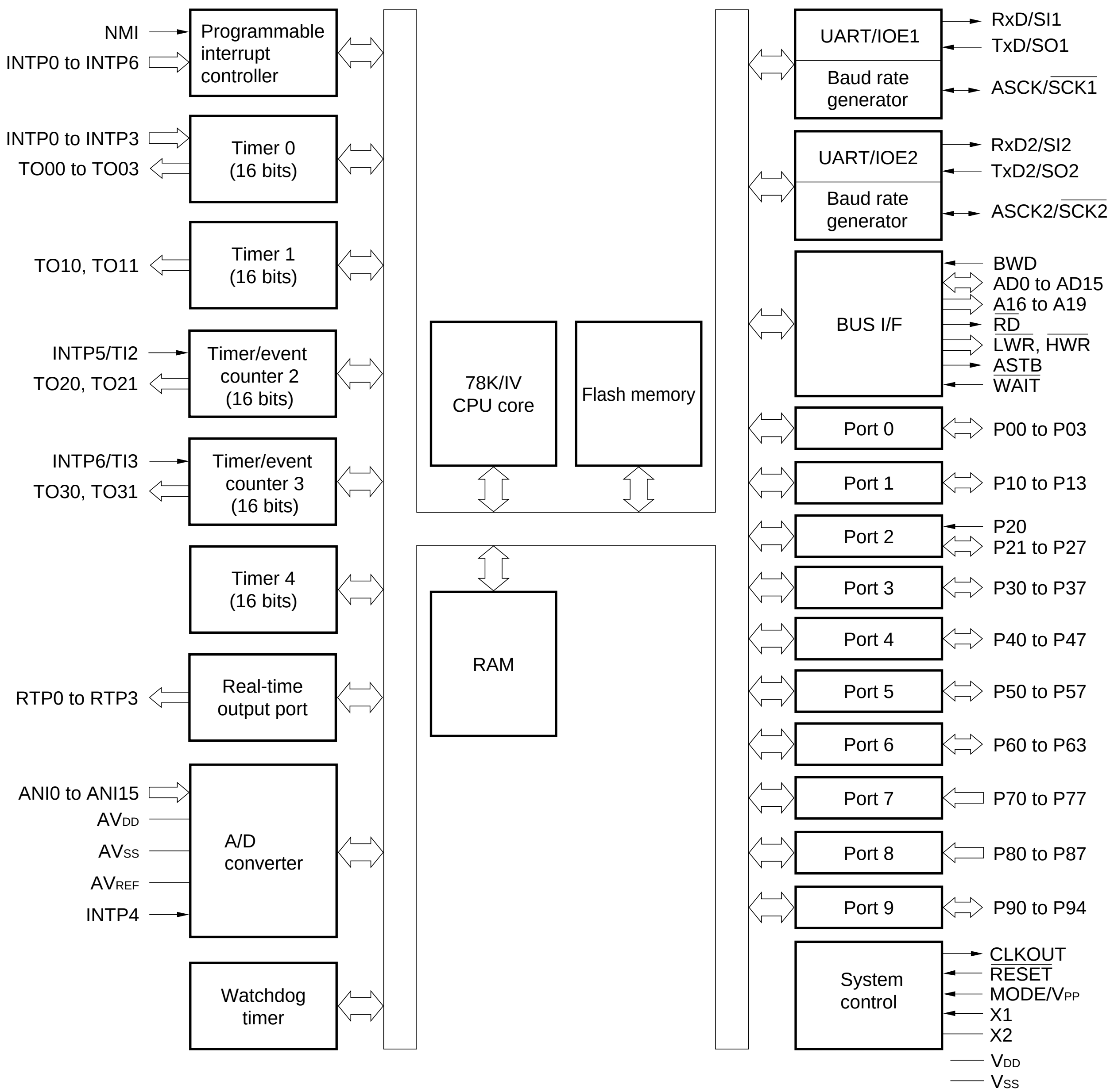
P00 to P03:	Port 0
P10 to P13:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P63:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P94:	Port 9
RTP0 to RTP3:	Real-Time Port
NMI:	Nonmaskable Interrupt
INTP0 to INTP6:	Interrupt from Peripherals
TO00 to TO03, TO10, TO11: TO20, TO21, TO30, TO31:	Timer Output
TI2, TI3:	Timer Input
RxD, RxD2:	Receive Data
TxD, TxD2:	Transmit Data
ASCK, ASCK2:	Asynchronous Serial Clock
SI1, SI2,:	Serial Input
SO1, SO2:	Serial Output
$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$:	Serial Clock

AD0 to AD15:	Address/Data Bus
A16 to A19:	Address Bus
$\overline{\text{RD}}$:	Read Strobe
$\overline{\text{LWR}}$:	Low Address Write Strobe
$\overline{\text{HWR}}$:	High Address Write Strobe
ASTB:	Address Strobe
$\overline{\text{WAIT}}$:	Wait
BWD:	Bus Width Definition
MODE:	Mode
CLKOUT:	Clock Out
X1, X2:	Crystal
$\overline{\text{RESET}}$:	Reset
ANI0 to ANI15:	Analog Input
AV_{REF}:	Analog Reference Voltage
AV_{DD}:	Analog Power Supply
AV_{SS}:	Analog Ground
V_{DD}:	Power Supply
V_{PP}:	Programming Power Supply
V_{SS}:	Ground

3. SYSTEM CONFIGURATION EXAMPLE (AC SERVO MOTOR CONTROL)



4. BLOCK DIAGRAM



5. PIN FUNCTIONS

5.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	
P00 to P03	I/O	RTP0 to RTP3	Port 0 (P0): • 4-bit I/O port • Input/output can be specified in 1-bit units. • When used as an input port, an on-chip pull-up resistor can be specified by means of software.	
P10	I/O	TO20	Port 1 (P1): • 4-bit I/O port • Input/output can be specified in 1-bit units.	
P11		TO21		
P12		TO30		
P13		TO31		
P20	Input	NMI	Port 2 (P2): • 8-bit I/O port	Input only
P21	I/O	INTP0/TO00		Input/output can be specified in 1-bit units.
P22		INTP1/TO01		
P23		INTP2/TO02		
P24		INTP3/TO03		
P25		INTP4		
P26		INTP5/TI2		
P27		INTP6/TI3		
P30	I/O	TO10	Port 3 (P3): • 8-bit I/O port • Input/output can be specified in 1-bit units.	
P31		TO11		
P32		RxD/SI1		
P33		TxD/SO1		
P34		ASCK/$\overline{SCK1}$		
P35		RxD2/SI2		
P36		TxD2/SO2		
P37		ASCK2/$\overline{SCK2}$		
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Input/output can be specified in 1-bit units. • When used as an input port, an on-chip pull-up resistor can be specified by means of software.	
P50 to P57	I/O	AD8 to AD15	Port 5 (P5): • 8-bit I/O port • Input/output can be specified in 1-bit units. • When used as an input port, an on-chip pull-up resistor can be specified by means of software.	
P60 to P63	I/O	A16 to A19	Port 6 (P6): • 4-bit I/O port • Input/output can be specified in 1-bit units. • When used as an input port, an on-chip pull-up resistor can be specified by means of software.	

5.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P70 to P77	Input	ANI0 to ANI7	Port 7 (P7): • 8-bit input-only port
P80 to P87	Input	ANI8 to ANI15	Port 8 (P8): • 8-bit input-only port
P90	I/O	$\overline{RD}$	Port 9 (P9): • 5-bit I/O port • Input/output can be specified in 1-bit units. • When used as an input port, an on-chip pull-up resistor can be specified by means of software.
P91		$\overline{LWR}$	
P92		$\overline{HWR}$	
P93		ASTB	
P94		$\overline{WAIT}$	

5.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	
RTP0 to RTP3	Output	P00 to P03	Real-time output	
NMI	Input	P20	Non-maskable interrupt request input	
INTP0		P21/TO00	External interrupt request input	Capture trigger signal of CC00
INTP1		P22/TO01		Capture trigger signal of CC01
INTP2		P23/TO02		Capture trigger signal of CC02
INTP3		P24/TO03		Capture trigger signal of CC03
INTP4		P25		Conversion start trigger input of A/D converter
INTP5		P26/TI2		–
INTP6		P27/TI3		
TO00	Output	P21/INTP0	Timer output from timer	
TO01		P22/INTP1		
TO02		P23/INTP2		
TO03		P24/INTP3		
TO10		P30		
TO11		P31		
TO20		P10		
TO21		P11		
TO30		P12		
TO31		P13		
TI2	Input	P26/INTP5	External count clock input to timer/event counter 2	
TI3		P27/INTP6	External count clock input to timer/event counter 3	
RxD		P32/SI1	Serial data input (UART0)	
RxD2		P35/SI2	Serial data input (UART2)	
TxD	Output	P33/SO1	Serial data output (UART0)	
TxD2		P36/SO2	Serial data output (UART2)	
ASCK	Input	P34/$\overline{SCK1}$	Baud rate clock input (UART0)	
ASCK2		P37/$\overline{SCK2}$	Baud rate clock input (UART2)	
SI1		P32/RxD	Serial data input (3-wire serial I/O1)	
SI2		P35/RxD2	Serial data input (3-wire serial I/O2)	
SO1	Output	P33/TxD	Serial data output (3-wire serial I/O1)	
SO2		P36/TxD2	Serial data output (3-wire serial I/O2)	
$\overline{SCK1}$	I/O	P34/ASCK	Serial clock input/output (3-wire serial I/O1)	
$\overline{SCK2}$		P37/ASCK2	Serial clock input/output (3-wire serial I/O2)	
AD0 to AD7		P40 to P47	Lower multiplexed address/data bus for expanding memory externally	
AD8 to AD15[Note]		P50 to P57	• When 8-bit bus is specified Higher address bus for expanding memory externally • When external 16-bit bus is specified Higher multiplexed address/data bus for expanding memory externally	
A16 to A19[Note]	Output	P60 to P63	Higher address bus for expanding memory externally	
$\overline{RD}$		P90	Read strobe to external memory	

Note The number of pins used as address bus pins differs depending on the external address space.

5.2 Non-Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
$\overline{LWR}$	Output	P91	• When external 8-bit bus is specified Write strobe to external memory • When external 16-bit bus is specified Write strobe to external memory located at lower address
$\overline{HWR}$		P92	Write strobe to external memory located at higher address when external 16-bit bus is specified
ASTB	Output	P93	Timing signal output that externally latches address information output from AD0 through AD15 pins to access external memory
$\overline{WAIT}$	Input	P94	Wait insertion
BWD		–	Bus width setting
MODE		V_{PP}	Connect directly to V_{SS} in normal operation mode (for specification of IC test mode).
CLKOUT	Output	–	Clock output
X1	Input	–	Connecting crystal resonator for system clock oscillation (clock can be input to X1).
X2	–	–	
$\overline{RESET}$	Input	–	Chip reset
ANI0 to ANI7		P70 to P77	Analog voltage input for A/D converter
ANI8 to ANI15		P80 to P87	
AV_{REF}	–	–	Reference voltage application for A/D converter
AV_{DD}		–	Positive power supply for A/D converter
AV_{SS}		–	GND for A/D converter
V_{DD}		–	Positive power supply
V_{PP}	Input	MODE	Flash memory programming mode setting Applying high-voltage for program write/verify.
V_{SS}	–	–	GND

5.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 5-1.

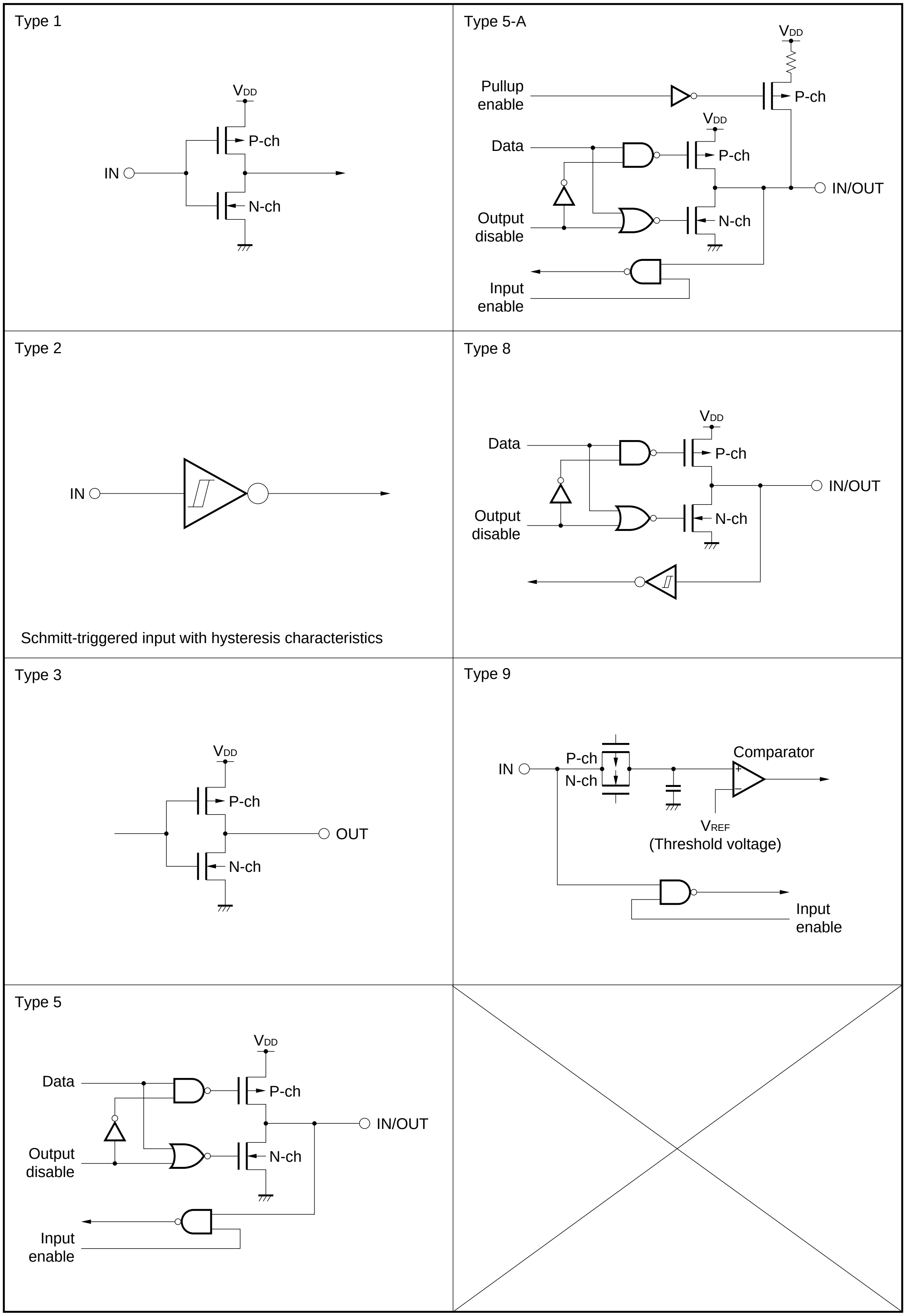
For the I/O circuit configuration of each type, refer to Figure 5-1.

Table 5-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/RTP0 to P03/RTP3	5-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P10/TO20	5		
P11/TO21			
P12/TO30			
P13/TO31			
P20/NMI	2	Input	Connect to V_{SS}.
P21/INTP0/TO00	8	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P22/INTP1/TO01			
P23/INTP2/TO02			
P24/INTP3/TO03			
P25/INTP4			
P26/INTP5/TI2			
P27/INTP6/TI3			
P30/TO10	5		
P31/TO11			
P32/RxD/SI1			
P33/TxD/SO1			
P34/ASCK/$\overline{SCK1}$	8		
P35/RxD2/SI2	5		
P36/TxD2/SO2			
P37/ASCK2/$\overline{SCK2}$	8		
P40/AD0 to P47/AD7	5-A		
P50/AD8 to P57/AD15			
P60/A16 to P63/A19			
P70/ANI0 to P77/ANI7	9	Input	Connect to V_{SS}.
P80/ANI8 to P87/ANI15			
P90/$\overline{RD}$	5-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P91/$\overline{LWR}$			
P92/$\overline{HWR}$			
P93/ASTB			
P94/$\overline{WAIT}$			
MODE	1	Input	–
$\overline{RESET}$	2		
CLKOUT	3	Output	Leave open.
AV_{REF}	–	–	Connect to V_{SS}.
AV_{SS}			
AV_{DD}			Connect to V_{DD}.

Remark Since type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 5-1. Pin I/O Circuits



6. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting this register, the internal memory of the μPD78F4046 can be mapped identically to that of a mask ROM version with a different internal memory (ROM and RAM) capacity.

IMS is set with an 8-bit memory manipulation instruction.

RESET input sets IMS to DEH.

Figure 6-1. Internal Memory Size Switching Register (IMS) Format

Address: 0FFFCH After reset: DEH R/W

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Internal ROM Capacity Selection
0	0	32 KB
0	1	64 KB
Other than above		Setting prohibited

RAM1	RAM0	Peripheral RAM Capacity Selection
0	1	768 bytes
1	0	1.5 KB
Other than above		Setting prohibited

Table 6-1 shows the IMS setting values to make the memory mapping the same as that of the mask ROM versions.

Table 6-1. Setting Values of Internal Memory Size Switching Register (IMS)

Target Mask ROM Version	IMS Setting Value
μPD784044, 784054	CDH[Note]
μPD784046	DEH

Note When IMS is set to CDH, the peripheral RAM capacity of the μPD78F4046 is 768 bytes, but that of the μPD784044 or 784054 is 512 bytes. Consequently, when making a mask ROM version, be sure not to use 0FA00H through 0FAFFH in the peripheral RAM area of μPD78F4046 (upon the execution of the LOCATION 0H instruction).

7. FLASH MEMORY PROGRAMMING

The flash memory can be written with the μPD78F4046 mounted on the target board (on-board write). Writing is performed with the dedicated flash programmer Flashpro II (part number: FL-PR2) and Flashpro III (part number: FL-PR3, PG-FP3)) connected to the host machine and the target system.

Remark Flashpro II and III are products of Naito Densei Machida Mfg. Co., Ltd..

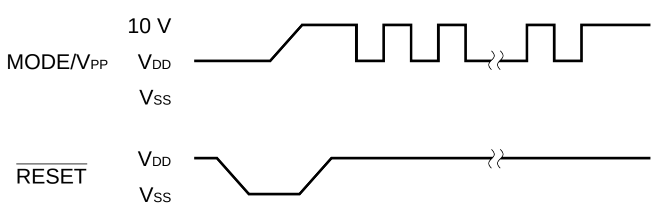
7.1 Selecting Communication Mode

Writing to flash memory is performed using the Flashpro II and III via a serial communication mode. Select a serial communication mode from those listed in Table 7-1. The selection of the communication mode is made by using the format shown in Figure 7-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 7-1.

Table 7-1. List of Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O	2	P34/ASCK/$\overline{SCK1}$ P33/TxD/SO1 P32/RxD/SI1	0
		P37/ASCK2/$\overline{SCK2}$ P36/TxD2/SO2 P35/RxD2/SI2	1
UART	2	P33/TxD/SO1 P32/RxD/SI1	8
		P36/TxD2/SO2 P35/RxD2/SI2	9

Figure 7-1. Format of Communication Mode Selection



7.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 7-2 shows the major functions of flash memory programming.

Table 7-2. Major Functions of Flash Memory Programming

Function	Description
Batch erase	Erases the entire memory contents.
Block erase	Erases the contents of the specified memory block, with one memory block consisting of 16 KB.
Batch blank check	Checks the erasure status of the entire memory.
Block blank check	Checks the erasure status of the specified block.
Data write	Writes to the flash memory based on the write start address and the amount of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.
Block verify	Compares the contents of the specified memory block with the input data.

7.3 Connection of Flashpro II and Flashpro III

The connection of the dedicated flash programmer and the μPD78F4046 differs according to the communication mode (3-wire serial I/O or UART). The connection for each communication mode is shown in Figures 7-2 and 7-3.

Figure 7-2. Connection of Flashpro II and Flashpro III in 3-Wire Serial I/O Mode

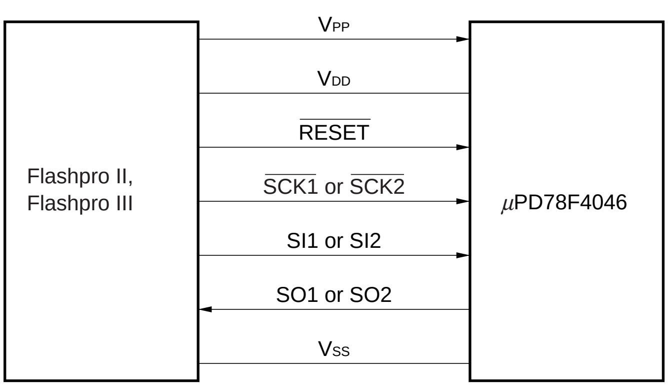
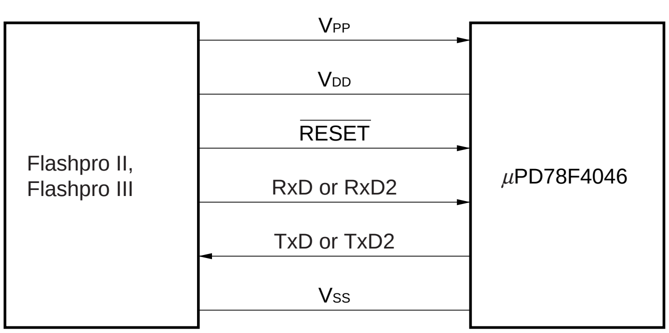


Figure 7-3. Connection of Flashpro II and Flashpro III in UART Mode



7.4 Cautions When Writing to Flash Memory

For writing data to the flash memory of the μPD78F4046, use the prewrite and ECC functions. Moreover, set the flash programmer as follows when writing to flash memory using these functions. Either 1-bit or 8-bit memory manipulation instructions can be used to make these settings.

(1) Using prewrite function

To improve flash memory rewrite characteristics, prewriting is necessary before erasing. Prewriting involves writing 00H to all the data. This is performed to delete the bits that are already 1 in the data (erasure state), and to prevent further erasure stress.

(2) Using ECC function

When writing to the μPD78F4046 and shipping it as a product, ECC data needs to be written in the ECC data area of flash memory. By writing ECC data and setting the ECC function, data writing can be performed correctly.

<1> Creating ECC data

Convert the EX file to an ECC-attached HEX file using the ECC generator included in the assembly package (Ver. 1.20 or later for PC). Download this ECC-attached HEX file to the flash programmer, and then write.

[ECC data creating method]

- Prepare the HEX file created by the object converter of the assembly package.
- Convert it to the program data + HEX file using the ECC generator (ECCGEN.EXE) included in the assembly package.

Example Convert the file “file.hex” to “file_ec.hex”.
ec file.hex-ofile_ec.hex -a0ffffh, 10000h, 14000h, 14004h

<2> Flash programmer (Flashpro II, Flashpro III) setting and writing

Prewriting and ECC writing are performed by Flashpro II and Flashpro III. The setting method when using an earlier version than Flashpro II Ver. 2.50 is described below.

Remark If using Flashpro II Ver. 2.50 or later or Flashpro III (PG-FP3 (Ver. 3.040 or later, products of NEC Corporation)), setting is not necessary. Setting is performed automatically by reading parameter files.

[When earlier version than Flashpro II Ver. 2.50 is used]

a. Connect the PC and FL-PR2, then start up the control software “flashpro.exex”.

Prewrite setting:

b. Press the CTRL + GRPH (ART) + P keys at the same time.
c. Check the check box of Pre-Write set. □→☒
d. Press the OK button.

ECC write setting:

e. Select Setting.
f. Select Option.
g. Check the ECC code area in the menu window.
h. Input 14004 to ECC END ADDRESS
i. Press the OK button.
j. Press the TYPE button.
k. Input 14004 to END ADDRESS
l. Press the OK button

[Writing method]

a. Download the ECC-attached HEX file to the flash programmer.
b. Set to chip mode and write using the E.P.V button.

Do not use the Program command, since this will disable writing to ECC.

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		–0.5 to V_{DD} + 0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1**	–0.5 to V_{DD} + 0.5 ≤ 7.0	V
	V_{I2}	TEST/V_{PP} pin in the programming mode	–0.5 to +11.0	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Output current, low	I_{OL}	All output pins	15	mA
		Total of all output pins	150	mA
Output current, high	I_{OH}	All output pins	–10	mA
		Total of all output pins	–100	mA
Analog input voltage	V_{IAN}	**Note 2** $AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
		$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	
A/D converter reference input voltage	AV_{REF}	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.5	V
		$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–40 to +125	°C

Notes 1. Pins other than the pins specified in Note 2.

2. Pins P70/ANI0 to P77/ANI7, P80/ANI8 to P87/ANI15

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that the absolute maximum ratings are not exceeded.**

Recommended Operating Conditions

Oscillation Frequency	T_A	V_{DD}
8 MHz ≤ f_{XX} ≤ 32 MHz	–10 to +70°C	4.5 to 5.5 V

Capacitance (T_A = 25°C, V_{SS} = V_{DD} = 0 V)

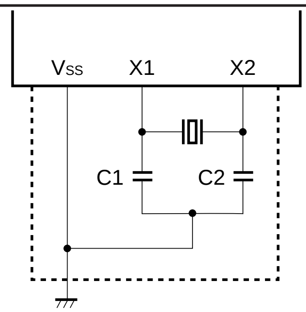
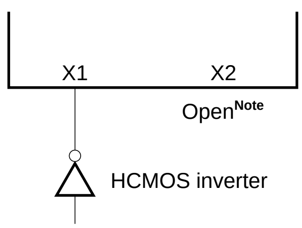
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V.			10	pF
I/O capacitance	C_{IO}				10	pF

★ Flash Memory Specifications (T_A = +10 to +40°C (rewriting), T_A = –10 to +70°C (other than rewriting))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} supply voltage	V_{DD}		4.5		5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP} high-voltage detection	9.7	10.0	10.3	V
Number of rewrites[Note]			10			Times

Note If the number of flash memory rewrites exceeds 10, operation is not guaranteed.

Oscillator Characteristics (T_A = –10 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_{XX})	8	32	MHz
External clock		X1 input frequency (f_X)	8	32	MHz
		X1 input rise/fall time	0	5	ns
		X1 input high-/low-level width	20	105	ns

Note When the EXTC bit of the oscillation stabilization time specification register (OSTS) = 0. Input the reverse phase clock of pin X1 to pin X2 when the EXTC bit = 1.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –10 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL}			0		0.8	V
Input voltage, high	V_{IH1}	**Note 1**		2.2		V_{DD}	V
	V_{IH2}	**Note 2**		0.8V_{DD}		V_{DD}	
Output voltage, low	V_{OL}	I_{OL} = 2.0 mA				0.45	V
Output voltage, high	V_{OH}	I_{OH} = –400 μA		V_{DD} – 1.0			V
Input leakage current	I_{LI}	**Note 3**	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	**Note 4**	0 V ≤ V_I ≤ AV_{DD}			±1	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode (f_{XX} = 32 MHz)			50	80	mA
	I_{DD2}	HALT mode (f_{XX} = 32 MHz)			30	60	mA
	I_{DD3}	IDLE mode (f_{XX} = 32 MHz)			10	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	15	μA
			V_{DDDR} = 5 V ±10%		15	50	μA
Pull-up resistor	R_L			15	40	80	kΩ

Notes 1. Pins other than the pins specified in Note 2

2. P20/NMI, P21/INTP0/TO00, P22/INTP1/TO01, P23/INTP2/TO02, P24/INTP3/TO03, P25/INTP4, P26/INTP5/TI2, P27/INTP6/TI3, P34/ASCK/$\overline{\text{SCK1}}$, P37/ASCK2/$\overline{\text{SCK2}}$, X1, X2, $\overline{\text{RESET}}$

3. Input and I/O pins (except X1 and X2, and P70/ANI0 to P77/ANI7, P80/ANI8 to P87/ANI15 used as analog inputs)

4. Pins P70/ANI0 to P77/ANI7, P80/ANI8 to P87/ANI15 (pins used as analog inputs, and only during a non-sampling operation)

AC Characteristics (T_A = –10 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Read/write operation

Parameter	Symbol	Expression	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		62.5	250	ns
Address setup time (to ASTB↓)	t_{SAST}	(0.5 + a) T – 20	11.2		ns
Address hold time (from ASTB↓)	t_{HSTA}	0.5T – 20	11.2		ns
ASTB high-level width	t_{WSTH}	(0.5 + a) T – 17	14.2		ns
$\overline{RD}$↓ delay time from address	t_{DAR}	(1 + a) T – 15	47.5		ns
Address float time from $\overline{RD}$↓	t_{FRA}			0	ns
Data input time from address	t_{DAID}	(2.5 + a + n) T – 56		100.2	ns
Data input time from $\overline{RD}$↓	t_{DRID}	(1.5 + n) T – 48		45.7	ns
Delay time from ASTB↓ to $\overline{RD}$↓	t_{DSTR}	0.5T – 16	15.3		ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0		ns
Address active time from $\overline{RD}$↑	t_{DRA}	0.5T – 14	17.2		ns
$\overline{RD}$ low-level width	t_{WRL}	(1.5 + n) T – 30	63.7		ns
Delay time from address to $\overline{LWR}$, $\overline{HWR}$↓	t_{DAW}	(1 + a) T – 15	47.5		ns
Data output time from $\overline{LWR}$, $\overline{HWR}$↓	t_{DWOD}			15	ns
Delay time from ASTB↓ to $\overline{LWR}$, $\overline{HWR}$↓	t_{DSTW}	0.5T – 16	15.3		ns
Data setup time (to $\overline{LWR}$, $\overline{HWR}$↑)	t_{SODW}	(1.5 + n) T – 25	68.7		ns
Data hold time (from $\overline{LWR}$, $\overline{HWR}$↑)	t_{HWOD}	0.5T – 14	17.2		ns
Delay time from $\overline{LWR}$, $\overline{HWR}$↑ to ASTB↑	t_{DWST}	1.5T – 15	78.8		ns
$\overline{LWR}$, $\overline{HWR}$ low-level width	t_{WWL}	(1.5 + n) T – 36	57.7		ns
$\overline{WAIT}$↓ input time from address	t_{DAWT}	(2 + a) T – 50		75	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	1.5T – 40		53.7	ns
$\overline{WAIT}$ hold time from ASTB↓	t_{HSTWT}	(1.5 + n) T + 5	98.8		ns
Delay time from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	(2.5 + n) T – 40		116.2 Note	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWT}	T – 40		22.5	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓	t_{HRWT}	(1 + n) T + 5	67.5		ns
Delay time from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	(1 + n) T – 40		85 Note	ns
$\overline{WAIT}$↓ input time from $\overline{LWR}$, $\overline{HWR}$↓	t_{DWWT}	T – 40		22.5	ns
$\overline{WAIT}$ hold time from $\overline{LWR}$, $\overline{HWR}$↓	t_{HWWT}	(1 + n) T + 5	67.5		ns
Delay time from $\overline{LWR}$, $\overline{HWR}$↓ to $\overline{WAIT}$↑	t_{DWWTH}	(1 + n) T – 40		85 Note	ns

Note Specification when an external wait is inserted

Remarks
1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is internal system clock frequency)
2. a = 1 when an address wait is inserted, otherwise 0.
3. n indicates the number of the wait cycles as specified by the external wait pin ($\overline{WAIT}$) or programmable wait control registers 1, 2 (PWC1, PWC2). ($n \geq 0$. $n \geq 1$ for t_{DSTWTH}, t_{DRWTH}, t_{DWWTH}).
4. Calculate values in the expression column with the system clock cycle time to be used because these values depend on the system clock cycle time (t_{CYK} = T). The values in the above expression column are calculated based on T = 62.5 ns.

Serial Operation (T_A = –10 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	T_{SFT}		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	500		ns
Serial clock low-level width	t_{WSKL}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	$0.5T_{SFT}$–40		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	210		ns
Serial clock high-level width	t_{WSKH}	$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ output	BRG	$0.5T_{SFT}$–40		ns
		$\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$ input	External clock	210		ns
SI1, SI2 setup time (to $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↑)	t_{SSSK}			80		ns
SI1, SI2 hold time (from $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↑)	t_{HSSK}			80		ns
Delay time from $\overline{\text{SCK1}}$, $\overline{\text{SCK2}}$↓ to SO1, SO2 output	t_{DSBSK}	R = 1 kΩ, C = 100 pF		0	150	ns

Remarks 1. T_{SFT} is a value set by software. The minimum value is $t_{CYK} \times 8$.

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

Other Operations (T_A = –10 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V)

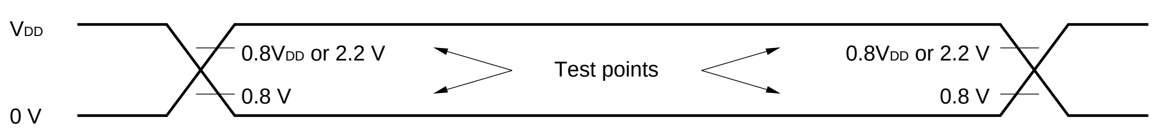
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high-/low-level width	t_{WNIH}, t_{WNIL}		10		μs
INTP0 to INTP6 high-/low-level width	t_{WITH}, t_{WITL}		4		t_{CYSMP}
TI2, TI3 high-/low-level width	t_{WTIH}, t_{WTIL}		4		t_{CYSMP}
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSH}, t_{WRSL}		10		μs

Remarks 1. t_{CYSMP} is a sampling clock set by software in the noise protection control register (NPC).
When NIn = 0, $t_{CYSMP} = t_{CYK}$
When NIn = 1, $t_{CYSMP} = t_{CYK} \times 4$

2. $t_{CYK} = 1/f_{CLK}$ (f_{CLK} is internal system clock frequency)

3. NIn: Bit n of NPC (n = 0 to 6)

AC Timing Test Points



AD Converter Characteristics (T_A = –10 to +70°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD})

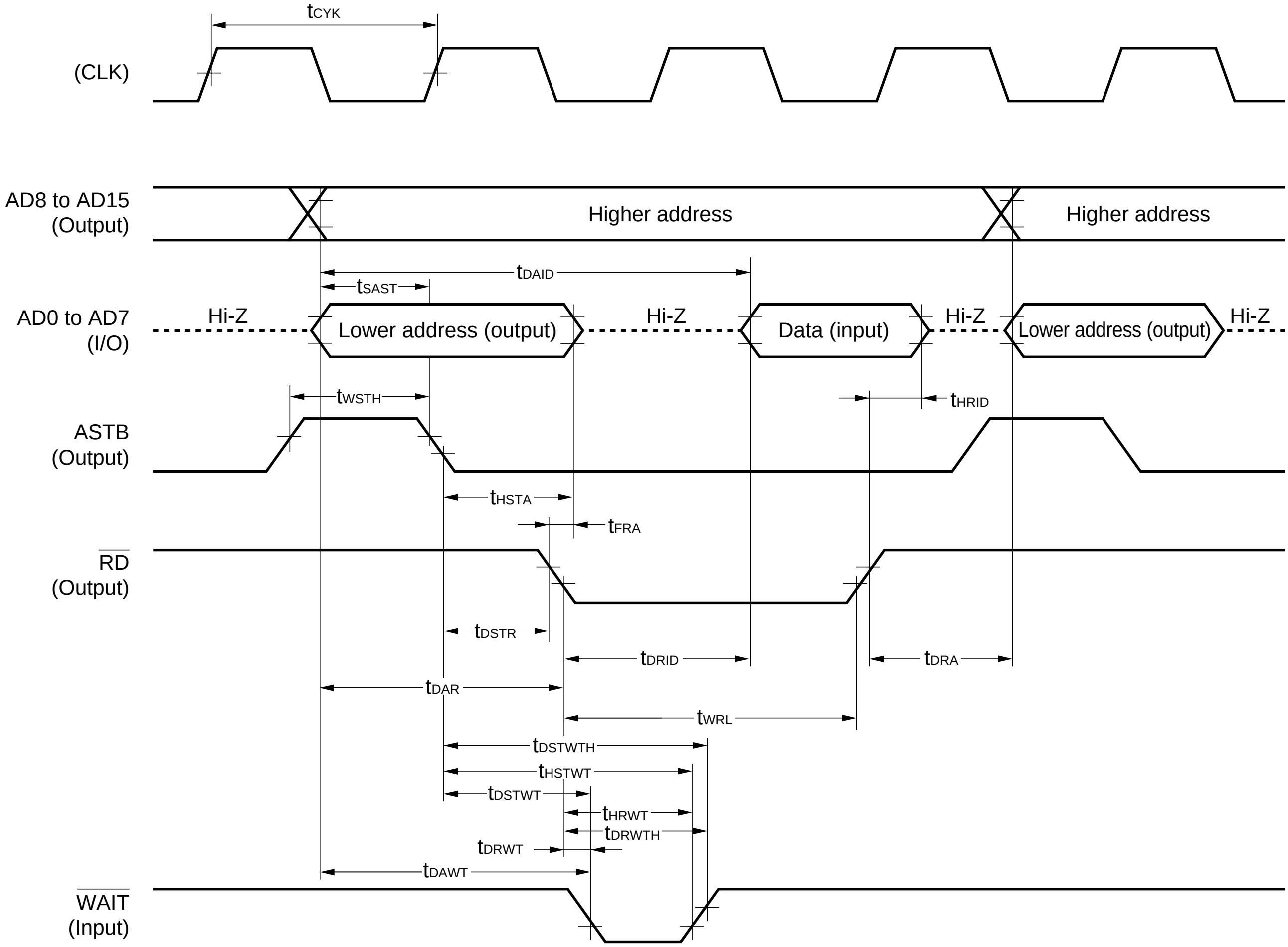
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Overall error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.5	%FSR[Note 2]
		3.4 V ≤ AV_{REF} < 4.5 V				±0.7	%FSR[Note 2]
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	80 ns ≤ t_{CYK} ≤ 250 ns		169			t_{CYK}
		62.5 ns ≤ t_{CYK} < 80 ns		208			t_{CYK}
Sampling time	t_{SAMP}	80 ns ≤ t_{CYK} ≤ 250 ns		20			t_{CYK}
		62.5 ns ≤ t_{CYK} < 80 ns		24			t_{CYK}
Zero-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±3.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Full-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±3.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Integral linearity error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} < 4.5 V			±1.5	±4.5	LSB
Analog input voltage	V_{IAN}			–0.3		AV_{REF} + 0.3	V
A/D converter reference input voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}				2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	10	μA
			AV_{DDDR} = 5 V ±10%		10	50	μA

Notes 1. Excludes quantization error.

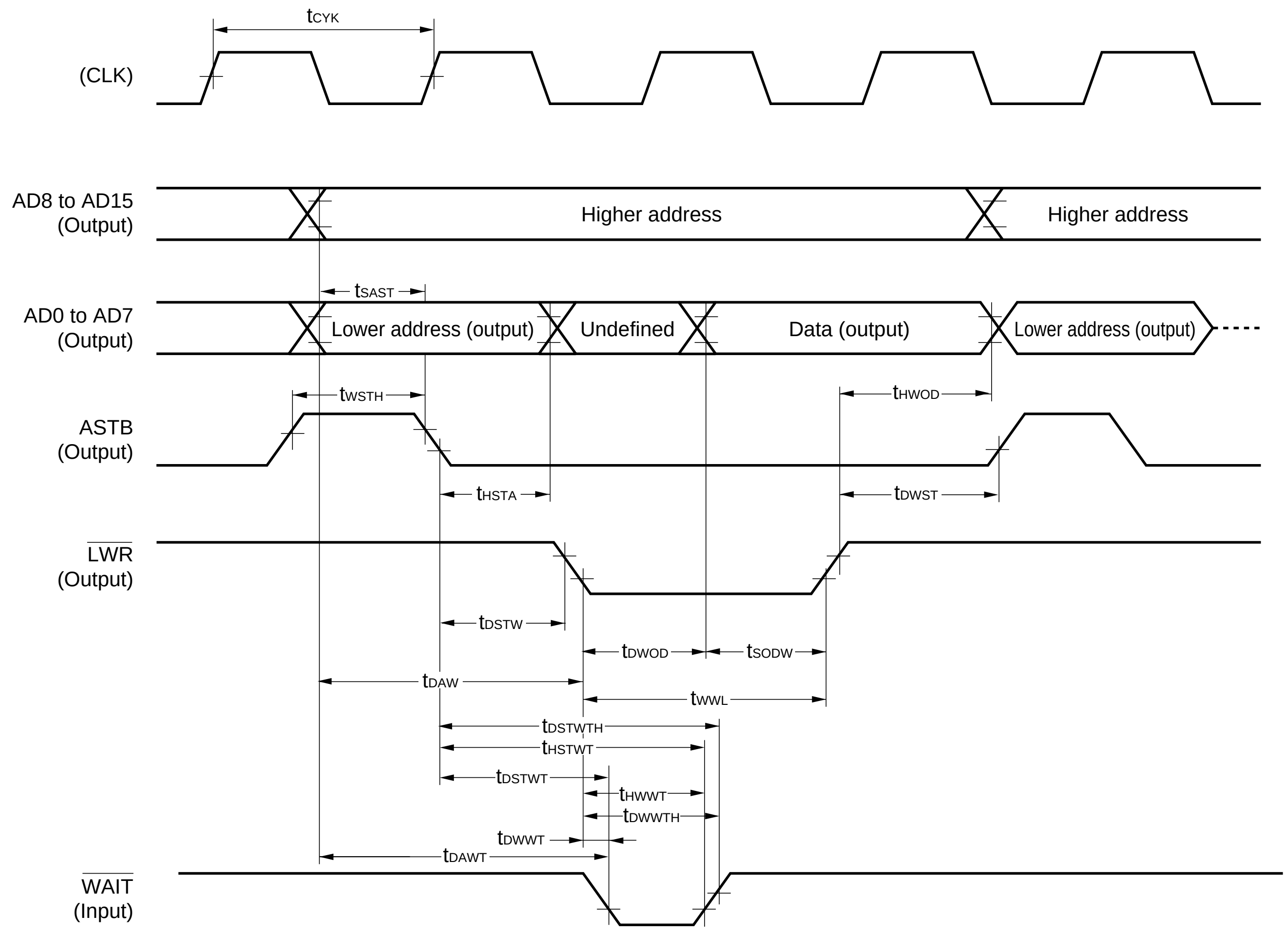
2. Indicated as a ratio (%FSR) to the full-scale value.

Remark t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency)

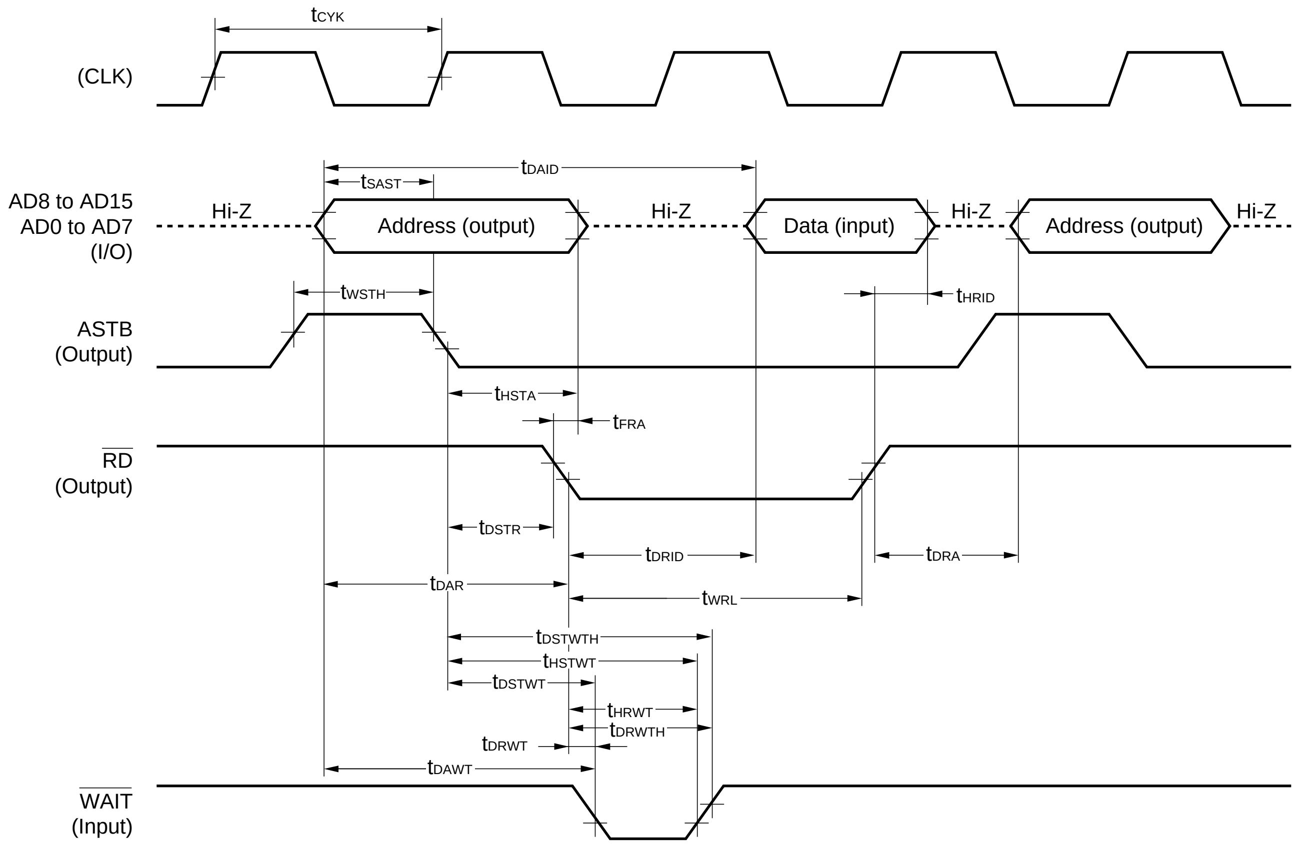
Read Operation (8 bits)



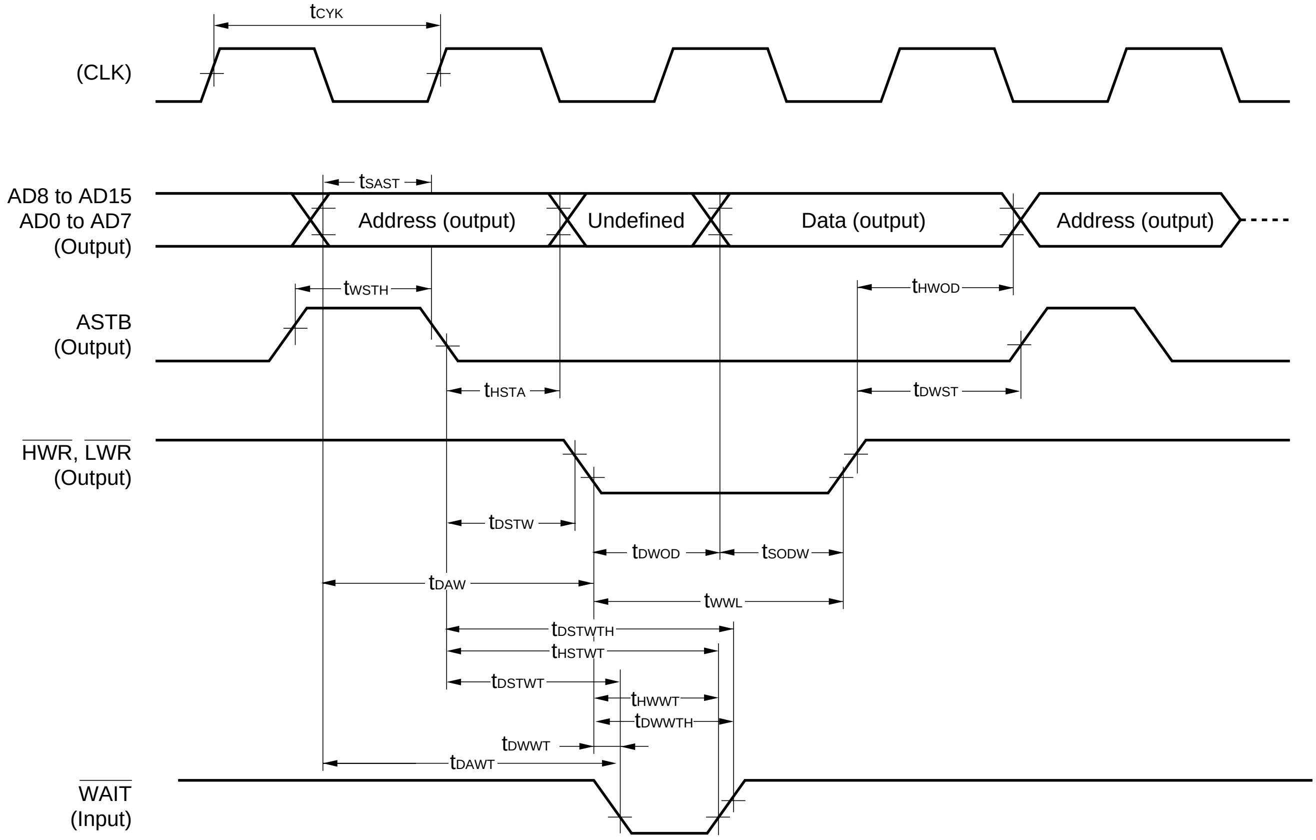
Write Operation (8 bits)



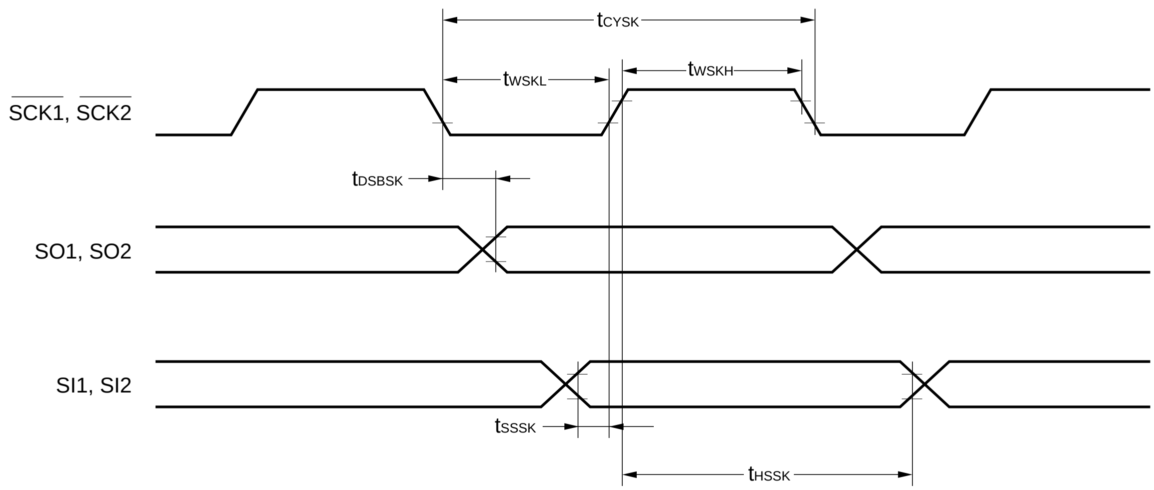
Read Operation (16 bits)



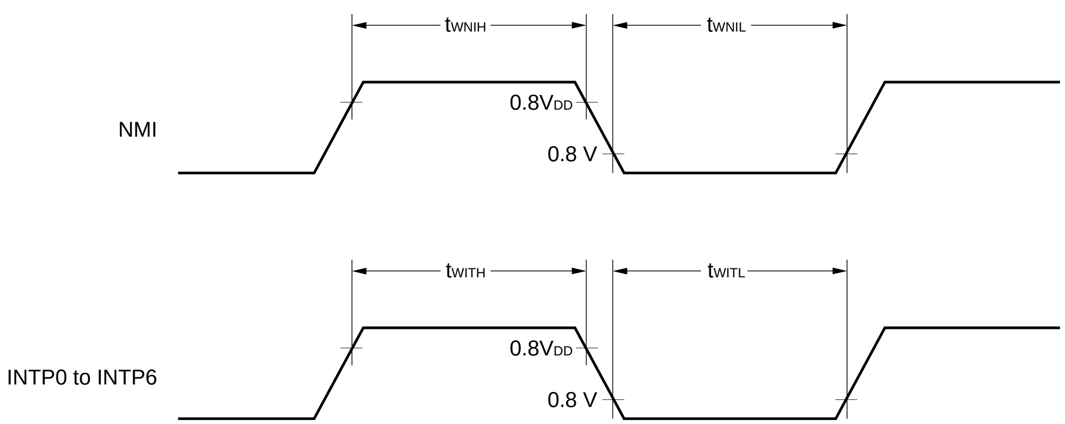
Write Operation (16 bits)



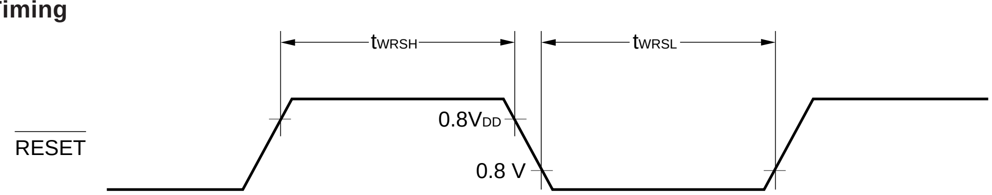
Serial Operation



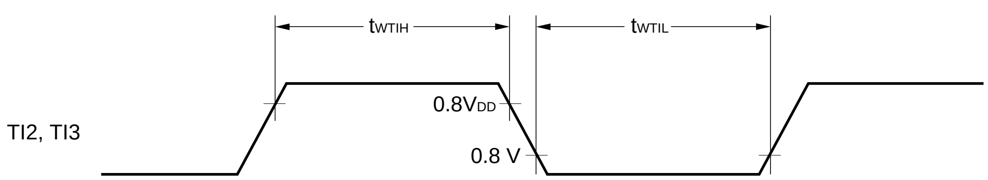
Interrupt Input Timing



Reset Input Timing

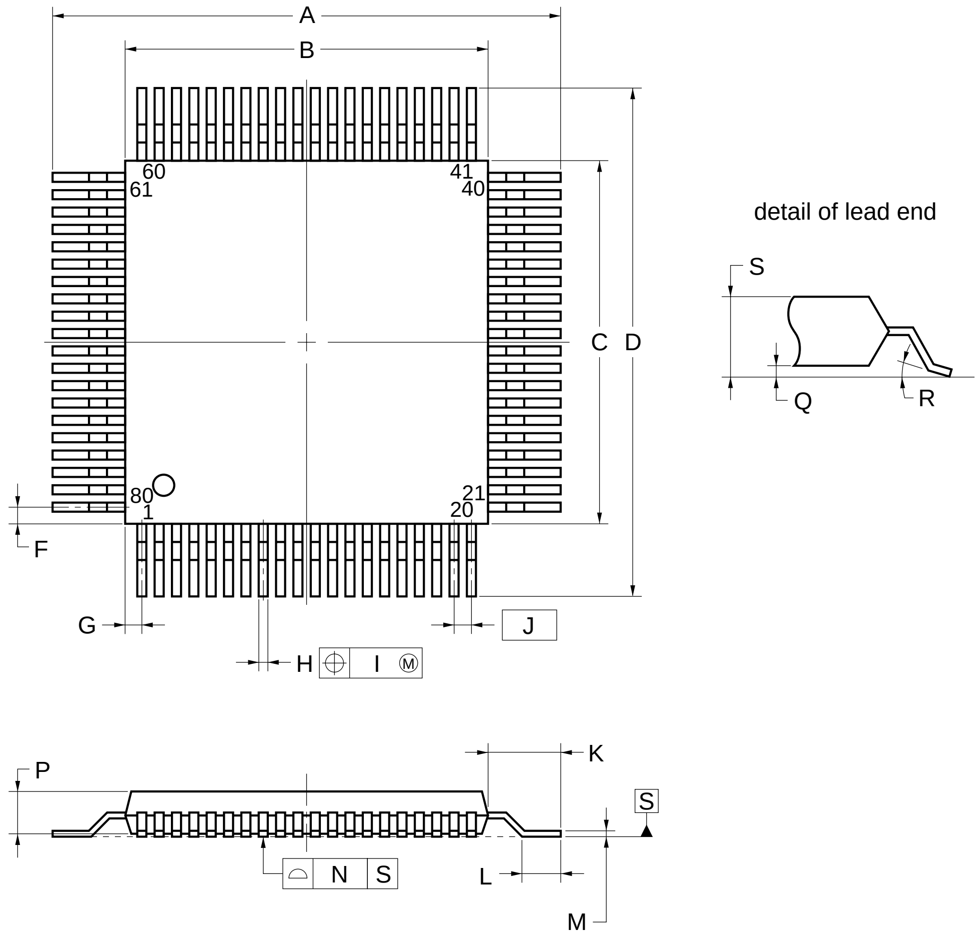


Timer Input Timing



9. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.2±0.4
B	14.0±0.2
C	14.0±0.2
D	17.2±0.4
F	0.825
G	0.825
H	0.30±0.10
I	0.13
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

S80GC-65-3B9-6

10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F4046 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F4046GC-3B9: 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 20 hours)	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 20 hours)	VP15-207-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 20 hours)	WS60-207-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F4046.
Refer to **(5) Cautions on using development tools.**

(1) Language processing software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784046	Device file for μPD784046 Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash memory writing tools

Flashpro II (Model FL-PR2), Flashpro III (Model FL-PR3, PG-FP3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-80GC	Adapter for flash memory programming

(3) Debugging tools

- **When IE-78K4-NS in-circuit emulator is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series PC (except notebook PC) is used as the host machine (C bus supported)
IE-70000-CD-IF	PC card and interface cable necessary when a PC-9800 series notebook PC is used as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT™-compatible is used as the host machine (ISA bus supported)
IE-784046-NS-EM1	Emulation board for emulating μPD784046 Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-3B9 type)
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-3B9 type)
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784046	Device file for the μPD784046 Subseries

- **When using the IE-784000-R in-circuit emulator**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series PC (except notebook PC) is used as the host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT-compatible is used as the host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter necessary when PC that incorporates PCI bus is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as the host machine
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-784046-NS-EM1 IE-784046-R-EM1	Emulation board for emulating μPD784046 Subseries
IE-78K4-R-EX2	Emulation probe conversion board necessary when the IE-784046-NS-EM1 is used in the IE-784000-R. Not necessary when the IE-784046-R-EM1 is used.
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-3B9 type)
EV-9200GC-80	Socket to be mounted on the board of the target system made for the 80-pin plastic QFP (GC-3B9 type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784046	Device file for μPD784046 Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on using development tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784046.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784046.
- FL-PR2, FL-PR3, FA-80GC, and NP-80GC are products of Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813).
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT-compatible [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	√Note	√
CC78K4	√Note	√
ID78K4-NS	√	–
ID78K4	√	√
SM78K4	√	–
RX78K/IV	√Note	√
MX78K4	√Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document	Document No.	
	Japanese	English
μPD784044, 784046 Data Sheet	U10951J	U10951E
μPD78F4046 Data Sheet	U11447J	This manual
μPD784046 Subseries User's Manual - Hardware	U11515J	U11515E
μPD784046 Subseries Special Function Register Table	U10986J	–
78K/IV Series User's Manual - Instruction	U10905J	U10905E
78K/IV Series Instruction List	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note - Software Basics	U10095J	U10095E

Documents Related to Development Tools (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K4 Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Operation	U11572J	U11572E
	Language	U11571J	U11571E
IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	U12903E
IE-784046-NS-EM1		U13744J	U13744E
IE-784046-R-EM1		U11677J	U11677E
EP-78230		EEU-985	EEU-1515
SM78K4 System Simulator Windows Based	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger PC Based	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Based	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Based	Reference	U11960J	U11960E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamentals	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	–
78K/IV Series OS MX78K4	Fundamental	U11779J	–

Other Documents

Document	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Parties	U11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

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[MEMO]

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

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Fax: 01-30-67 58 99

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Madrid Office
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Fax: 91-504-2860

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Fax: 08-63 80 388

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Hong Kong
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Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

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United Square, Singapore
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP Brasil
Tel: 55-11-6462-6810
Fax: 55-11-6462-6829

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The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.