

PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μ PD78F4218Y

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μ PD78F4218Y is a product in the μ PD784218Y subseries in the 78K/IV series.

The μ PD78F4218Y has a flash memory in the place of the internal ROM of the μ PD784218Y. Data can be written to or erased from the flash memory of the μ PD78F4218Y with the microcontroller mounted on a printed wiring board.

The μ PD78F4218Y is based on the μ PD78F4218 with an I²C bus control function appended, and is ideal for applications in audio-visual.

The functions are explained in detail in the following user's manuals. Be sure to read this manual when designing your system.

μ PD784218, 784218Y Subseries User's Manual - Hardware: Planned
78K/IV Series User's Manual - Instruction : U10905E

FEATURES

- I²C bus serial interface supporting multi master
- Pin-compatible with mask ROM model (except V_{PP} pin)
- Flash memory: 256K bytes
- Internal RAM: 12800 bytes
- Same operating voltage as mask ROM model: V_{DD} = 1.8 to 5.5 V

ORDERING INFORMATION

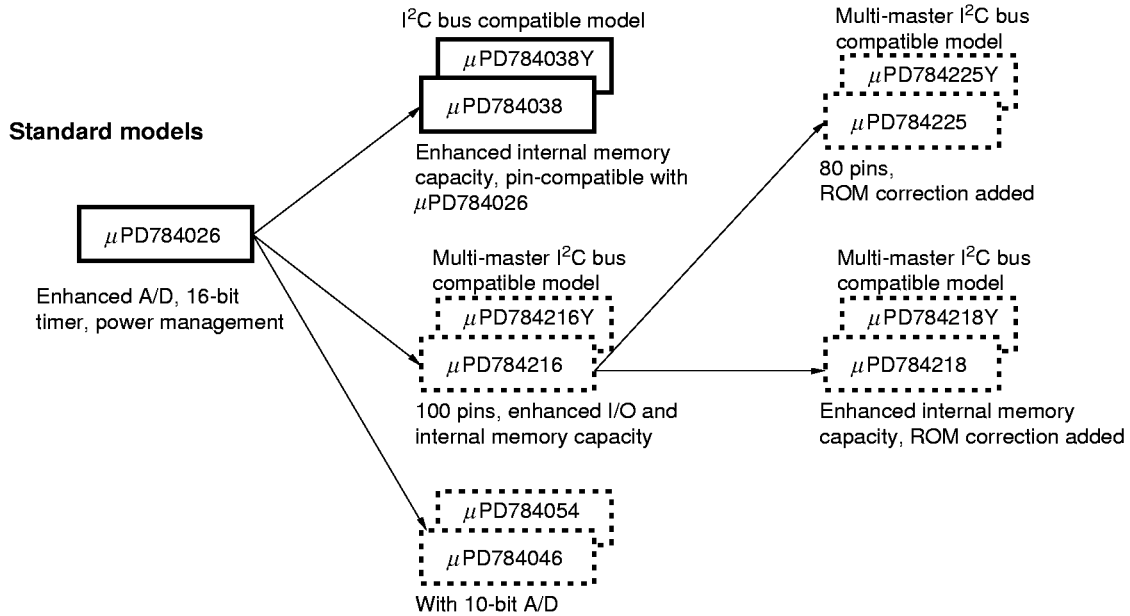
Part Number	Package
μ PD78F4218YGC-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)
μ PD78F4218YGF-3BA	100-pin plastic QFP (14 × 20 mm)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

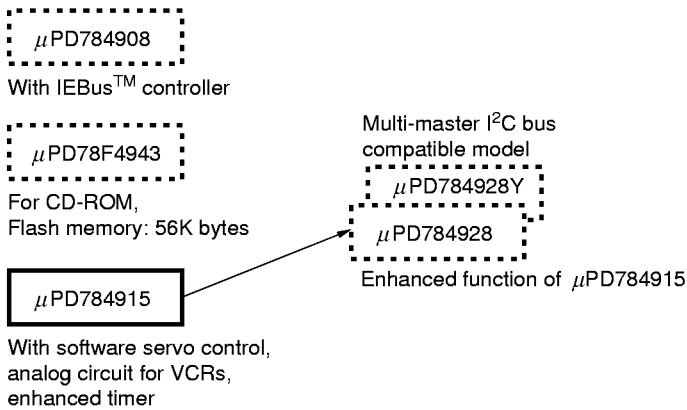
78K/IV Series Product Development

: Under mass production

: Under development



ASSP models



FUNCTIONS (1/2)

Item		Function	
Number of basic instructions (mnemonics)		113	
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
Minimum instruction execution time		• 160 ns/320 ns/640 ns/1280 ns/2560 ns (main system clock: f _{xx} = 12.5 MHz) • 61 μs (subsystem clock: f _{xx} = 32.768 KHz)	
Internal memory	Flash memory	256K bytes	
	RAM	12800 bytes	
Memory space		1 MB with program and data spaces combined	
I/O port	Total	86	
	CMOS Input	8	
	CMOS I/O	72	
	N-ch open-drain I/O	6	
Pins with ancillary functions ^{Note}	Pins with pull-up resistor	70	
	LEDs direct drive output	22	
	Medium voltage pin	6	
Real-time output port		4 bits × 2, or 8 bits × 1	
Timer/counter		16-bit timer/counter : timer register × 1 Capture/compare register × 2	Pulse output • PWM/PPG output • Square wave output • One-shot pulse output
		8-bit timer/counter 1 : timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		8-bit timer/counter 2 : timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		8-bit timer/counter 5 : timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		8-bit timer/counter 6 : timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		8-bit timer/counter 7 : timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		8-bit timer/counter 8 : timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output

Note The pins with ancillary functions are included in the I/O pins.

FUNCTIONS (2/2)

Item		Function
Serial interface		<ul style="list-style-type: none"> • UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) • CSI (3-wire serial I/O, I²C bus supporting multi master): 1 channel
A/D converter		8-bit resolution × 8 channels
D/A converter		8-bit resolution × 2 channels
Clock output		Selectable from f_{xx} , $f_{xx}/2$, $f_{xx}/2^2$, $f_{xx}/2^3$, $f_{xx}/2^4$, $f_{xx}/2^5$, $f_{xx}/2^6$, $f_{xx}/2^7$, f_{XT}
Buzzer output		Selectable from $f_{xx}/2^{10}$, $f_{xx}/2^{11}$, $f_{xx}/2^{12}$, $f_{xx}/2^{13}$
Watch timer		1 channel
Watchdog timer		1 channel
Standby		<ul style="list-style-type: none"> • HALT/STOP/IDLE mode • In power-saving mode (with subsystem clock): HALT/IDLE mode
Interrupt	Hardware	29 (internal: 20, external: 9)
	Software	BRK instruction, BRKCS instruction, operand error
	Non-maskable	Internal: 1, external: 1
	Maskable	Internal: 19, external: 8
		<ul style="list-style-type: none"> • 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching
Supply voltage		$V_{DD} = 1.8$ to 5.5 V
Package		<ul style="list-style-type: none"> • 100-pin plastic QFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)

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1. DIFFERENCES AMONG MODELS IN μPD784218Y SUBSERIES

The only difference between the μPD784217Y and 784218Y lies in the internal memory capacity.

The μPD78F4218Y is provided with a 256-KB flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

Table 1-1. Differences among Models in μPD784218Y Subseries

Part Number Item	μPD784217Y	μPD784218Y	μPD78F4218Y
Internal ROM	192K bytes (mask ROM)	256K bytes (mask ROM)	256K bytes (Flash memory)
Internal RAM	12800 bytes		
Internal memory size switching register (IMS)	None		Provided
V _{PP} pin	None		Provided

2. DIFFERENCES BETWEEN μPD78F4218Y AND μPD78F4216Y

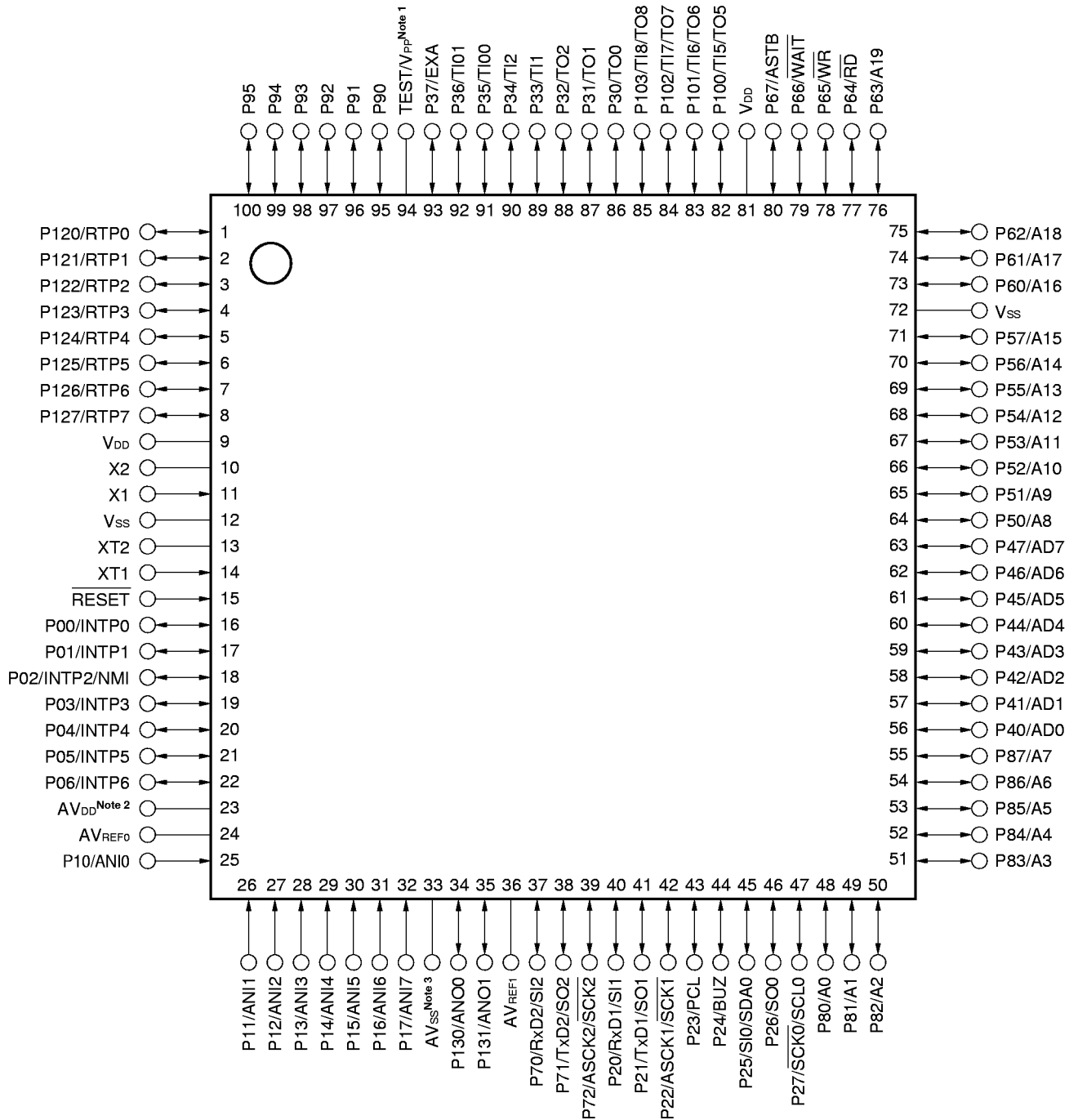
The differences between μPD78F4218Y and μPD78F4216Y are shown in Table 2-1.

Table 2-1. Differences between μPD78F4218Y and μPD78F4216Y

Part Number Item	μPD78F4218Y	μPD78F4216Y
Flash memory	256K bytes	128K bytes
Internal RAM	12800 bytes	8192 bytes
ROM correction	Provided	None
External access status function	Provided	None

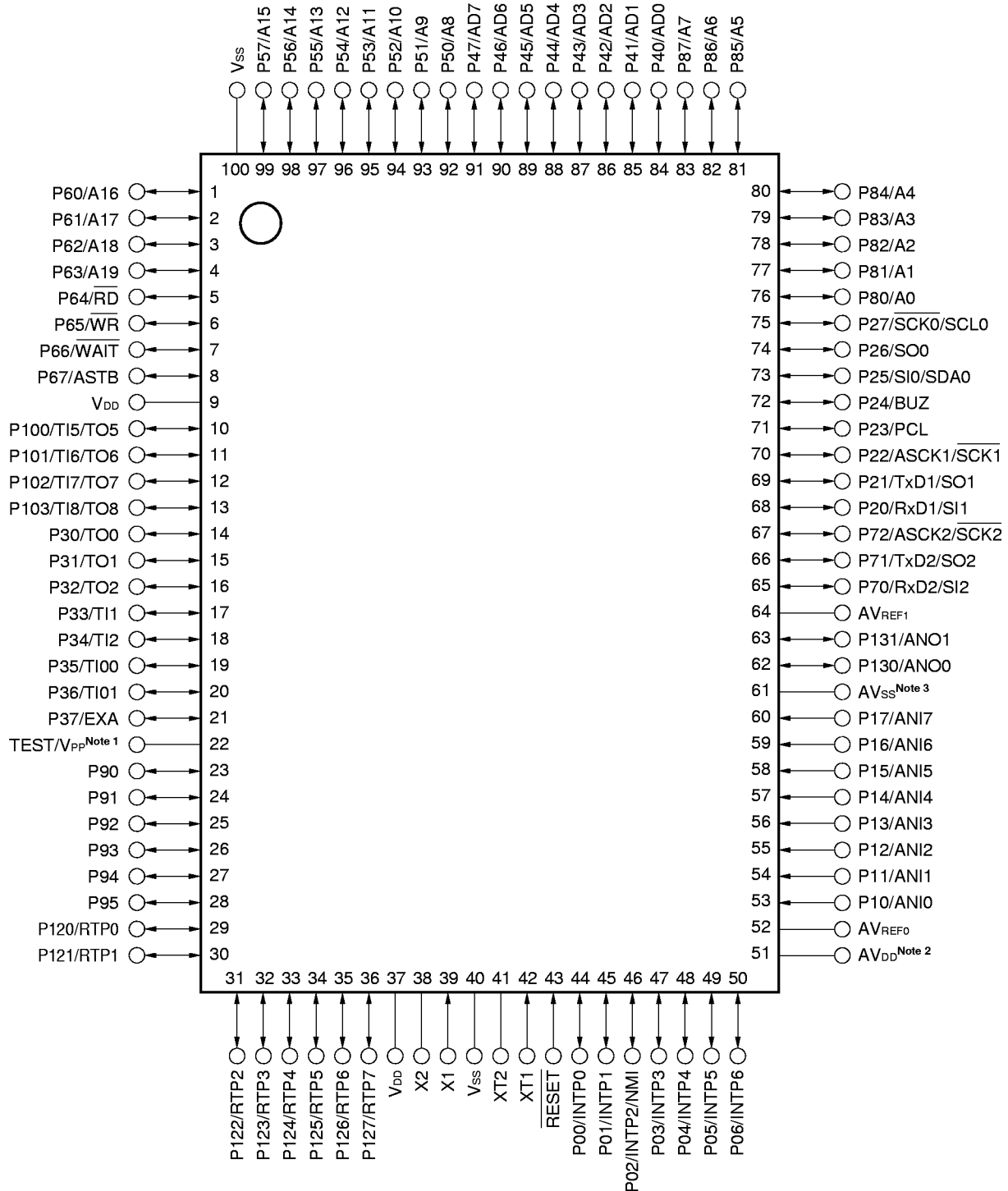
3. PIN CONFIGURATION (Top View)

- 100-pin plastic QFP (fine pitch) (14 × 14 mm)
μPD78F4218YGC-7EA



- Notes**
1. Directly connect the TEST/V_{PP} pin to V_{SS} in normal operation mode.
 2. Connect the AV_{DD} pin to V_{DD}.
 3. Connect the AV_{SS} pin to V_{SS}.

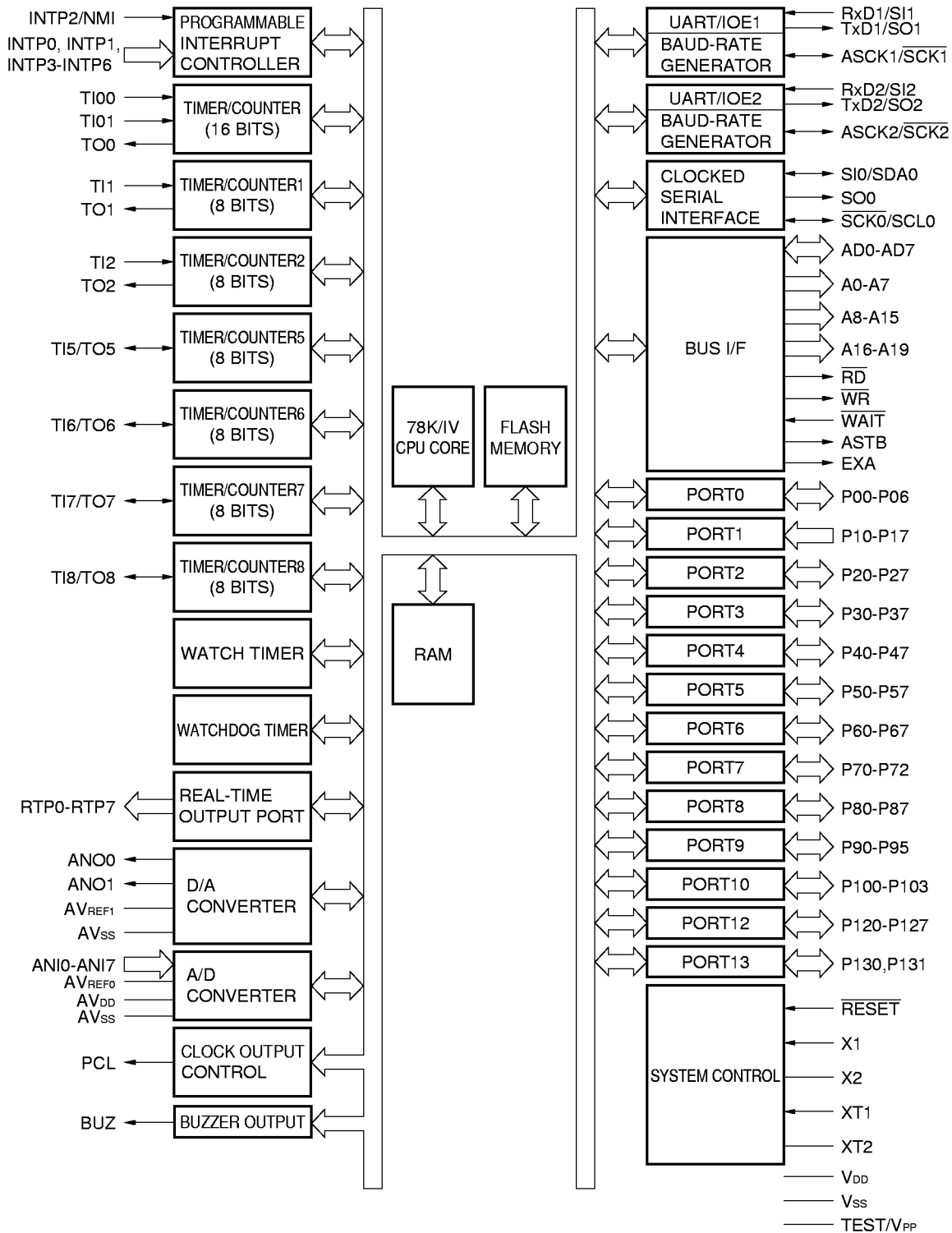
- 100-pin plastic QFP (14 × 20 mm)
μPD78F4218YGF-3BA



- Notes**
1. Directly connect the TEST/V_{PP} pin to V_{SS} in normal operation mode.
 2. Connect the AV_{DD} pin to V_{DD}.
 3. Connect the AV_{SS} pin to V_{SS}.

A0-A19	: Address Bus	P120-P127	: Port12
AD0-AD7	: Address/Data Bus	P130, P131	: Port13
ANI0-ANI7	: Analog Input	PCL	: Programmable Clock
ANO0, ANO1	: Analog Output	\overline{RD}	: Read Strobe
ASCK1, ASCK2	: Asynchronous Serial Clock	\overline{RESET}	: Reset
ASTB	: Address Strobe	RTP0-RTP7	: Real-time Output Port
AV _{DD}	: Analog Power Supply	RxD1, RxD2	: Receive Data
AV _{REF0} , AV _{REF1}	: Analog Reference Voltage	$\overline{SCK0-SCK2}$: Serial Clock
AV _{SS}	: Analog Ground	SCL0	: Serial Clock
BUZ	: Buzzer Clock	SDA0	: Serial Data
EXA	: External Access Status Output	SI0-SI2	: Serial Input
INTP0-INTP6	: Interrupt from Peripherals	SO0-SO2	: Serial Output
NMI	: Non-maskable Interrupt	TEST	: Test
P00-P06	: Port0	TI00, TI01,	
P10-P17	: Port1	TI1, TI2, TI5-TI8	: Timer Input
P20-P27	: Port2	TO0-TO2, TO5-TO8	: Timer Output
P30-P37	: Port3	TxD1, TxD2	: Transmit Data
P40-P47	: Port4	V _{DD}	: Power Supply
P50-P57	: Port5	V _{PP}	: Programming Power Supply
P60-P67	: Port6	V _{SS}	: Ground
P70-P72	: Port7	\overline{WAIT}	: Wait
P80-P87	: Port8	\overline{WR}	: Write Strobe
P90-P95	: Port9	X1, X2	: Crystal (Main System Clock)
P100-P103	: Port10	XT1, XT2	: Crystal (Subsystem Clock)

4. BLOCK DIAGRAM



5. PIN FUNCTION

5.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 7-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P01		INTP1	
P02		INTP2/NMI	
P03		INTP3	
P04		INTP4	
P05		INTP5	
P06		INTP6	
P10-P17	Input	ANI0-ANI7	Port 1 (P1): • 8-bit input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P21		TxD1/SO1	
P22		ASCK1/SCK1	
P23		PCL	
P24		BUZ	
P25		SI0/SDA0	
P26		SO0	
P27		SCK0/SCL0	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P31		TO1	
P32		TO2	
P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		EXA	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.

5.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): <ul style="list-style-type: none"> • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software.
P61		A17	
P62		A18	
P64		$\overline{\text{RD}}$	
P65		$\overline{\text{WR}}$	
P66		$\overline{\text{WAIT}}$	
P67		ASTB	
P70		I/O	
P71	TxD2/SO2		
P72	$\overline{\text{ASCK2/SCK2}}$		
P80-P87	I/O	A0-A7	Port 8 (P8): <ul style="list-style-type: none"> • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise. • Interrupt control flag (KRIF) is set to 1 when falling edge is detected at a pin of this port.
P90-P95	I/O	—	Port 9 (P9): <ul style="list-style-type: none"> • N-ch open-drain medium-voltage I/O port • 6-bit I/O port • Can be set in input or output mode bit-wise. • Can directly drive LEDs.
P100	I/O	TI5/TO5	Port 10 (P10): <ul style="list-style-type: none"> • 4-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P101		TI6/TO6	
P102		TI7/TO7	
P103		TI8/TO8	
P120-P127	I/O	RTP0-RTP7	Port 12 (P12): <ul style="list-style-type: none"> • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): <ul style="list-style-type: none"> • 2-bit I/O port • Can be set in input or output mode bit-wise.

5.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	
TI00	Input	P35	External count clock input to 16-bit timer register	
TI01		P36	Capture trigger signal input to capture/compare register 00	
TI1		P33	External count clock input to 8-bit timer register 1	
TI2		P34	External count clock input to 8-bit timer register 2	
TI5		P100/TO5	External count clock input to 8-bit timer register 5	
TI6		P101/TO6	External count clock input to 8-bit timer register 6	
TI7		P102/TO7	External count clock input to 8-bit timer register 7	
TI8		P103/TO8	External count clock input to 8-bit timer register 8	
TO0		Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1	P31		8-bit timer output (shared by 8-bit PWM output)	
TO2	P32			
TO5	P100/TI5			
TO6	P101/TI6			
TO7	P102/TI7			
TO8	P103/TI8			
RxD1	Input			P20/SI1
RxD2		P70/SI2		Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)	
TxD2		P71/SO2	Serial data output (UART2)	
ASCK1	Input	P22/ $\overline{\text{SCK1}}$	Baud rate clock input (UART1)	
ASCK2		P72/ $\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SI0	Input	P25/SDA0	Serial data input (3-wire serial clock I/O0)	
SI1		P20/RxD1	Serial data input (3-wire serial clock I/O1)	
SI2		P70/RxD2	Serial data input (3-wire serial clock I/O2)	
SO0	Output	P26	Serial data output (3-wire serial I/O0)	
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)	
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)	
SDA0	I/O	P25/SI0	Serial data input/output (I ² C bus)	
$\overline{\text{SCK0}}$	I/O	P27/SCL0	Serial clock input/output (3-wire serial I/O0)	
$\overline{\text{SCK1}}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)	
$\overline{\text{SCK2}}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)	
SCL0		P27/ $\overline{\text{SCK0}}$	Serial clock input/output (I ² C bus)	
NMI	Input	P02/INTP2	Non-maskable interrupt request input	
INTP0		P00	External interrupt request input	
INTP1		P01		
INTP2		P02/NMI		
INTP3		P03		
INTP4		P04		
INTP5		P05		
INTP6		P06		

5.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function	
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)	
BUZ	Output	P24	Buzzer output	
RTP0-RTP7	Output	P120-P127	Real-time output port that outputs data in synchronization with trigger	
AD0-AD7	I/O	P40-P47	Low-order address/data bus when external memory is connected	
A0-A7	Output	P80-P87	Low-order address bus when external memory is connected	
A8-A15		P50-P57	Middle-order address bus when external memory is connected	
A16-A19		P60-P63	High-order address bus when external memory is connected	
\overline{RD}	Output	P64	Strobe signal output for read operation of external memory	
\overline{WR}		P65	Strobe signal output for write operation of external memory	
\overline{WAIT}	Input	P66	To insert wait state(s) when external memory is accessed	
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 through 6 and port 8 to access external memory	
EXA	Output	P37	Status signal output when external memory is accessed	
\overline{RESET}	Input	—	System reset input	
X1	Input	—	To connect main system clock oscillation crystal	
X2	—			
XT1	Input	—	To connect subsystem clock oscillation crystal	
XT2	—			
ANI0-ANI7	Input	P10-P17	Analog voltage input for A/D converter	
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter	
AV _{REF0}	—	—	To apply reference voltage for A/D converter	
AV _{REF1}			To apply reference voltage for D/A converter	
AV _{DD}			Positive power supply for A/D converter. Connected to V _{DD} .	
AV _{SS}			GND for A/D converter and D/A converter. Connected to V _{SS} .	
V _{DD}			Positive power supply	
V _{SS}			GND	
TEST			V _{PP}	Directly connect this pin to V _{SS} (this pin is for IC test).
V _{PP}			TEST	Sets flash memory programming mode. To apply a high voltage when program is written or verified.

5.3 I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins

Table 5-1 shows symbols indicating the I/O circuit types of the respective pins and the recommended connection of unused pins.

For the circuit diagram of each type of I/O circuit, refer to **Figure 5-1**.

Table 5-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (1/2)

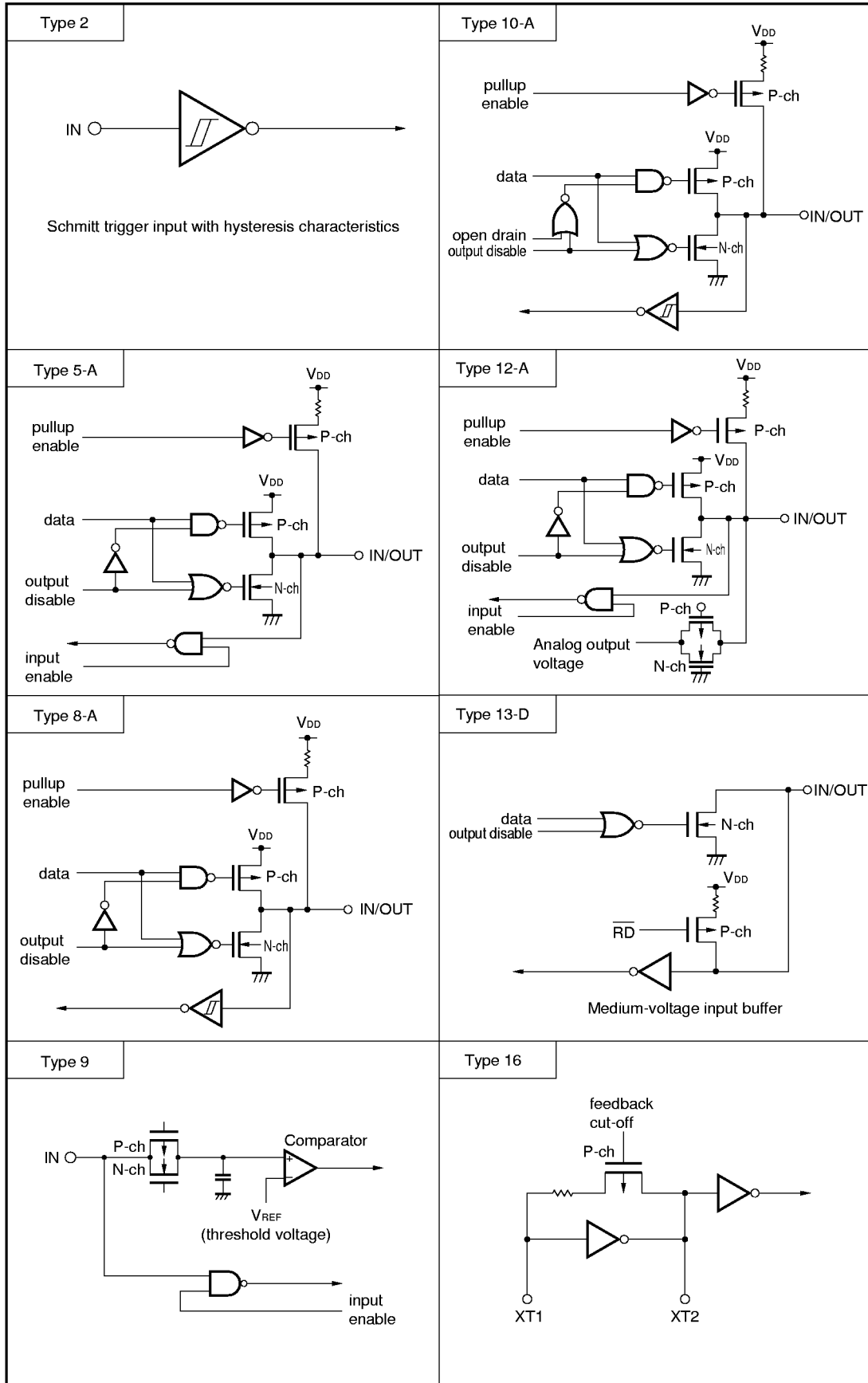
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-A	I/O	Input : Individually connected to V _{SS} via resistor Output: Open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3-P06/INTP6			
P10/ANI0-P17/ANI7	9	Input	Connected to V _{SS} or V _{DD}
P20/RxD1/SI1	10-A	I/O	Input : Individually connected to V _{SS} via resistor Output: Open
P21/TxD1/SO1			
P22/ASCK1/SCK1			
P23/PCL			
P24/BUZ			
P25/SDA0/SI0			
P26/SO0			
P27/SCL0/SCK0			
P30/TO0-P32/TO2	8-A		
P33/TI1, P34/TI2			
P35/TI00, P36/TI01			
P37/EXA			
P40/AD0-P47/AD7	5-A		
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/RD			
P65/WR			
P66/WAIT			
P67/ASTB			
P70/RxD2/SI2	8-A		
P71/TxD2/SO2			
P72/ASCK2/SCK2			
P80/A0-P87/A7			
P90-P95	13-D		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102/TI7/TO7			
P103/TI8/TO8			
P120/RTP0-P127/RTP7			
P130/ANO0, P131/ANO1	12-A		

Table 5-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
RESET	2	Input	—
XT1	16	—	Connected to V _{SS}
XT2			Open
AV _{REF0}	—	—	Connected to V _{SS}
AV _{REF1}			Connected to V _{DD}
AV _{DD}			
AV _{SS}			Connected to V _{SS}
TEST/V _{PP}			Directly connected to V _{SS}

Remark Because the circuit type numbers are standardized among the 78K series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 5-1. Types of Pin I/O Circuits



6. INTERNAL MEMORY SIZE SELECT REGISTER (IMS)

The IMS is a register that prevents by software a part of the internal memory from being used. By using this register, the memory of the μPD78F4218Y can be mapped in the same manner as a mask ROM model with different internal memory (ROM and RAM) capacity.

This register is set by using an 8-bit memory manipulation instruction.

Its value is set to FFH by RESET input.

Figure 6-1. Format of Internal Memory Size Select Register (IMS)

Address: 0FFFCH At reset: FFH W

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Selects internal ROM capacity
0	0	64K bytes
0	1	128K bytes
1	0	192K bytes
1	1	256K bytes

RAM1	RAM0	Selects peripheral RAM capacity
0	0	3072 bytes
0	1	6656 bytes
1	0	7168 bytes
1	1	12288 bytes

Caution IMS is not provided on the mask ROM models (μPD784217Y and 784218Y).

The value to be set to the IMS to map the memory of the μPD78F4218Y in the same manner as the mask ROM model is shown in Table 6-1.

Table 6-1. Set Value of Internal Memory Size Select Register (IMS)

Mask ROM Model	Set Value of IMS
μPD784217Y	EFH
μPD784218Y	FFH

7. PROGRAMMING FLASH MEMORY

The flash memory can be written with the μPD78F4218Y mounted on the target board (on-board). To do so, connect a dedicated flash writer (Flashpro II) to the host machine and target system.

Remark Flashpro II is a product of Naito Densai Machida Mfg. Co., Ltd.

7.1 Selecting Communication Mode

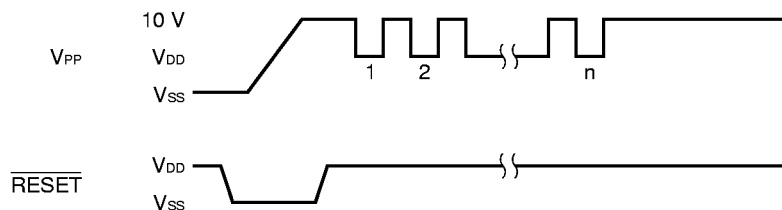
To write the flash memory, use Flashpro II and serial communication. Select a serial communication mode from those listed in Table 7-1 in the format shown in Figure 7-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 7-1.

Table 7-1. Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V _{PP} Pulses
3-wire serial I/O	3	SCK0/SCL0/P27 SO0/P26 SI0/SDA0/P25	0
		SCK1/ASCK1/P22 SO1/TxD1/P21 SI1/RxD1/P20	1
		SCK2/ASCK2/P72 SO2/TxD2/P71 SI2/RxD2/P70	2
UART	2	TxD1/SO1/P21 RxD1/SI1/P20	8
		TxD2/SO2/P71 RxD2/SI2/P70	9

Caution Be sure to select a communication mode with the number of V_{PP} pulses shown in Table 7-1.

Figure 7-1. Communication Mode Selecting Format



7.2 Flash Memory Programming Function

The flash memory is written by transferring or receiving commands and data in a selected communication mode. The major functions of flash memory programming are listed in Table 7-2.

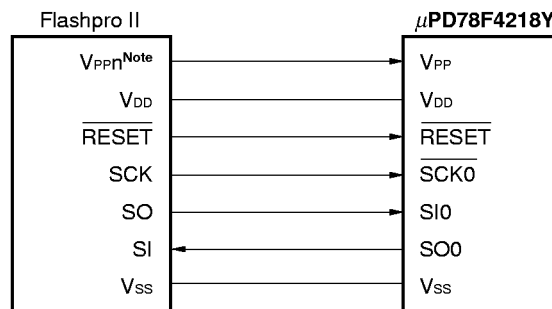
Table 7-2. Major Functions of Flash Memory Programming

Function	Description
Batch erasure	Erases all contents of memory.
Block erasure	Erases contents of specified memory block with one memory block consisting of 16K bytes.
Batch blank check	Checks erased status of entire memory.
Block blank check	Checks erased status of specified block
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Batch verify	Compares all contents of memory with input data.
Block verify	Compares contents of specified memory block with input data.

7.3 Connecting Flashpro II

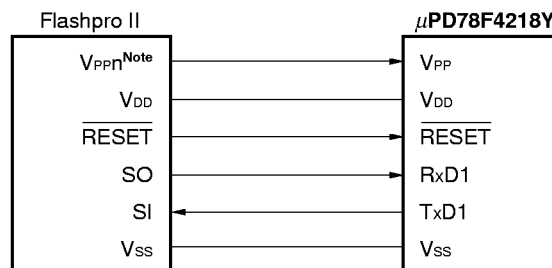
The Flashpro II and μPD78F4218Y are connected differently depending on the selected communication mode (3-wire serial I/O or UART). Figures 7-2 and 7-3 show the connections in the respective communication modes.

Figure 7-2. Connection of Flashpro II in 3-Wire Serial I/O Mode (when using 3-wire serial I/O0)



Note n = 1, 2

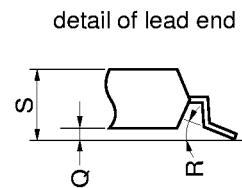
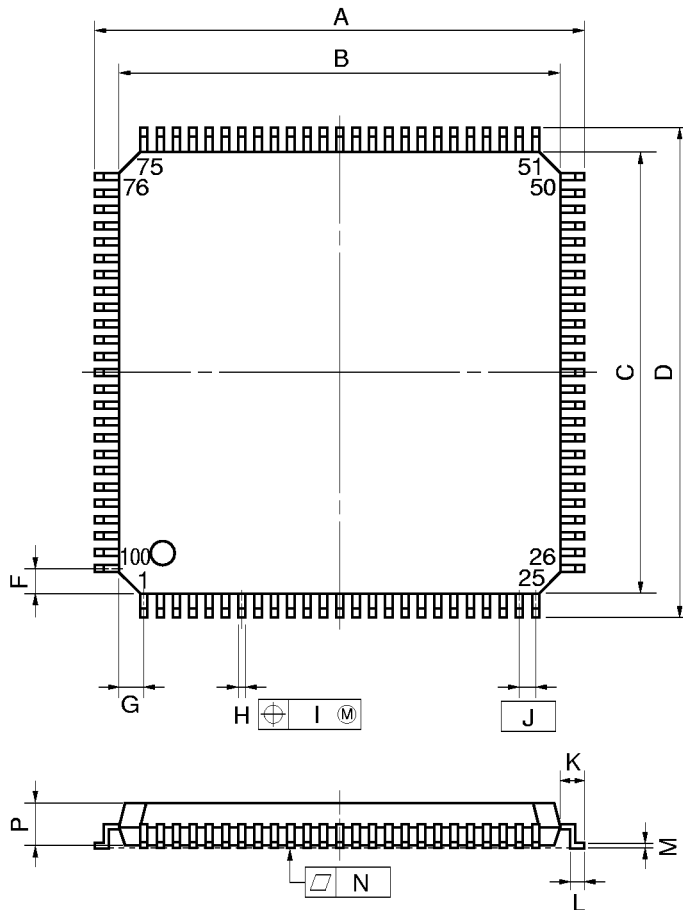
Figure 7-3. Connection of Flashpro II in UART Mode (when using UART1)



Note n = 1, 2

8. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



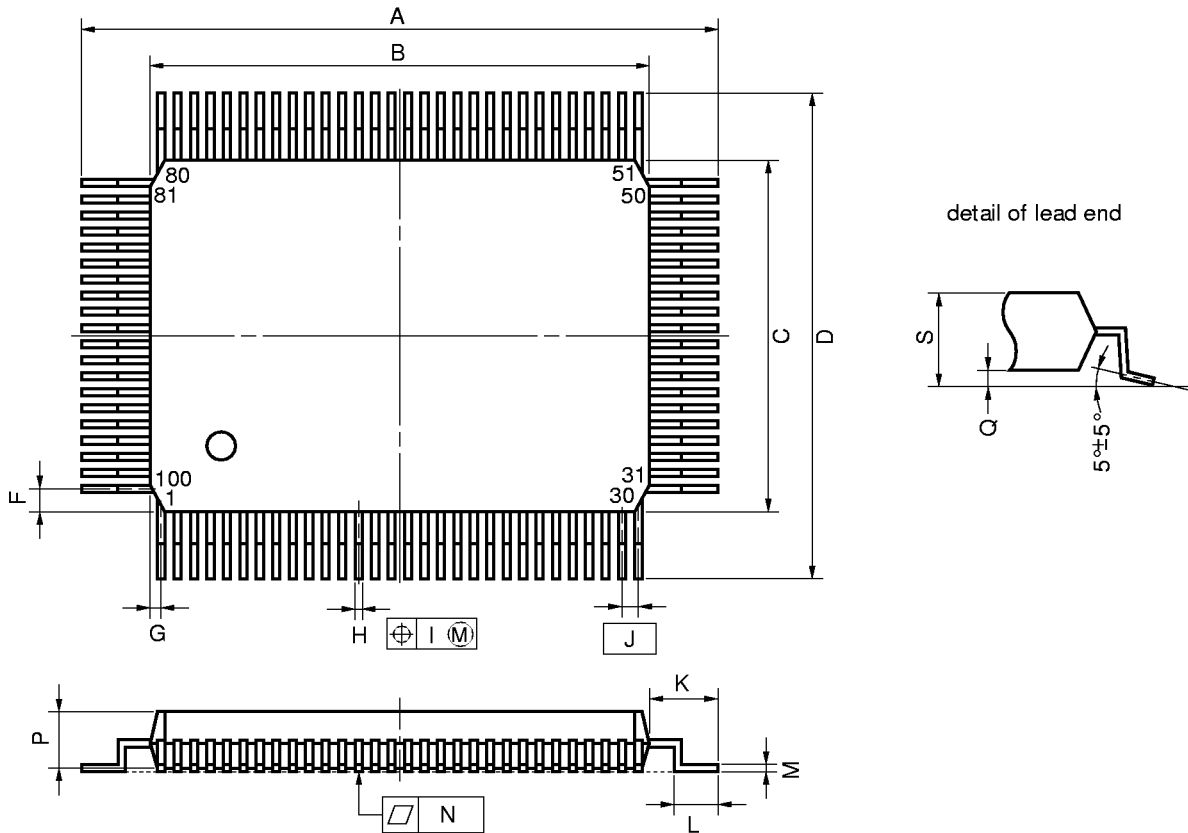
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

100 PIN PLASTIC QFP (14 × 20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P100GF-65-3BA1-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for supporting development of a system using the μPD78F4218Y.

Language processor software

RA78K4 ^{Note 1}	Assembler package common to 78K/IV series
CC78K4 ^{Note 1}	C compiler package common to 78K/IV series
CC78K4-L ^{Note 1}	C compiler library source file common to 78K/IV series

Flash memory writing tool

Flashpro II	Dedicated flash writer. Flashpro II is the product of Naito Densai Machida Mfg. Co., Ltd.
FA-100GC FA-100GF	Adapter for flash memory writing. Flash memory writing adapter is a product of Naito Densai Machida Mfg. Co., Ltd.

Debugging tool

IE-784000-R	In-circuit emulator common to 78K/IV series
IE-784000-R-BK	Break board common to 78K/IV series
IE-784218-R-EM1 IE-784000-R-EM	Emulation board for evaluation of μPD784218Y subseries
IE-70000-98-IF-B	Interface adapter when PC-9800 series (except notebook type) is used as host machine
IE-70000-98N-IF	Interface adapter and cable when notebook type PC-9800 series is used as host machine
IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as host machine
IE-78000-R-SV3	Interface adapter and cable when EWS is used as host machine
EP-78064GC-R	Emulation probe for 100-pin plastic QFP (fine pitch) (GC-7EA type) common to μPD784218Y subseries
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GC-3BA type) common to μPD784218Y subseries
TGC-100SDW	Adapter mounted on board of target system created for 100-pin plastic QFP (fine pitch) (GC-7EA type). TGC-100SDW is the product of Tokyo Eletech Corporation ((03) 5295-1661). Consult NEC distributor when purchasing the product.
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
SM78K4 ^{Note 2}	System simulator common to 78K/IV series
ID78K4 ^{Note 2}	Integrated debugger for IE-784000-R
DF784218 ^{Note 3}	Device file for μPD784218Y subseries

Real-time OS

RX78K/IV ^{Note 3}	Real-time OS for 78K/IV series
MX78K4 ^{Note 4}	OS for 78K/IV series

Remark RA78K4, CC78K4, SM78K4, and ID78K4 are used in combination with DF784218.

- Notes**
1. • PC-9800 series (MS-DOS™) base
 - IBM PC/AT and compatible machine (PC DOS™, Windows™, MS-DOS, IBM DOS™) base
 - HP9000 series 700™ (HP-UX™) base
 - SPARCstation™ (SunOS™) base
 - NEWS™ (NEWS-OS™) base
 2. • PC-9800 series (MS-DOS+Windows) base
 - IBM PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base
 - HP9000 series 700 (HP-UX) base
 - SPARCstation (SunOS) base
 3. • PC-9800 series (MS-DOS) base
 - IBM PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base
 - HP9000 series 700 (HP-UX) base
 - SPARCstation (SunOS) base
 4. • PC-9800 series (MS-DOS) base
 - IMB PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base

APPENDIX B. RELATED DOCUMENTS

Documents related to device

Document Name	Document No.	
	Japanese	English
μPD784217Y, 784218Y Preliminary Product Information	U12304J	U11725E
μPD78F4218Y Preliminary Product Information	U11824J	This document
μPD784218, 784218Y Subseries User's Manual - Hardware	Planned	Planned
μPD784218Y Subseries Special Function Register Table	Planned	–
78K/IV Series User's Manual - Instruction	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note - Software Basics	U10095J	–

Documents related to development tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	–
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K4 Series	Operation	EEU-960	–
	Language	EEU-961	–
CC78K Series Library Source File		U12322J	–
IE-784000-R		EEU-5004	EEU-1534
IE-784218-R-EM1		U12155J	U12155E
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator - Windows base	Reference	U10093J	U10093E
SM78K Series System Simulator	External component user open interface specification	U10092J	U10092E
ID78K4 Integrated Debugger - Windows base	Reference	U10440J	U10440E

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.

Documents related to embedded software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basics	U10603J	–
	Installation	U10604J	–
	Debugger	U10364J	–
78K/IV Series OS MX78K4	Basics	U11779J	–

Other documents

Document Name		Document No.	
		Japanese	English
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
Quality Grades on NEC Semiconductor Devices		C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System		C10983J	C10983E
Electrostatic Discharge (ESD) Test		MEM-539	–
Guide to Quality Assurance for Semiconductor Devices		C11893J	MEI-1202
Guide to Microcomputer-Related Products by Third Parties		U11416J	–

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.