

# NEC

NEC Electronics Inc.

## $\mu$ PD795 1024-BIT CCD IMAGE SENSOR

### PRELIMINARY INFORMATION

#### Description

The  $\mu$ PD795 is a CCD (charge-coupled device) linear image sensor that changes optical images to electrical signals. It has 1024 photo-elements, two lines of 525-bit CCD charge transfer registers, a drive unit, a sample-and-hold circuit, and an output amplifier. The drive unit simplifies the external circuit and reduces total drive power. The sample-and-hold circuit substantially reduces output signal noise.

The photo-elements have excellent response characteristics because of their PN junction construction. They are 14 by 9  $\mu$ m separated by 5- $\mu$ m channel stoppers.

The CCD charge transfer registers have very high transfer efficiency, above 99.996 percent.

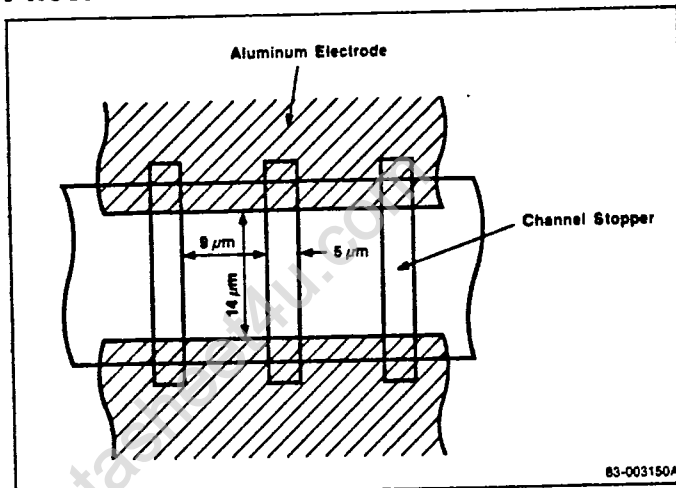
#### Features

- Excellent photo-electrical characteristics
- Single 12-volt power supply
- On-chip drive unit and sample-and-hold circuit
- High resolution of 8 dots per mm across 12.8-cm page
- Transfer efficiency above 99.996 percent
- 20-pin ceramic DIP

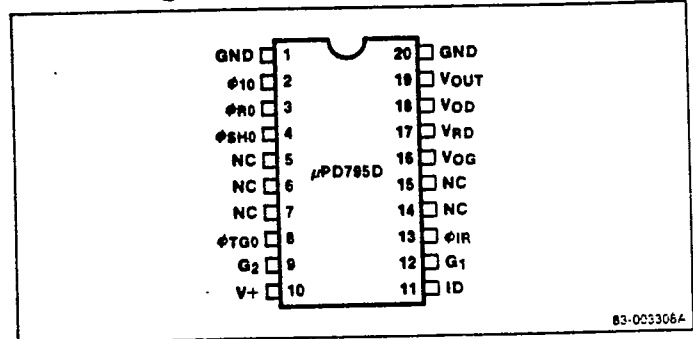
#### Applications

Facsimile  
OCR (optical character reader)  
Instrumentation

#### Photo-Element Construction



#### Pin Configuration



#### Pin Identification

Pin	Name	*Function
1	GND	Ground
2	$\phi$ 10	Register clock input
3	$\phi$ R0	Reset gate clock input
4	$\phi$ SH0	Sample-and-hold clock input
5, 6, 7	NC	No connection
8	$\phi$ TG0	Transfer gate clock input
9	G2	Test input
10	V+	Drive unit power supply input
11	ID	Test input
12	G1	Test input
13	$\phi$ IR	Test input
14, 15	NC	No connection
16	V0G	Output gate bias input
17	VRD	Reset part power supply input
18	V0D	Output amplifier power supply input
19	V0UT	Output
20	GND	Ground

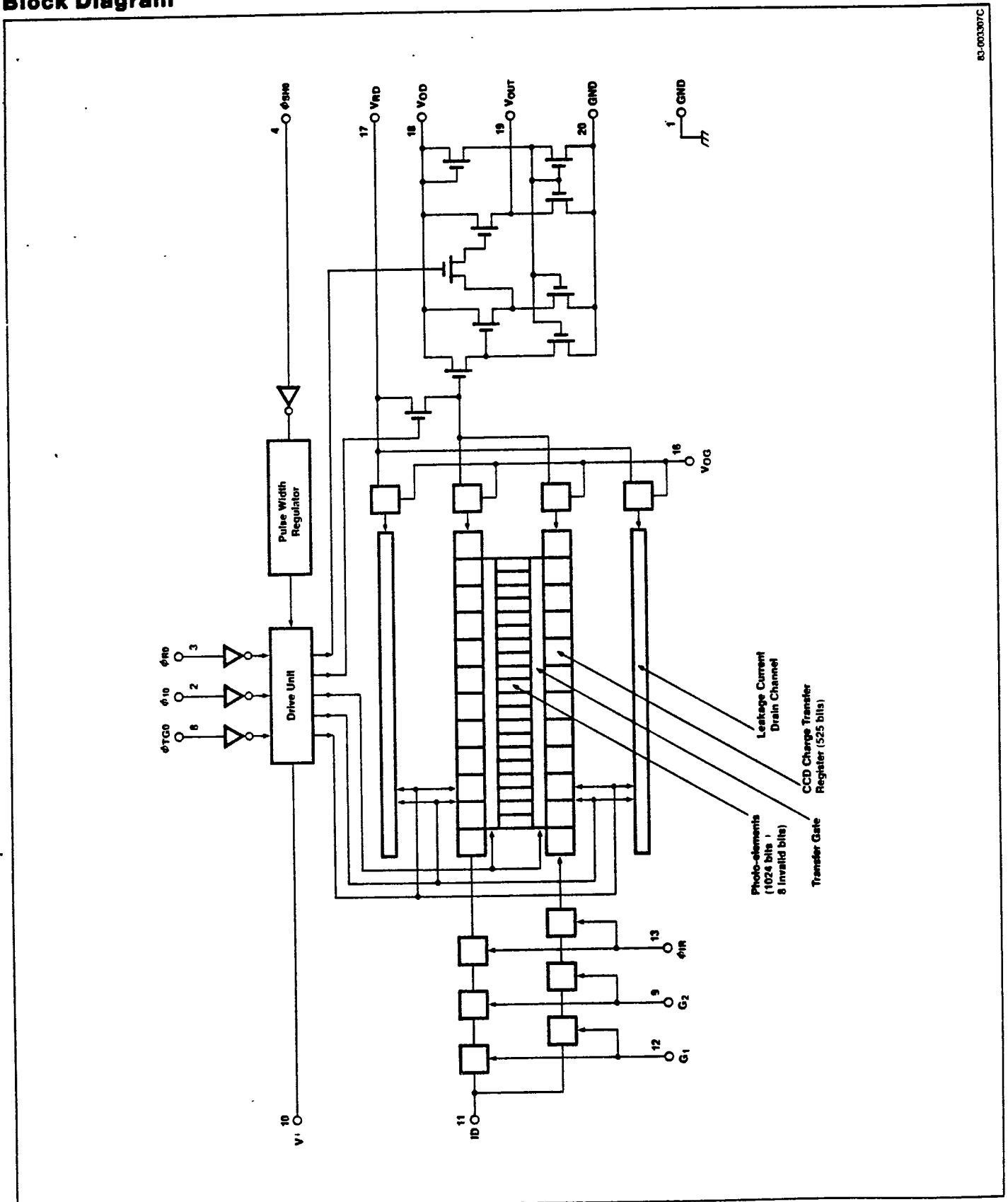
\*All NC pins should be connected to ground.

#### Ordering Information

Part Number	Package	Operating Ambient Temperature
$\mu$ PD795D	20-pin ceramic DIP	-25 to +55 $^{\circ}$ C

## $\mu$ PD795

### Block Diagram



**NEC****μPD795****Electrical Characteristics**

$T_A = +25^\circ\text{C}$ ; source of light, 2856 K tungsten lamp; exposure period = 5.0 ms;  $V_{GG}$ ,  $V_{OD}$ , and  $V_{RD} = 12.0\text{ V}$ ;  $f_{\phi 10} = 250\text{ kHz}$ ;  $f_{\phi R0} = 500\text{ kHz}$ .

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Saturation Output Voltage	$V_{SAT}$	400	650		mV	
Saturation Exposure	SE	0.15	0.20		ixes	
Photo-Response Nonuniformity	PRNU		$\pm 5$	$\pm 10$	%	$V_{OUT} = 200\text{ mV}$ ; Infrared cut filter, Corning 1-75
Average Dark Signal	ADS		3	10	mV	No exposure
Dark Signal Nonuniformity	DSNU		5	15	mV	No exposure
Working Power Consumption	$P_D$		200		mW	Current of pins 10, 17, and 18 x supply voltage
Spectral Response Range Limits	SR	0.3		1.1	$\mu\text{m}$	
Sensitivity	S	2000	3250	4500	mV/ixes	
Offset Voltage	$V_{io}$		4.0		V	0% level of $V_{OUT}$ in timing waveforms
Feed-Through Delay Time	$t_D$		50	100	ns	See timing waveforms.
Feed-Through Level	$V_{FT}$		70	120	mV	
Feed-Through Pulse Width	$t_{pw}$		70	120	ns	

**Reference Characteristics**

Parameter	Limits			Unit
	Min	Typ	Max	
Input Capacitance at $\phi_{10}$ , $\phi_{RD}$ , $\phi_{SHD}$ , or $\phi_{TGO}$ (pins 2, 3, 4, 8)		5	10	pF
Rise Time and Fall Time of Feed-Through Pulse		50	100	ns
Output Impedance at $V_{OUT}$ (pin 19)	0.5	1.0	2.0	k $\Omega$

**Absolute Maximum Ratings**

$T_A = +25^\circ\text{C}$

Output Amplifier Supply Voltage, $V_{OD}$	-0.3 to +15 V
Reset Part Supply Voltage, $V_{RD}$	-0.3 to +15 V
Drive Unit Supply Voltage, $V+$	-0.3 to +15 V
Output Gate Voltage, $V_{OG}$	-0.3 to +15 V
Register Clock Signal Voltage, $V_{\phi 10}$	-0.3 to +15 V
Transfer Gate Clock Signal Voltage, $V_{\phi TGO}$	-0.3 to +15 V
Reset Gate Clock Signal Voltage, $V_{\phi RO}$	-0.3 to +15 V
Sample-and-Hold Clock Signal Voltage, $V_{\phi SHD}$	-0.3 to +15 V
Operating Temperature, $T_{OP}$	-25 to +55 $^\circ\text{C}$
Storage Temperature, $T_{STG}$	-40 to +100 $^\circ\text{C}$

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

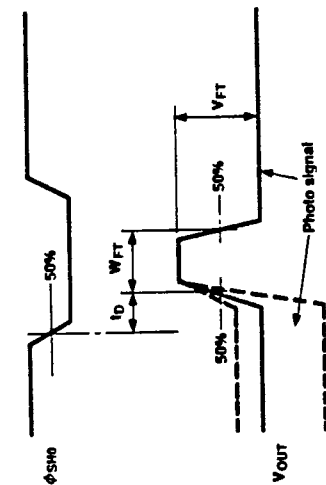
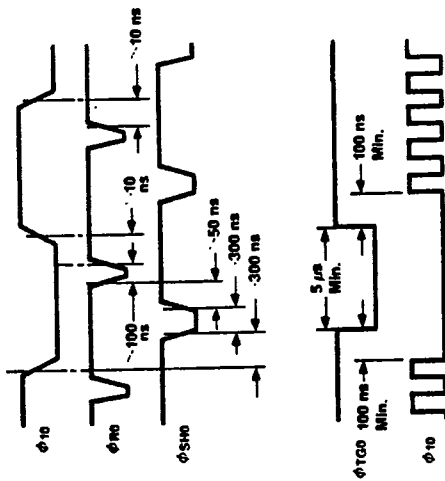
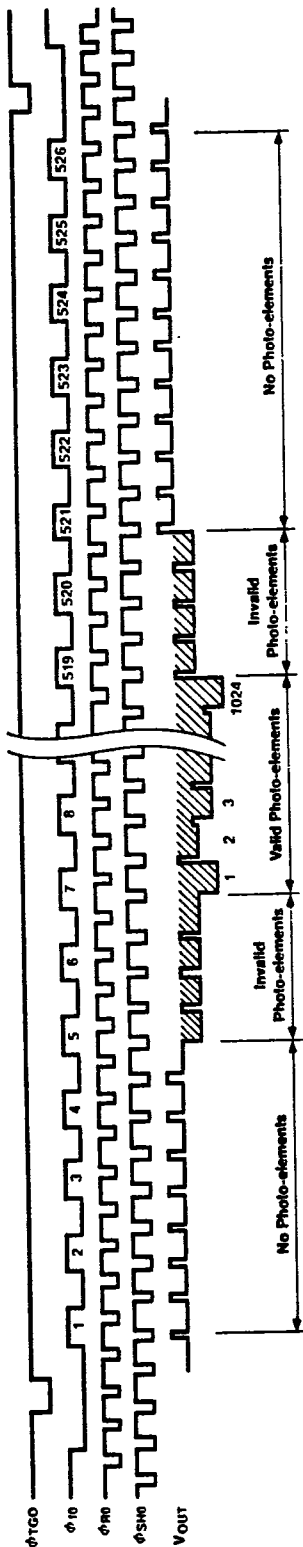
**Recommended Operating Conditions**

$T_A = -25$  to  $+55^\circ\text{C}$

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Output Amplifier Supply Voltage	$V_{OD}$	11.4	12.0	12.6	V
Reset Part Supply Voltage	$V_{RD}$	11.4	12.0	12.6	V
Drive Unit Supply Voltage	$V+$	11.4	12.0	12.6	V
Output Gate Bias Voltage	$V_{OG}$	1.0	1.25	1.50	V
Test Terminal G <sub>1</sub> Voltage	$V_{G1}$		0		V
Test Terminal G <sub>2</sub> Voltage	$V_{G2}$		0		V
Test Terminal I <sub>D</sub> Voltage	$V_{ID}$		12.0		V
Test Terminal $\phi_{IR}$ Voltage	$V_{\phi IR}$		0		V
High Level of Register Clock Signal	$V_{\phi 1H}$	2.4	4.5	5.5	V
Low Level of Register Clock Signal	$V_{\phi 1L}$	-0.3	0	0.5	V
High Level of Transfer Gate Clock Signal	$V_{\phi TGH}$	2.4	4.5	5.5	V
Low Level of Transfer Gate Clock Signal	$V_{\phi TGL}$	-0.3	0	0.5	V
High Level of Reset Gate Clock Signal	$V_{\phi RH}$	2.4	4.5	5.5	V
Low Level of Reset Gate Clock Signal	$V_{\phi RL}$	-0.3	0	0.5	V
High Level of Sample-and-Hold Clock Signal	$V_{\phi SHH}$	2.4	4.5	5.5	V
Low Level of Sample-and-Hold Clock Signal	$V_{\phi SHL}$	-0.3	0	0.5	V
Register Clock Signal Frequency	$f_{\phi 10}$		250	500	kHz
Reset Gate Clock Signal Frequency	$f_{\phi R0}$		500	1000	kHz

**μPD795**

**Timing Waveforms**



- The register clock signal φ10 should be not more than 526 cycles.
- Width of the transfer gate pulse φTGO should be less than 20 μs.

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## Definitions of Electrical Parameters

**Saturation Output Voltage [V<sub>SAT</sub>].** An output signal level above which the PRNU (photo-response non-uniformity) is ≥10% or the response is nonlinear.

**Saturation Exposure [SE].** Product of illuminance (lx) and exposure period (s) in which the output is saturated.

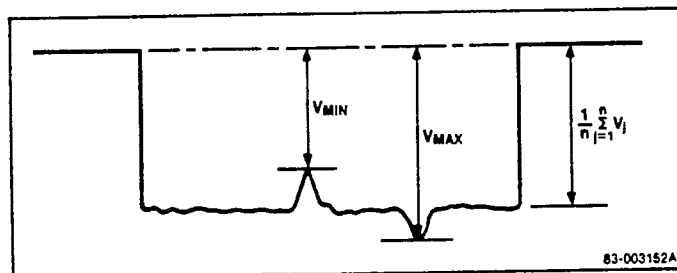
**Photo-Response Nonuniformity [PRNU].** Percentage of peak output level and bottom output level against average output level of all valid photo-elements in static and uniform light.

$$\text{PRNU (\%)} = \left( \frac{V_{\text{MAX or MIN}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

where

n = number of valid photo-elements

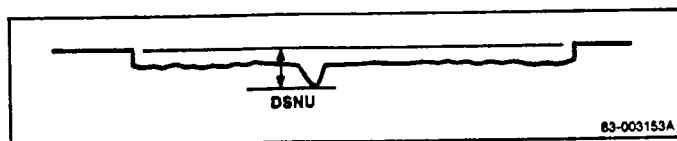
V<sub>j</sub> = output voltage of each photo element



**Average Dark Signal [ADS].** Average output level of valid photo-elements with no exposure.

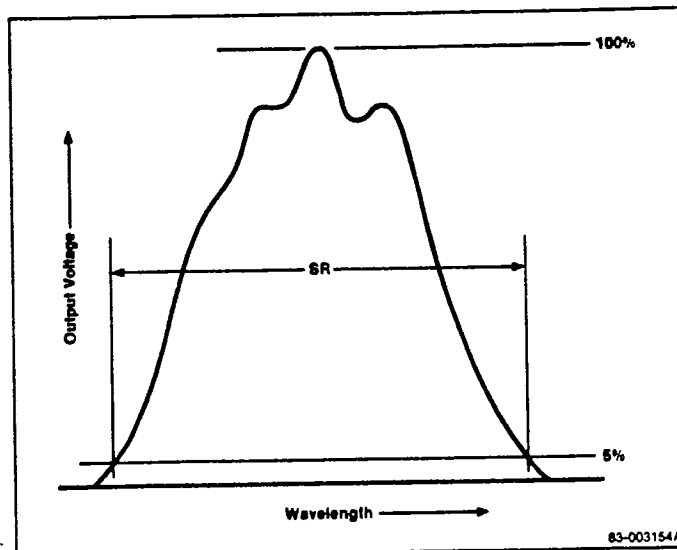
$$\text{ADS (mV)} = \frac{1}{n} \sum_{j=1}^n V_j$$

**Dark Signal Nonuniformity [DSNU].** Peak output level with no exposure.



**Working Power Consumption [P<sub>w</sub>].** Product of supply voltage and current when supply voltage is 12.0 V.

**Spectral Response Range Limits [SR].** Short side and long side limits of response spectral range having sensitivity above 5 percent of sensitivity of most sensitive wavelength.



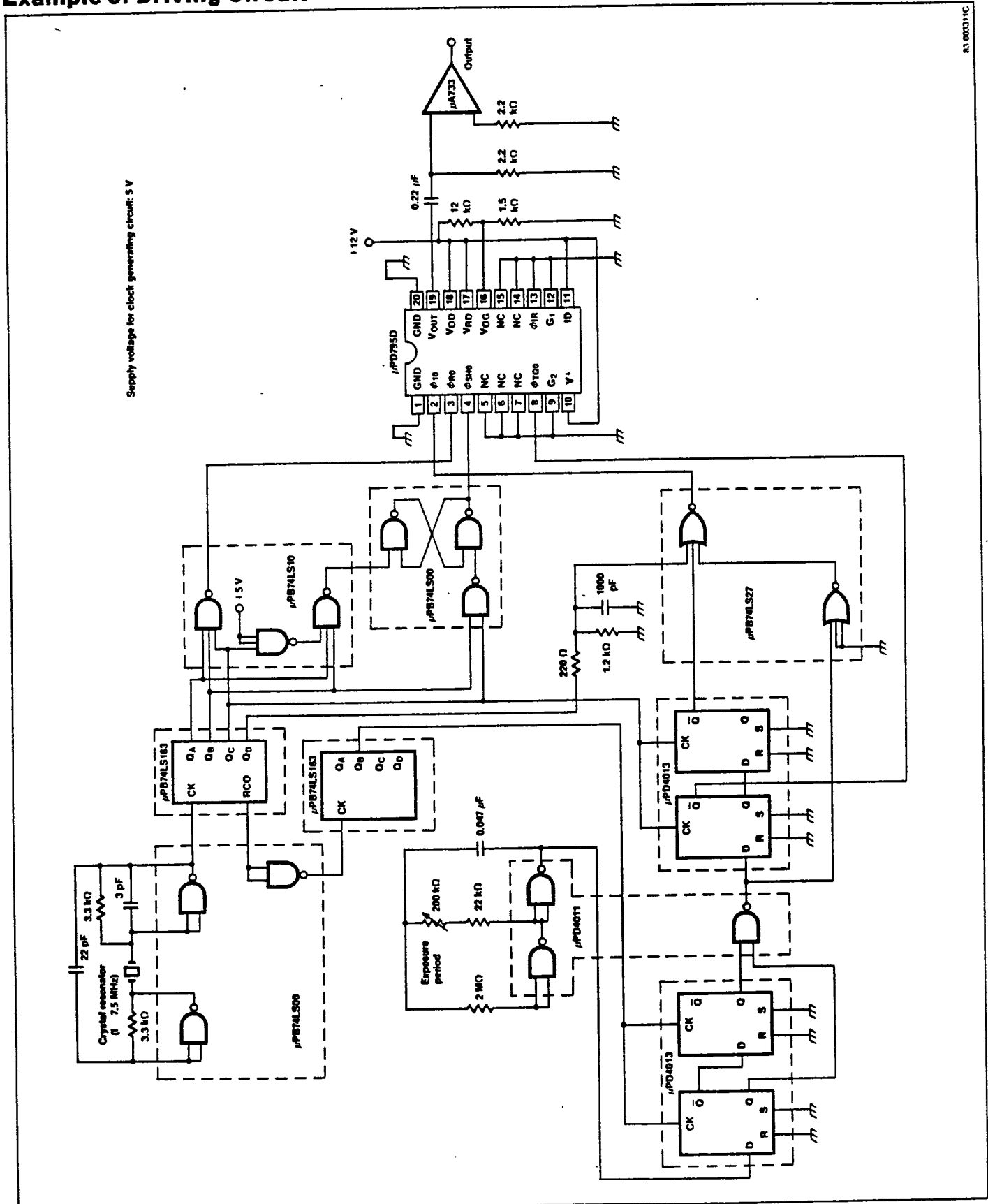
**Sensitivity [S].** Quotient of the output level divided by exposure (lx\*s).

**Offset Voltage [V<sub>OS</sub>].** Output terminal potential with no exposure.



# μPD795

## Example of Driving Circuit

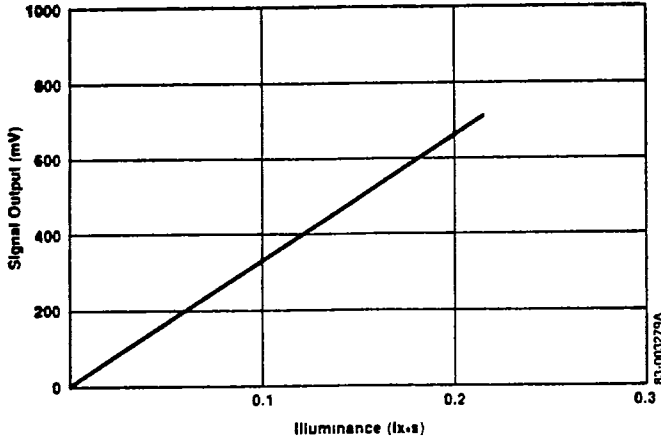


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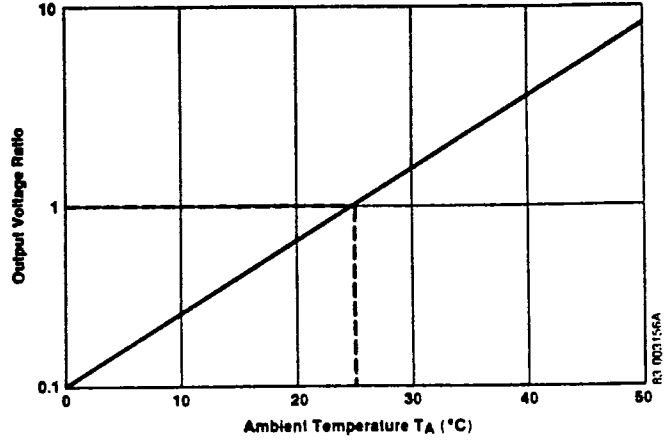
### Operating Characteristics

T<sub>A</sub> = 25°C

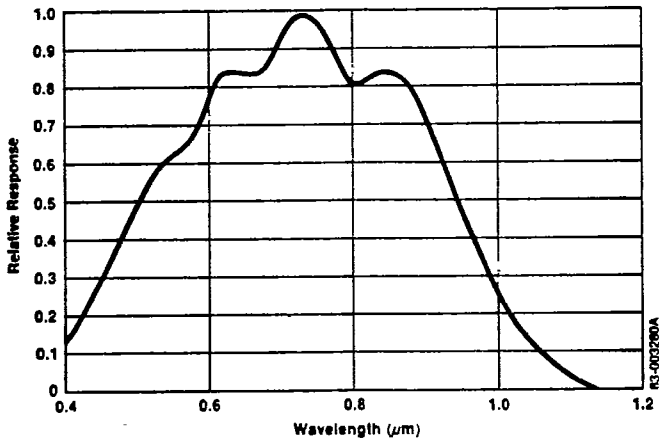
Signal Output



Dark Signal



Relative Spectrum Response



MTF

