SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

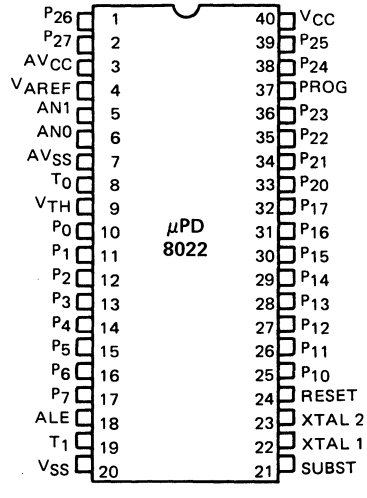
DESCRIPTION

The NEC μPD8022 is designed for low cost, high volume applications requiring large ROM space, analog to digital conversion capability, a capacitive touchpanel keyboard interface and/or a power line time base. The μPD8022 satisfies these requirements by integrating on one chip, an 8-bit μPD8021 type processor with 2K of ROM, a 2 channel 8-bit A/D converter, a high impedance comparator input port, and a zero crossing detector.

FEATURES

- 8-Bit Processor, ROM, RAM, I/O and Clock Generator
- Single +5V Supply (4.5V to 6.5V)
- NMOS Silicon Gate Technology
- 2K x 8 ROM, 64 x 8 RAM, 26 I/O Lines
- On Chip 8-Bit A/D Converter with 2 Input Channels
- 8.3 μs Instruction Cycle Timer
- Instructions are a Subset of μPD8048; Superset of μPD8021
- Internal Timer/Event Counter
- External and Timer/Counter Interrupts
- On-Chip Zero-Cross Detector
- High Impedance Comparator Port with Variable Threshold
- Clock Generator Using a Crystal or Single Inductor
- High Current Drive Capability on 2 I/O Pins
- Expandable I/O Utilizing the μPD8243
- Available in 40-Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



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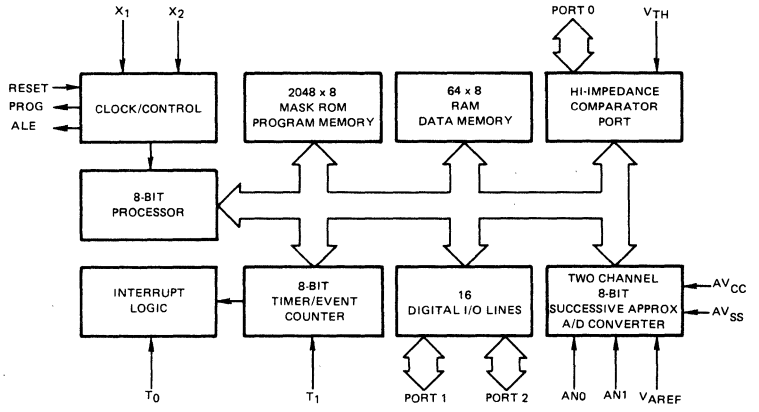
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Plastic Package) . . . . . -65°C to +125°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts①
Power Dissipation . . . . . 1 Watt

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	V_{TH} Floating
Input Low Voltage (Port 0)	V_{IL1}	-0.5		V_{TH}-0.1	V	
Input High Voltage (All except XTAL 1, RESET)	V_{IH}	2.0		V_{CC}	V	V_{CC} = 5.0V ± 10% V_{TH} Floating
Input High Voltage (All except XTAL 1, RESET)	V_{IH1}	3.0		V_{CC}	V	V_{CC} = 5.5V ± 1V V_{TH} Floating
Input High Voltage (Port 0)	V_{IH2}	V_{TH}+0.1		V_{CC}	V	
Input High Voltage (RESET, XTAL 1)	V_{IH3}	3.0		V_{CC}	V	
Port 0 Threshold Voltage	V_{TH}	0		0.4 V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			0.25	V	I_{OL} = 7 mA
Output High Voltage (All unless open drain option for Port 0)	V_{OH}	2.4			V	I_{OH} = 50 μA
Input Current (T1)	I_{L1}			±200	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Output Leakage Current (Open drain option for Port 0)	I_{L0}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
V_{CC} Supply Current	I_{CC}			100	mA	

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
8	T_0	Active low interrupt input if enabled. Also testable using the conditional jump instructions JTO and JNTO.
19	T_1	Zero-cross detector input. After executing a STRT CNT instruction this becomes the event counter input. Also testable using the conditional jump instructions JT1 and JNT1. Optional ROM mask pull-up resistor available.
6	AN0	Analog input to the A/D converter after execution of the SEL AN0 instruction.
5	AN1	Analog input to the A/D converter after execution of the SEL AN1 instruction.
22	XTAL 1	Input for internal oscillator connected to one side of a crystal or inductor. Serves as an external frequency input also (Non-TTL compatible V_{IH}).
23	XTAL 2	Input for internal oscillator connected to the other side of a crystal or inductor. This pin is not used when employing an external frequency source.
37	PROG	Strobe output for the μPD8243 I/O expander.
18	ALE	Active high address latch enable output occurring once every instruction cycle. Can be used as an output clock.
24	RESET	Active high input that initializes the processor to a defined state and starts the program at memory location zero.
40	V_{CC}	+5V power supply.
3	AV_{CC}	+5V A/D converter power supply.
20	V_{SS}	Power supply ground potential.
7	AV_{SS}	A/D converter power supply ground potential. Sets conversion range lower limit.
4	VA_{REF}	Reference voltage for A/D converter. Sets conversion range upper limit.
9	V_{TH}	Port 0 comparator threshold reference input.
21	SUBST	Substrate connection used with bypass capacitor to V_{SS} for substrate voltage stabilization and improvement of A/D accuracy.
10-17	P_{00}-P_{07}	Port 0. 8-bit open drain I/O port with comparator inputs. The reference threshold is set via V_{TH}. Optional ROM mask pull-up resistors available.
25-32	P_{10}-P_{17}	Port 1. 8-bit quasi-bidirectional port. TTL compatible.
1-2 33-36 38-39	P_{20}-P_{27}	Port 2. 8-bit quasi-bidirectional port. TTL compatible. P_{20}-P_{23} also function as an I/O expander port for the μPD8243.

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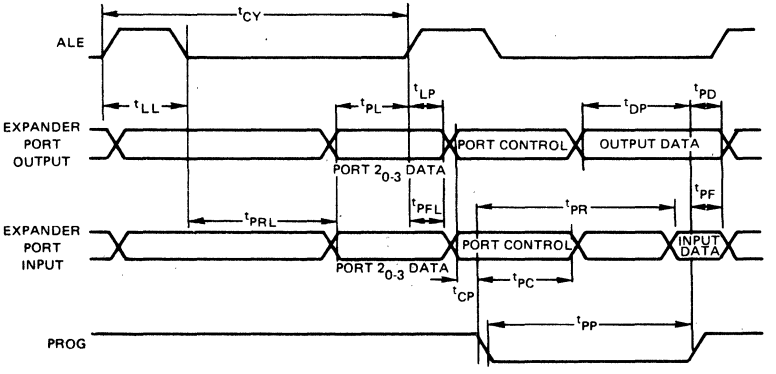
T_a = 0°C to 70°C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V

AC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Cycle Time	t_{CY}	8.38		50.0	μs	3.58 MHz XTAL for t_{CY} min.
Zero-Cross Detection Input (T1)	V_{T1}	1		3	VAC_{pp}	AC coupled
Zero-Cross Accuracy	A_{ZC}			±135	mV	60 Hz Sine Wave
Zero-Cross Detection Input Frequency (T1)	F_{T1}	0.06		1	kHz	
Port Control Setup Before Falling Edge of PROG	t_{CP}	0.5			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Port Control Hold After Falling Edge of PROG	t_{PC}	0.8			μs	t_{CY} = 8.38 μs, C_L = 80 pF
PROG to Time P2 Input Must be Valid	t_{PR}			1.0	μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Setup Time	t_{PP}	7.0			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Hold Time	t_{PD}	8.3			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Input Data Hold Time	t_{PF}	0		150	μs	t_{CY} = 8.38 μs, C_L = 80 pF
PROG Pulse Width	t_{PP}	8.3			μs	t_{CY} = 8.38 μs, C_L = 80 pF
ALE to Time P2 Input Must be Valid	t_{PRL}			3.6	μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Setup Time	t_{PL}	0.8			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Hold Time	t_{LP}	1.6			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Input Data Hold Time	t_{PFL}	0			μs	t_{CY} = 8.38 μs, C_L = 80 pF
ALE Pulse Width	t_{LL}	3.9		23.0	μs	t_{CY} = 8.38 μs for min.

TIMING WAVEFORM

PORT 2 TIMING



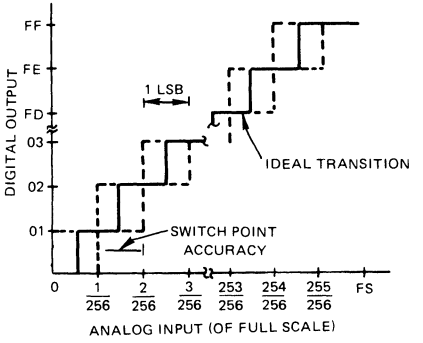
A/D CONVERTER CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$, $AV_{CC} = 5.5V \pm 1V$, $AV_{SS} = 0V$
$AV_{CC}/2 \leq V_{AREF} \leq AV_{CC}$

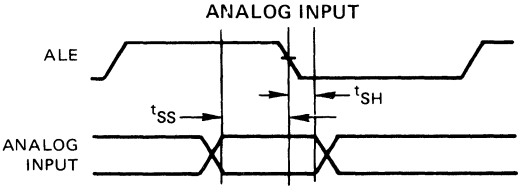
PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution		8			BITS	
Switch Point Accuracy	A_{SP}		±½		LSB	②
Absolute Accuracy	A_{AB}		±1		LSB	
Sample Setup Before Falling Edge of ALE	t_{SS}		0.20		t_{CY}	①
Sample Hold After Falling Edge of ALE	t_{SH}		0.10		t_{CY}	①
Input Capacitance (AN0, AN1)	C_{AD}		1		pF	
Conversion Time	t_{CNV}	4		4	t_{CY}	
Conversion Range		AV_{SS}		V_{AREF}	V	
Reference Voltage	V_{AREF}	$AV_{CC}/2$		AV_{CC}	V	

Note: ① The analog signal on AN0 and AN1 must remain constant during the sample time $t_{SS} + t_{SH}$.

②



TIMING WAVEFORM



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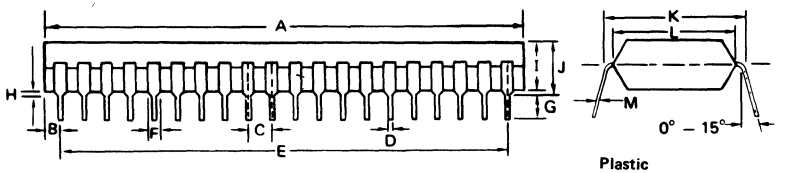
INSTRUCTION SET

The instruction set of the μPD8022 is a subset of the μPD8048 instruction set except for three instructions, SEL AN0, SEL AN1, and RAD, which are unique to the μPD8022. The μPD8022 instruction set is also a superset of the μPD8021, meaning that the μPD8022 will execute ALL of the μPD8021 instructions PLUS some additional instructions which are listed below. For a summary of the μPD8021 instruction set, please refer to that section. Symbols used below are defined in the same manner as in that section. Also note that the instructions listed below do not affect any status flags.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
JTO addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jump to specified address if T0 is high	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNTO addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jump to specified address if T0 is low	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
RAD	$(A) \leftarrow (CRR)$	Move to A the contents of the A/D conversion result register (CRR)	1	0	0	0	0	0	0	0	2	1
SEL AN0		Select AN0 as the input for the A/D converter	1	0	0	0	0	1	0	1	1	1
SEL AN1		Select AN1 as the input for the A/D converter	1	0	0	1	0	1	0	1	1	1
EN I		Enable the external interrupt input T0	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input T0	0	0	0	1	0	1	0	1	1	1
EN TCNTI		Enable internal timer/ counter interrupt	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal timer/ counter interrupt	0	0	1	1	0	1	0	1	1	1
RETI	$(SP) \leftarrow (SP) - 1$ $(PC) \leftarrow ((SP))$	Return from interrupt and re-enable interrupt input logic	1	0	0	1	0	0	1	1	2	1

PACKAGE OUTLINE μPD8022C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

8022DS-12-80-CAT