NEC Microcomputers, Inc.

NEC

µPD8085A
µPD8085A-2

µPD8085A SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

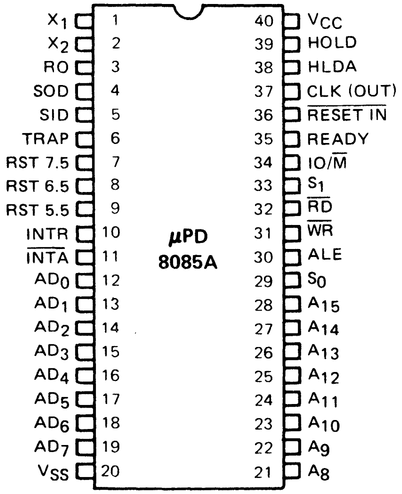
DESCRIPTION

The µPD8085A is a single chip 8-bit microprocessor which is 100 percent software compatible with the industry standard 8080A. It has the ability of increasing system performance of the industry standard 8080A by operating at a higher speed. Using the µPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count.

FEATURES

- Single Power Supply: +5 Volt, ±10%
- Internal Clock Generation and System Control
- Internal Serial In/Out Port.
- Fully TTL Compatible
- Internal 4-Level Interrupt Structure
- Multiplexed Address/Data Bus for Increased System Performance
- Complete Family of Components for Design Flexibility
- Software Compatible with Industry Standard 8080A
- Higher Throughput: µPD8085A – 3 MHz
  µPD8085A-2 – 5 MHz
- Available in Either Plastic or Ceramic Package

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL compatible.

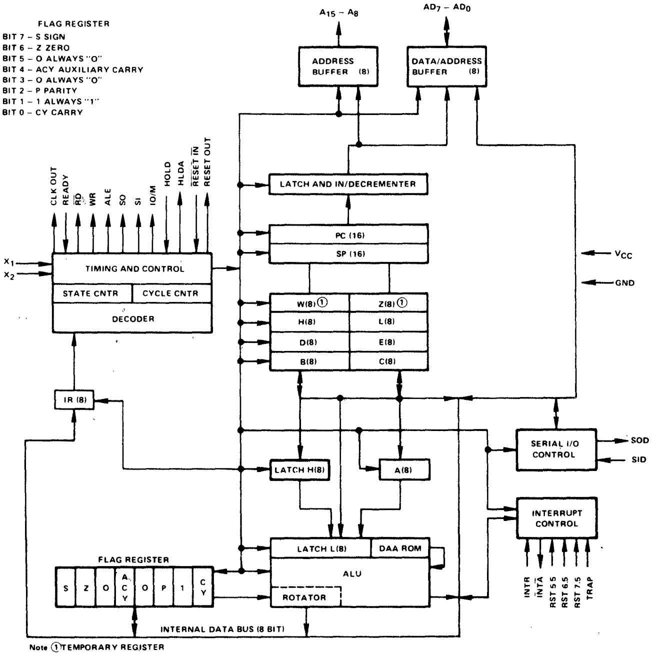
The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

BLOCK DIAGRAM



Note ①TEMPORARY REGISTER

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2	X_1, X_2	Crystal In	Crystal, RC, or external clock input
3	RO	Reset Out	Acknowledge that the processor is being reset to be used as a system reset
4	SOD	Serial Out Data	1-bit data out by the SIM instruction
5	SID	Serial In Data	1-bit data into ACC bit 7 by the RIM instruction
6	Trap	Trap Interrupt Input	Highest priority nonmaskable restart interrupt
7 8 9	RST 7.5 RST 6.5 RST 5.5	Restart Interrupts	Priority restart interrupt inputs, of which 7.5 is the highest and 5.5 the lowest priority
10	INTR	Interrupt Request In	A general interrupt input which stops the PC from incrementing, generates $\overline{\text{INTA}}$, and samples the data bus for a restart or call instruction
11	$\overline{\text{INTA}}$	Interrupt Acknowledge	An output which indicates that the processor has responded to INTR
12-19	$AD_0 - AD_7$	Low Address/Data Bus	Multiplexed low address and data bus
20	V_{SS}	Ground	Ground Reference
21-28	$A_8 - A_{15}$	High Address Bus	Nonmultiplexed high 8-bits of the address bus
29, 33	S_0, S_1	Status Outputs	Outputs which indicate data bus status: Halt, Write, Read, Fetch
30	ALE	Address Latch Enable Out	A signal which indicates that the lower 8-bits of address are valid on the AD lines
31, 32	$\overline{\text{WR}}$, $\overline{\text{RD}}$	Write/Read Strobes Out	Signals out which are used as write and read strobes for memory and I/O devices
34	IO/$\overline{\text{M}}$	I/O or Memory Indicator	A signal out which indicates whether $\overline{\text{RD}}$ or $\overline{\text{WR}}$ strobes are for I/O or memory devices
35	Ready	Ready Input	An input which is used to increase the data and address bus access times (can be used for slow memory)
36	$\overline{\text{Reset In}}$	Reset Input	An input which is used to start the processor activity at address 0, resetting IE and HLDA flip-flops
37	CLK	Clock Out	System Clock Output
38, 39	HLDA, HOLD	Hold Acknowledge Out and Hold Input Request	Used to request and indicate that the processor should relinquish the bus for DMA activity. When hold is acknowledged, $\overline{\text{RD}}$, $\overline{\text{WR}}$, IO/$\overline{\text{M}}$, Address and Data busses are all 3-stated.
40	V_{CC}	5V Supply	Power Supply Input

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
(Plastic Package)	−40°C to +125°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts
Power Dissipation	1.5W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = GND, unless otherwise specified

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	V_{SS} − 0.5		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA on all outputs
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μs ①
Power Supply Current (V_{CC})	I_{CC} (AV)			170	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ①	μA	V_{IN} = V_{CC}
Output Leakage	I_{LO}			±10 ①	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
Input Low Level, Reset	V_{ILR}	−0.5		+0.8	V	
Input High Level, Reset	V_{IHR}	2.4		V_{CC} + 0.5	V	
Hysteresis, Reset	V_{HY}	0.25			V	

Note: ① Minus (−) designates current flow out of the device.

AC CHARACTERISTICS

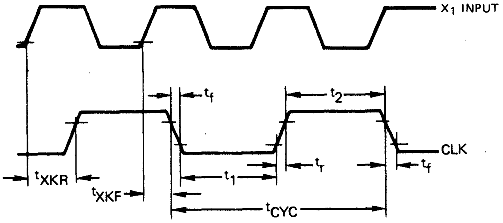
T_a = 0°C to + 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS µPD8085A MIN	LIMITS µPD8085A MAX	LIMITS µPD8085A-2 MIN	LIMITS µPD8085A-2 MAX	UNIT	TEST CONDITIONS
CLK Cycle Period	T_{CYC}	320	2000	200	2000	ns	
CLK Low Time	t_1	80		40		ns	
CLK High Time	t_2	120		70		ns	
CLK Rise and Fall Time	t_r, t_f		30		30	ns	T_{CYC} = 320 ns
Address Valid Before Trailing Edge of ALE	t_{AL}	110		50		ns	C_L = 150 pF
Address Hold Time After ALE	t_{LA}	100		50		ns	
ALE Width	t_{LL}	140		80		ns	
ALE Low During CLK High	t_{LCK}	100		50		ns	Output Voltages
Training Edge of ALE to Leading Edge of Control	t_{LC}	130		60		ns	V_L = 0.8 Volts V_H = 2.0 Volts
Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)	t_{AFR}		0		0	ns	
Valid Address to Valid Data In	t_{AD}		575		350	ns	Input Voltages
$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	t_{RD}		300		150	ns	V_L = 0.8 Volts
Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	t_{RDH}	0		0		ns	V_H = 1.5 Volts at
Training Edge of READ to Re-Enabling of Address	t_{RAE}	150		90		ns	20 ns rise and fall times
Address (A_8-A_{15}) Valid After Control ①	t_{CA}	120		60		ns	For outputs where
Data Valid to Training Edge of $\overline{WRITE}$	t_{DW}	420		230		ns	C_L = 150 pf, correct
Data Valid After Training Edge of $\overline{WRITE}$	t_{WD}	100		60		ns	as follows:
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400		230		ns	25 pf ≤ CL < 150 pf –0.10 ns/pf
Training Edge of Control to Leading Edge of ALE	t_{CL}	50		25		ns	
READY Valid from Address Valid	t_{ARY}		220		100	ns	150 pf < CL ≤
READY Setup Time to Leading Edge of CLK	t_{RYS}	110		100		ns	300 pf + 0.30 ns/pf
READY Hold Time	t_{RYH}	0		0		ns	
HLDA Valid to Training Edge of CLK	t_{HACK}	110		40		ns	Outputs measured
Bus Float After HLDA	t_{HABF}		210		150	ns	with only
HLDA to Bus Enable	t_{HABE}		210		150	ns	capacitive load
ALE to Valid Data In	t_{LDR}		460		270	ns	
Control Training Edge to Leading Edge of Next Control	t_{RV}	400		220		ns	
Address Valid to Leading Edge of Control	t_{AC}	270		115		ns	
HOLD Setup Time to Training Edge of CLK	t_{HDS}	170		120		ns	
HOLD Hold Time	t_{HDH}	0		0		ns	
INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	t_{INS}	160		150		ns	
INTR Hold Time	t_{INH}	0		0		ns	
X_1 Falling to CLK Rising	t_{XKR}	30	120	30	100	ns	
X_1 Falling to CLK Falling	t_{XKF}	30	150	30	110	ns	
Leading Edge of Write to Data Valid	t_{WDL}		40		20		

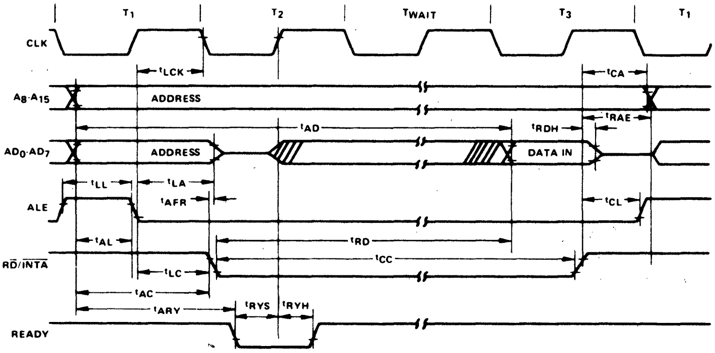
Note: ① IO/$\overline{M}$, SO, SI

TIMING WAVEFORMS

CLOCK TIMING

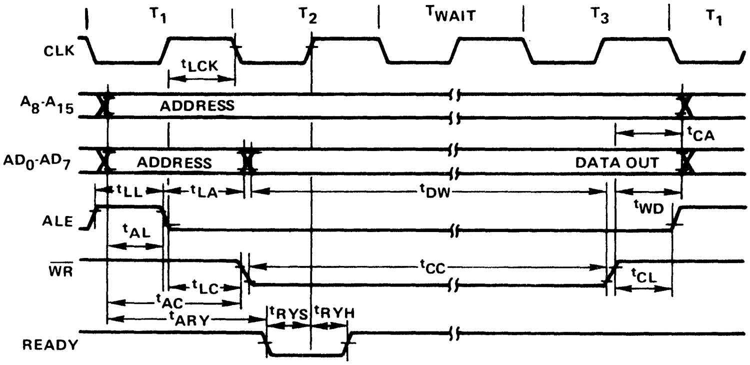


READ OPERATION

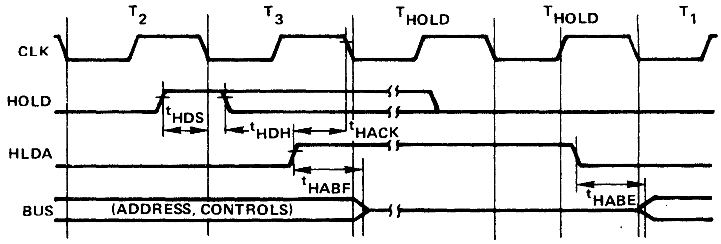


TIMING WAVEFORMS (CONT.)

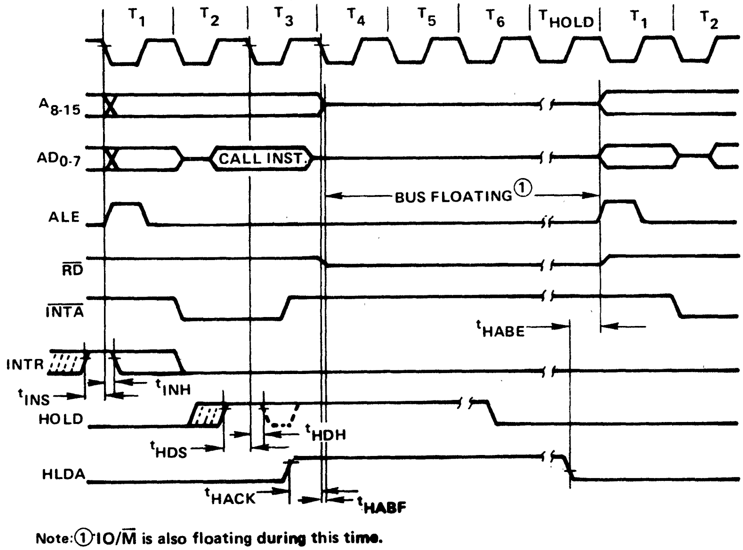
WRITE OPERATION



HOLD OPERATION

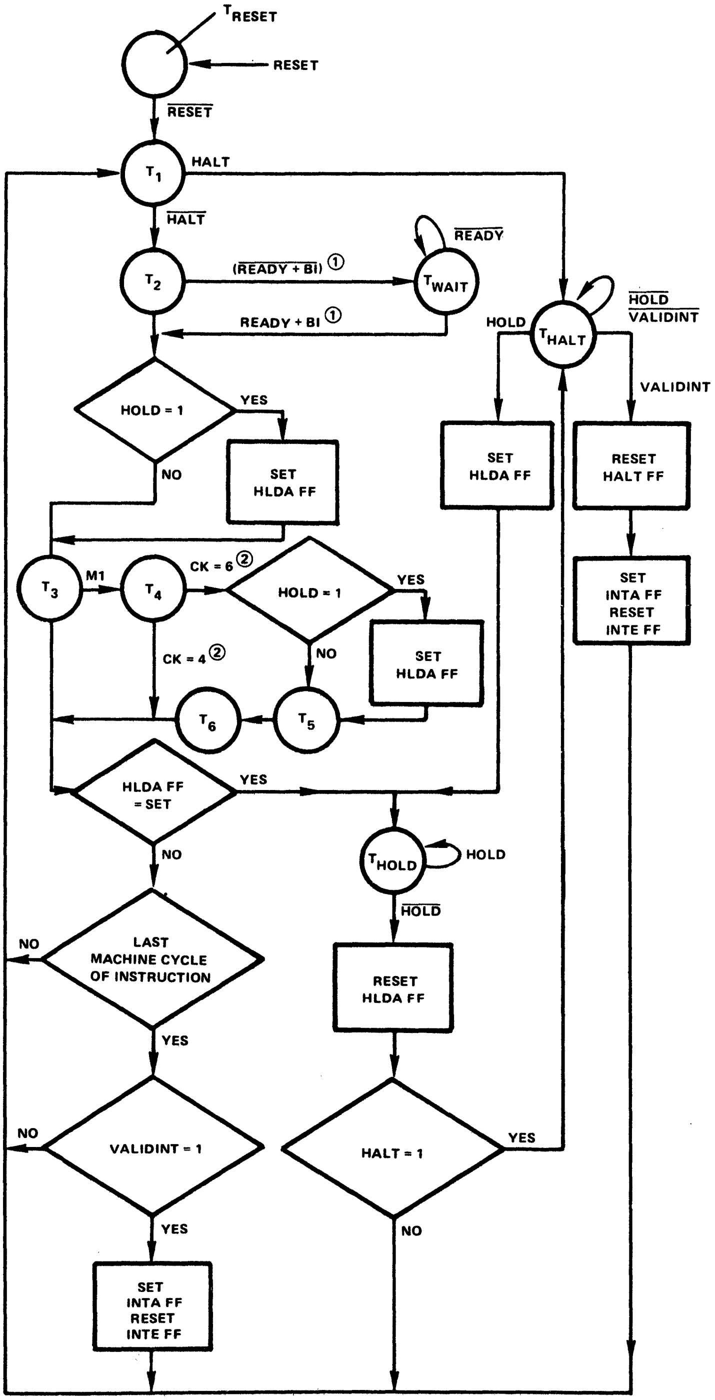


INTERRUPT TIMING



Note:① IO/M̄ is also floating during this time.

PROCESSOR STATE TRANSITION DIAGRAM



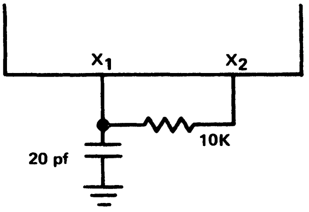
Notes: ① BI indicates that the bus is idle during this machine cycle.

② CK indicates the number of clock cycles in this machine cycle.

CLOCK INPUTS ①

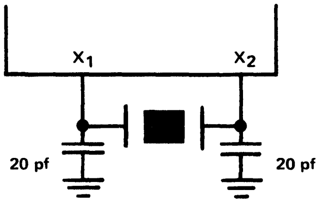
As stated, the timing for the μPD8085A may be generated in one of three ways; crystal, RC, or external clock. Recommendations for these methods are shown below.

RC



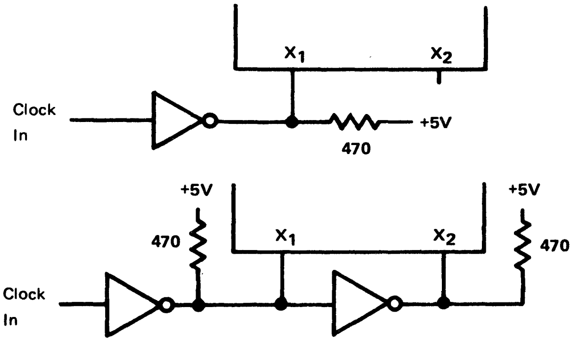
≈3 MHz Input Frequency
RC Resonance

CRYSTAL



1-6 MHz Input Frequency
Parallel Resonant Crystal

EXTERNAL



1-6 MHz 25-50% DC
X_2 not used

1-6 MHz > 50% DC

Note: ① Input frequency must be twice the internal operating frequency.

STATUS OUTPUTS

The Status Outputs are valid during ALE time and have the following meaning:

	S1	S0
Halt	0	0
Write	0	1
Read	1	0
Fetch	1	1

These pins may be decoded to portray the processor's data bus status.

INTERRUPTS

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5 and 7.5, and TRAP, a nonmaskable restart.

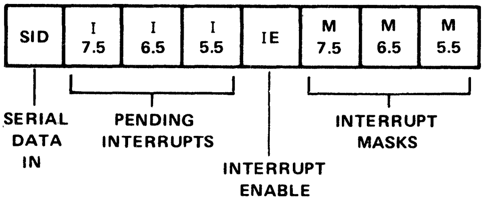
PRIORITY	INTERRUPT	RESTART ADDRESS
Highest	TRAP	24_{16}
|	RST 7.5	$3C_{16}$
|	RST 6.5	34_{16}
|	RST 5.5	$2C_{16}$
Lowest	INTR	

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising edge. TRAP, the highest priority interrupt, is nonmaskable and is set on the rising edge or positive level. It must make a low to high transition and remain high to be seen, but it will not be generated again until it makes another low to high transition.

SERIAL I/O

Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

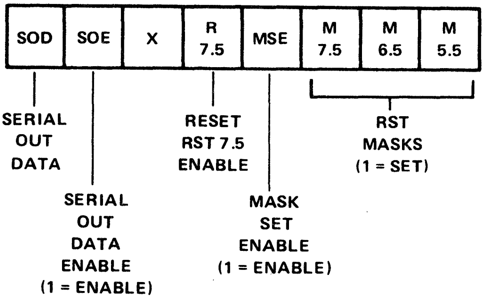
The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:



SID	I 7.5	I 6.5	I 5.5	IE	M 7.5	M 6.5	M 5.5

Note: After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:



SOD	SOE	X	R 7.5	MSE	M 7.5	M 6.5	M 5.5

SERIAL OUT DATA
SERIAL OUT DATA ENABLE (1 = ENABLE)
RESET RST 7.5 ENABLE
MASK SET ENABLE (1 = ENABLE)
RST MASKS (1 = SET)

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the µPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the µPD8085A. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the µPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

The special instruction group completes the µPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the µPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
MSB			DATA WORD				LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

									TYPICAL INSTRUCTIONS
One Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Register to register, memory reference, arithmetic or logical rotate, return, push, pop, enable, or disable interrupt instructions
Two Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Immediate mode or I/O instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND	
Three Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Jump, call or direct load and store instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2	

INSTRUCTION SET TABLE

		INSTRUCTION CODE[2]									FLAGS[4]			
MNEMONIC[1]	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	4				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	4	●	●	●	
DCR d	Decrement register	0	0	d	d	d	1	0	1	4	●	●	●	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	●	●	●	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	●	●	●	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	●	●	●	●
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	●	●	●	●
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	●	●	●	●
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	●	●	●	●
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	●	●	●	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	●	●	●	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	●	●	●	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	●	●	●	●
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	●	●	●	●
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	●	●	●	●
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	●	●	●	●
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	●	●	●	●
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	●	●	●	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	●	●	●	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	●	●	●	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	●	●	●	●
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	●	●	●	●
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	●	●	●	●
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	●	●	●	●
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	●	●	●	●
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	●	●	●	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	●	●	●	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	●	●	●	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	●	●	●	●
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				●
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				●
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				●
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				●
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	7/10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	7/10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	7/10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	7/10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	7/10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	7/10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	7/10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	7/10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	18				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	9/18				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	9/18				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	9/18				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	9/18				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	9/18				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	9/18				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	9/18				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	9/18				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	6/12				
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12				
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12				
RC	Return on carry	1	1	0	1	1	0	0	0	6/12				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12				
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12				
RP	Return on positive	1	1	1	1	0	0	0	0	6/12				
RM	Return on minus	1	1	1	1	1	0	0	0	6/12				

		INSTRUCTION CODE[2]									FLAGS[4]			
MNEMONIC[1]	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	12				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	12				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	12				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	●	●	●	●
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				●
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				●
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				●
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				●
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	6				
INX D	Increment DE	0	0	0	1	0	0	1	1	6				
INX H	Increment HL	0	0	1	0	0	0	1	1	6				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	6				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	6				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	6				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	6				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	6				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	16				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	6				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	6				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4				
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4				
RST A	Restart	1	1	A	A	A	1	1	1	12				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				$\overline{Cy}$
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	●	●	●	●
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	5				

Notes

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101L – 110 Memory – 111 A

[3] Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags.

[4] ● = flag affected
- flag not affected
0 = flag reset
1 = flag set

INSTRUCTION CYCLE TIMES

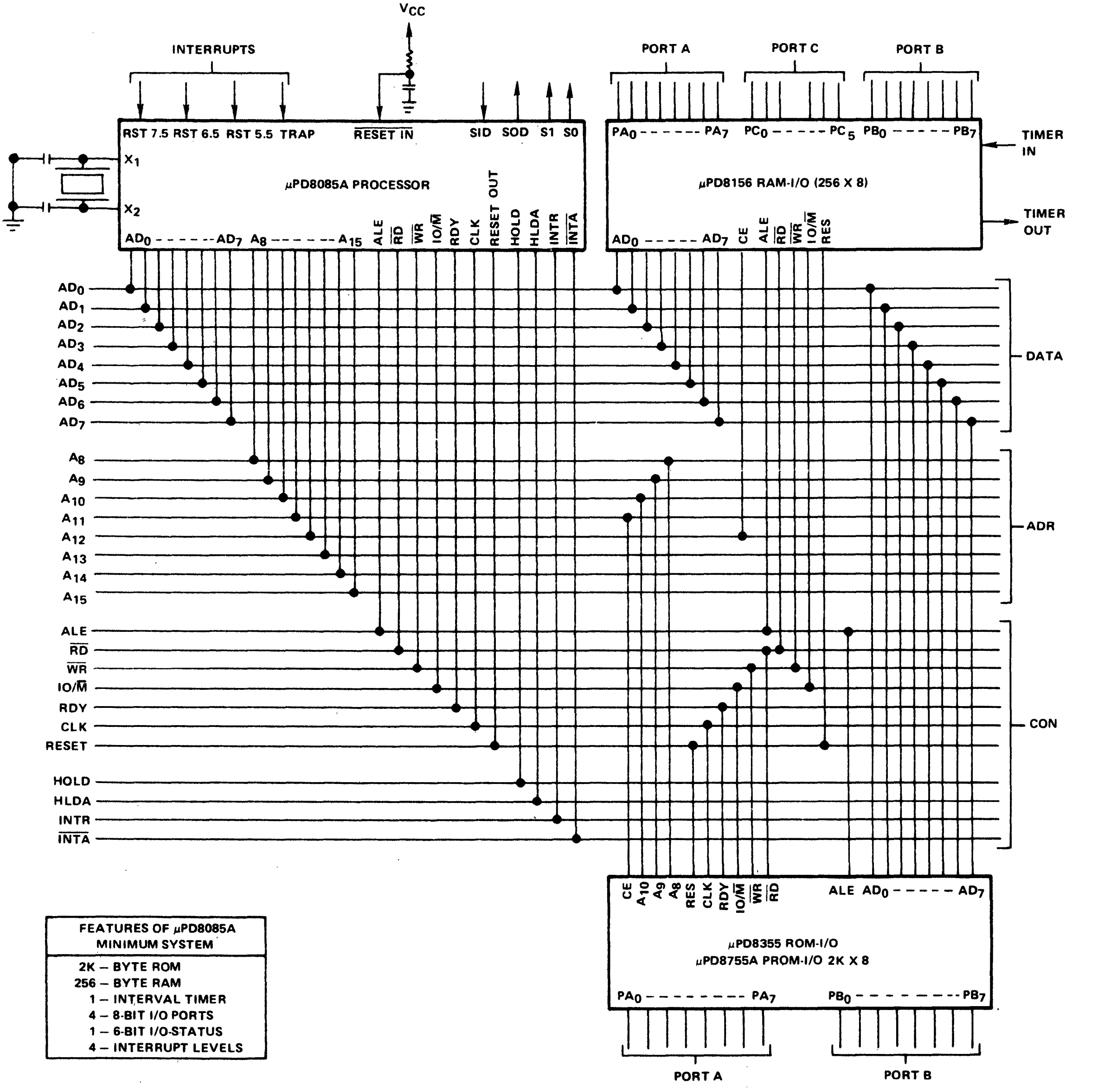
One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$).

Machine cycles and clock states used for each type of instruction are shown below.

INSTRUCTION TYPE	MACHINE CYCLES EXECUTED MIN/MAX	CLOCK STATUS MIN/MAX
ALU R	1	4
CMC	1	4
CMA	1	4
DAA	1	4
DCR R	1	4
DI	1	4
EI	1	4
INR R	1	4
MOV R, R	1	4
NOP	1	4
ROTATE	1	4
RIM	1	4
SIM	1	4
STC	1	4
XCHG	1	4
HLT	1	5
DCX	1	6
INX	1	6
PCHL	1	6
RET COND.	1/3	6/12
SPHL	1	6
ALU I	2	7
ALU M	2	7
JNC	2/3	7/10
LDAX	2	7
MVI	2	7
MOV M, R	2	7
MOV R, M	2	7
STAX	2	7
CALL COND.	2/5	9/18
DAD	3	10
DCR M	3	10
IN	3	10
INR M	3	10
JMP	3	10
LOAD PAIR	3	10
MVI M	3	10
OUT	3	10
POP	3	10
RET	3	10
PUSH	3	12
RST	3	12
LDA	4	13
STA	4	13
LHLD	5	16
SHLD	5	16
XTHL	5	16
CALL	5	18

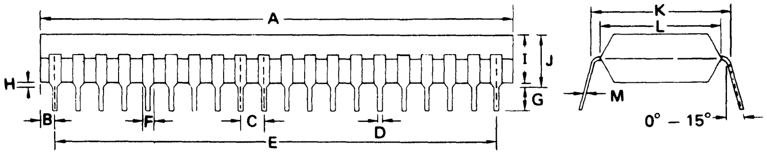
μPD8085A FAMILY MINIMUM SYSTEM CONFIGURATION

A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3-40 pin packs. This system is shown below with its address, data, control busses and I/O ports.



FEATURES OF μPD8085A MINIMUM SYSTEM
2K – BYTE ROM
256 – BYTE RAM
1 – INTERVAL TIMER
4 – 8-BIT I/O PORTS
1 – 6-BIT I/O-STATUS
4 – INTERRUPT LEVELS

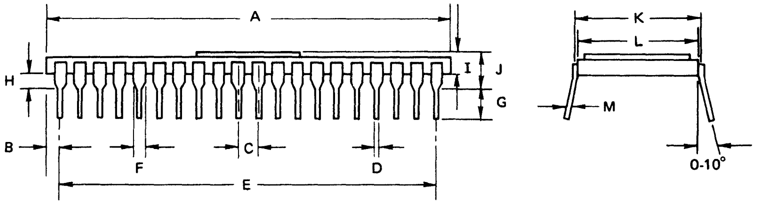
PACKAGE OUTLINE
μPD8085AC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25\,^{+0.1}_{\quad 0.05}$	$0.010\,^{+0.004}_{\quad 0.002}$

μPD8085AD



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Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019