PROGRAMMABLE DMA CONTROLLER

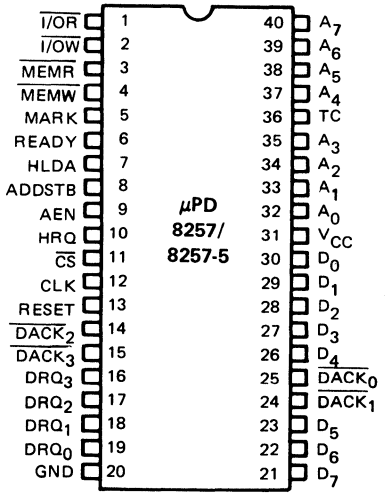
DESCRIPTION

The μPD8257-5 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the μPD8257-5 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the μPD8257-5 so that the system bus may be acquired by the generation of a single HOLD command to the 8080A. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other μPD8257-5 devices for systems requiring more than four DMA channels.

FEATURES

- NEC Now Supplies μPD8257-5 to μPD8257 Requirements
- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply ±10%
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

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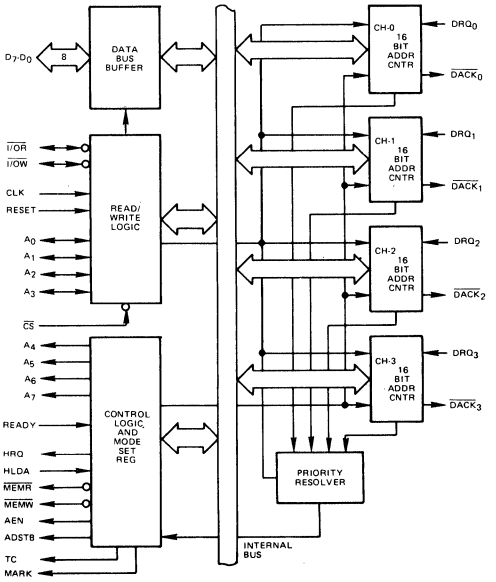
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①
Power Dissipation . . . . . 1 Watt

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10% GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Low Voltage	V_{IL}	-0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	I_{OH} = -150 μA for AB, DB and AEN I_{OH} = -80 μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	I_{OH} = -80 μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC}
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT} ①

Note: ① $V_{CC} > V_{OUT} > GND + 0.45V$

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

T_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V ①

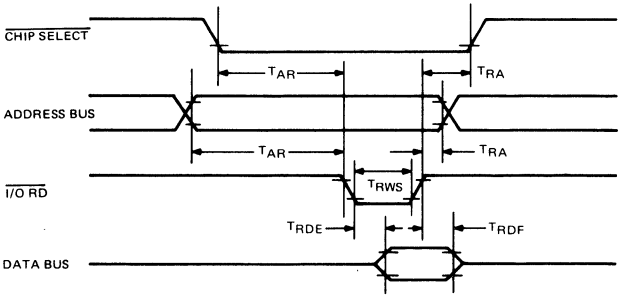
PARAMETER	SYMBOL	② LIMITS μPD8257 MIN	TYP	MAX	μPD8257-5 MIN	TYP	MAX	UNIT	TEST CONDITIONS
READ									
Adr or $\overline{CS}\downarrow$ Setup to $\overline{Rd}\downarrow$	T_{AR}	0			0			ns	
Adr or $\overline{CS}\uparrow$ Hold from $\overline{Rd}\uparrow$	T_{RA}	0			0			ns	
Data Access from $\overline{Rd}\downarrow$	T_{RDE}	0		300	0		170	ns	C_L = 100 pF
DB→Float Delay from $\overline{Rd}\uparrow$	T_{RDF}	20		150	20		100	ns ns	C_L = 100 pF C_L = 15 pF
$\overline{Rd}$ Width	T_{RW}	250			250			ns	
WRITE									
$\overline{CS}\downarrow$ Setup to $\overline{Wr}\downarrow$	T_{CW}	300			300			ns	
$\overline{CS}\uparrow$ Hold from $\overline{Wr}\uparrow$	T_{WC}	20			20			ns	
Adr Setup to $\overline{Wr}\downarrow$	T_{AW}	20			20			ns	
Adr Hold from $\overline{Wr}\uparrow$	T_{WA}	0			0			ns	
Data Setup to $\overline{Wr}\downarrow$	T_{DW}	200			200			ns	
Data Hold from $\overline{Wr}\uparrow$	T_{WD}	0			0			ns	
Wr Width	T_{WWS}	200			200			ns	
OTHER TIMING									
Reset Pulse Width	T_{RSTW}	300			300			ns	
Power Supply ↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			500			μs	
Signal Rise Time	T_r			20			20	ns	
Signal Fall Time	T_f			20			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			2			t_{CY}	

Note: ① All timing measurements are made at the following reference voltages unless specified otherwise. Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

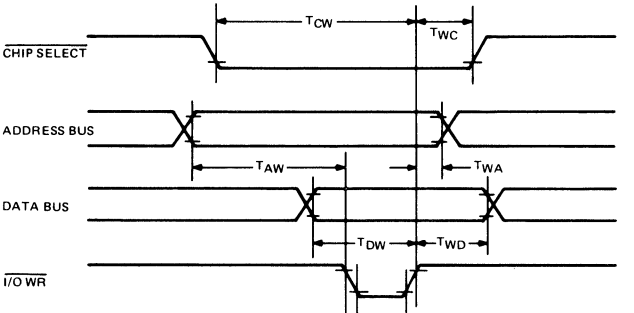
② Data for comparison only.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

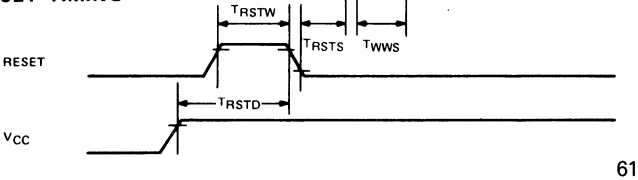
READ TIMING



WRITE TIMING



RESET TIMING



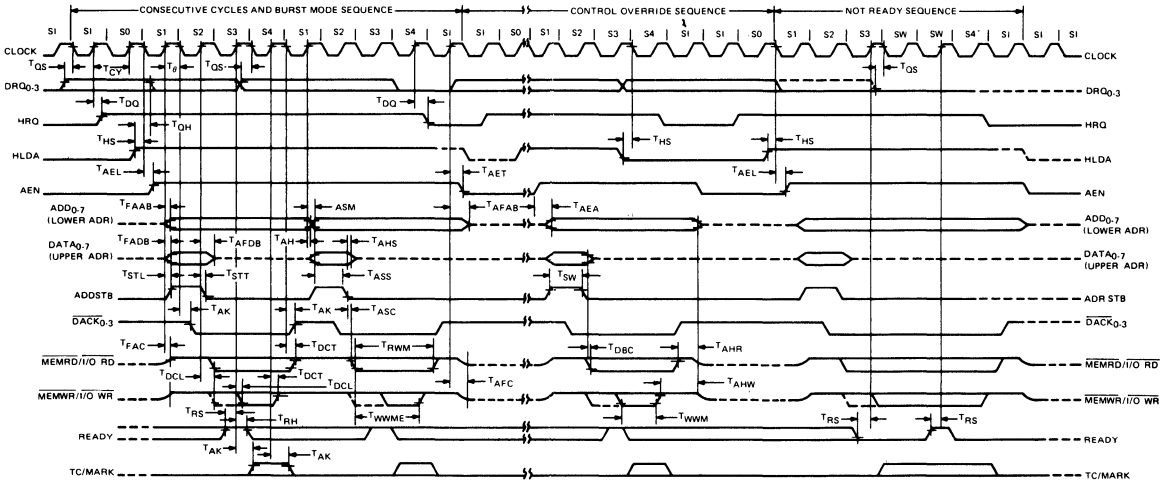
AC CHARACTERISTICS DMA (MASTER) MODE

T_a = 0°C to 70°C; V_{CC} = +5V ± 10%; GND = 0V

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		⑧ μPD8257		μPD8257-5			
		MIN	MAX	MIN	MAX		
Cycle Time (Period)	T_{CY}	0.320	4	0.250	4	μs	
Clock Active (High)	T_θ	120	.8T_{CY}	30	.8T_{CY}	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	120		120			
DRQ↓ Hold from HLDA↑	T_{QH}	0		0			④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}		160		160	ns	①
HRQ↑ or ↓ Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}		250		250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100		100		ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}		300		250	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}		200		200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20		20		ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}		250		250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}		150		150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}		250		250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	T_{ASM}−50		T_{ASM}−50			②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1, SI)	T_{AHR}	60		60		ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300		300		ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}		300		250	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}+20	250	T_{STT}+20	170	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100		100		ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50		50		ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}		200		200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}		140		140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	T_{CY}−100		T_{CY}−100		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70		70		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20		20		ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark ↑ Delay from θ↑ (S3) and TC/Mark ↓ Delay from θ↑ (S4)	T_{AK}		250		250	ns	① ⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}		200		200	ns	② ⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}		200		200	ns	② ⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}		300		250	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}		150		150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}$+ T_θ−50		$2T_{CY}$+ T_θ−50		ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	T_{CY}−50		T_{CY}−50		ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}$−50		$2T_{CY}$−50		ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30		30		ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20		20		ns	

Notes: ① Load = 1 TTL
② Load = 1 TTL + 50 pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ ΔT_{AK} <50 ns
⑥ ΔT_{DGL} <50 ns
⑦ ΔT_{DCT} <50 ns
⑧ Data for comparison only

TIMING WAVEFORMS
DMA (MASTER) MODE



FUNCTIONAL DESCRIPTION

The μPD8257-5 is a programmable, Direct Memory Address (DMA) device. When used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080A/8085A based systems. Once initialized by an 8080A/8085A CPU, the μPD8257-5 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occurs within the μPD8257-5.

- It acquires control of the system bus (placing 8080A/8085A in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16-bit memory address word is generated with the aid of an 8212 in the following manner:

  The μPD8257-5 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The μPD8257-5 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The μPD8257-5 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read, which causes data to be transferred from memory to a peripheral;
- DMA write, which causes data to be transferred from a peripheral to memory; and
- DMA verify, which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the μPD8257-5. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

DMA OPERATION

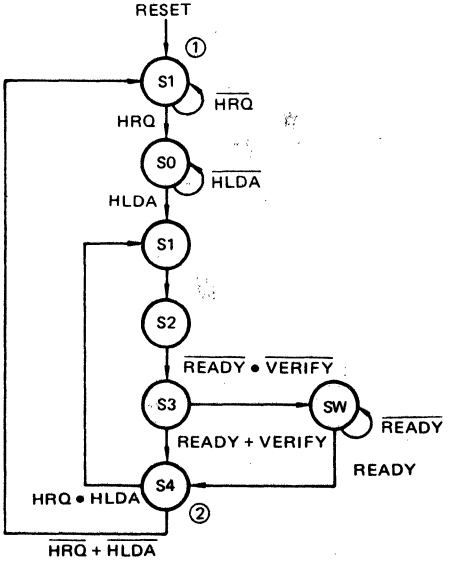
Internally the μPD8257-5 contains six different states (S0, S1, S2, S3, S4 and SW). The duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the μPD8257-5 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080A/8085A and the μPD8257-5 waits in S0 until the 8080A/8085A issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK}_n$) with the highest priority is driven low, selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK}_n$) or both $\overline{DACK}_n$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst model).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the μPD8257-5 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the μPD8257-5 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the μPD8257-5 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the μPD8257-5 and the 8080A/8085A.

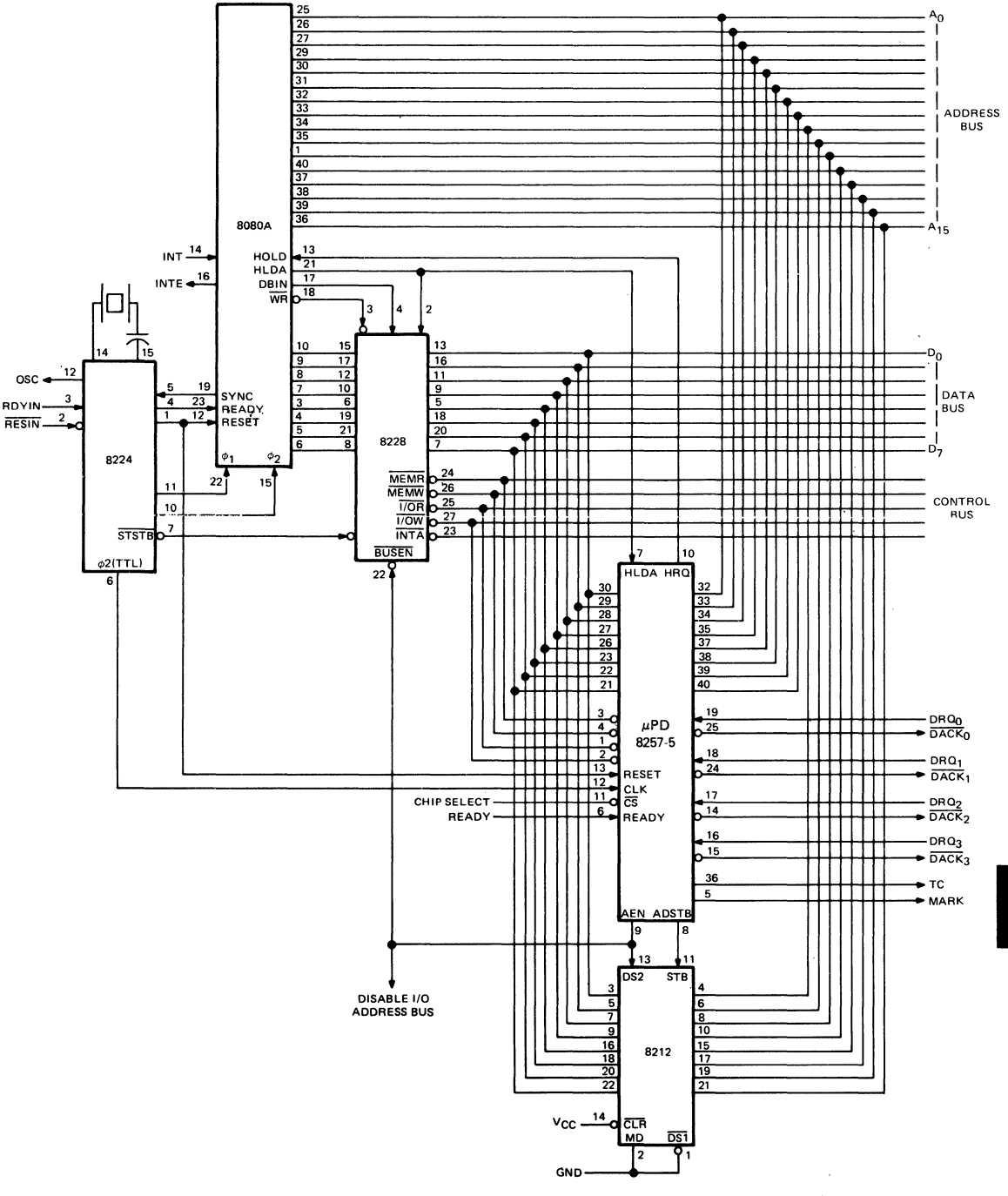
During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

DMA OPERATION STATE DIAGRAM



Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

TYPICAL μPD8257-5
SYSTEM INTERFACE SCHEMATIC



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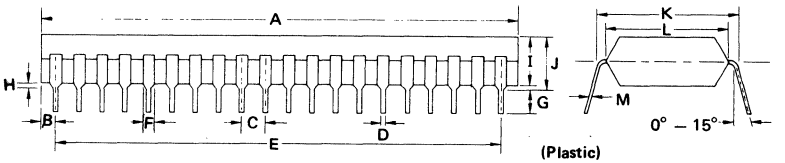
PACKAGE OUTLINE
μPD8257C
μPD8257C-5



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$