NEC Microcomputers, Inc.

NEC

μPD8259A
μPD8259A-2

PROGRAMMABLE INTERRUPT CONTROLLER

DESCRIPTION

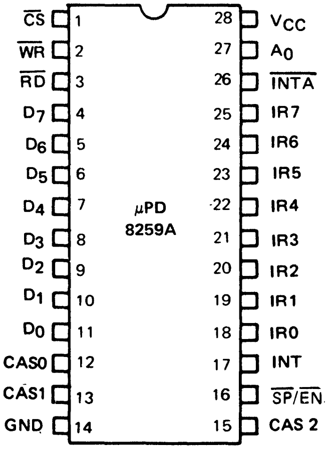
The NEC μPD8259A is a programmable interrupt controller directly compatible with the 8080A/8085A/8086/8088 microprocessors. It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to 64 levels with the addition of other μPD8259As. The user is offered a selection of priority algorithms to tailor the priority processing to meet his system requirements. These can be dynamically modified during operation, expanding the versatility of the system.

The μPD8259A is completely upward compatible with the μPD8259-5, so software written for the μPD8259-5 will run on the μPD8259A.

FEATURES

- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Full Compatibility with 8080A/8085A/8086/8088
- Available in 28 Pin Plastic and Ceramic Packages

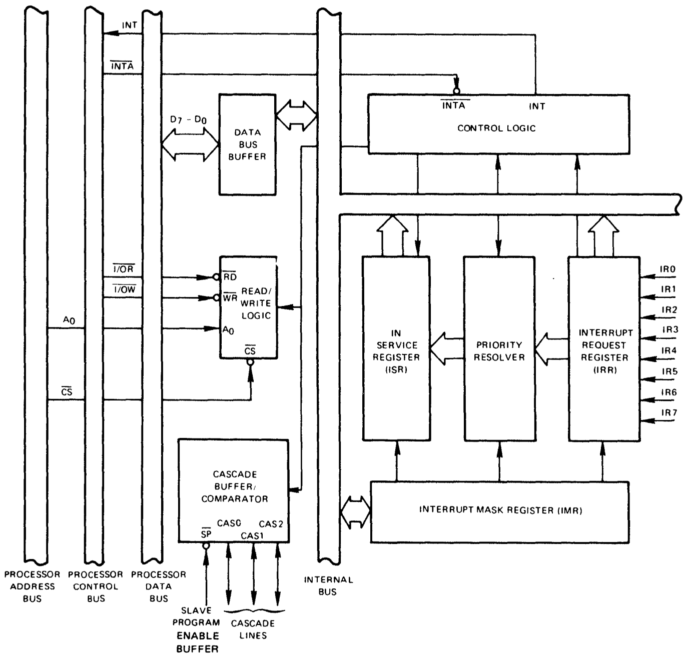
PIN CONFIGURATION



PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program Input/ Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Interrupt Output- High Voltage	V_{OH-INT}	2.4 3.5			V V	I_{OH} = −400 μA I_{OH} = −50 μA
Input Leakage Current for IR_{0-7}	I_{IL} (IR_{0-7})			−300 10	μA μA	V_{IN} = 0V V_{IN} = V_{CC}
Input Leakage Current for other Inputs	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LOL}			− 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Supply Current	I_{CC}			100	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5V ± 10% (μPD8259A)

PARAMETER	SYMBOL	μPD8259A		μPD8259A-2		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	t_{AHRL}	0		0		ns	
AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	t_{RHAX}	0		0		ns	
$\overline{RD}$ Pulse Width	t_{RLRH}	235		160		ns	
AO/$\overline{CS}$ Setup to $\overline{WR}$↓	t_{AHWL}	0		0		ns	
AO/$\overline{CS}$ Hold after $\overline{WR}$↑	t_{WHAX}	0		0		ns	
$\overline{WR}$ Pulse Width	t_{WLWH}	290		190		ns	
Data Setup to $\overline{WR}$↑	t_{DVWH}	240		160		ns	
Data Hold after $\overline{WR}$↑	t_{WHDX}	0		0		ns	
Interrupt Request Width (Low)	t_{JLJH}	100		100		ns	①
Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	t_{CVIAL}	55		40		ns	
End of $\overline{RD}$ to Next Command	t_{RHRL}	160		160		ns	
End of $\overline{WR}$ to Next Command	t_{WHRL}	190		190		ns	

Note: ① This is the low time required to clear the input latch in the edge triggered mode.

PARAMETER	SYMBOL	μPD8259A		μPD8259A-2		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Data Valid from $\overline{RD}$/$\overline{INTA}$↓	t_{RLDV}		200		120	ns	C of Data Bus = 100 pF
Data Float after $\overline{RD}$/$\overline{INTA}$↑	t_{RHDZ}		100		85	ns	C of Data Bus Max Test C = 100 pF Min Test C = 15 pF
Interrupt Output Delay	t_{JHIH}		350		300	ns	
Cascade Valid from First $\overline{INTA}$↓ (Master Only)	t_{IAHCV}		565		360	ns	C_{INT} = 100 pF
Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓	t_{RLEL}		125		100	ns	$C_{CASCADE}$ = 100 pF
Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑	t_{RHEH}		150		150	ns	
Data Valid from Stable Address	t_{AHDV}		200		200	ns	
Cascade Valid to Valid Data	t_{CVDV}		300		200	ns	

FUNCTIONAL DESCRIPTION

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259 is set high. The IR input line must remain high until the first $\overline{\text{INTA}}$ input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080A/8085A/8086/8088.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT ACKNOWLEDGE ($\overline{\text{INTA}}$)

$\overline{\text{INTA}}$ pulses cause the μPD8259A to put vectoring information on the bus. The number of pulses depends upon whether the μPD8259A is in μPD8085A mode or 8086/8088 mode.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{CS}}$ inputs.

μPD8259A BASIC OPERATION						
A_0	D_4	D_3	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259A aligns these commands in the proper order.

CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259 Array.)

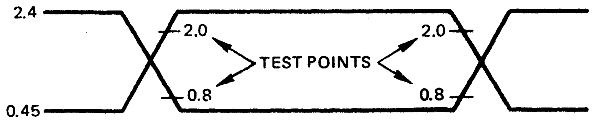
The ID's of all μPD8259A's are buffered and compared in the cascade buffer/comparator. The master μPD8259A sends the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{\text{INTA}}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

SLAVE PROGRAM ($\overline{\text{SP}}$). (For Use in Multiple μPD8259A Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259A's in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The $\overline{\text{SP}}$ input to the device selects the CAS0-2 lines as either outputs ($\overline{\text{SP}}$=1) for the master or as inputs ($\overline{\text{SP}}$=0) for the slaves. For one device only the $\overline{\text{SP}}$ must be set to a logic "1" since it is functioning as a master.

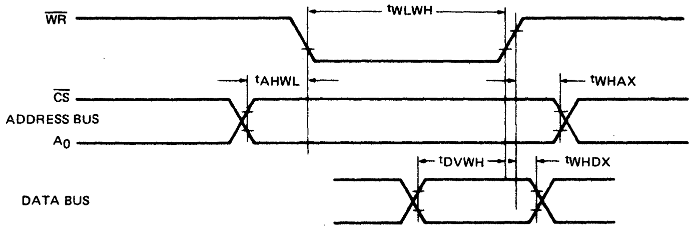
AC CHARACTERISTICS (CONT.)

INPUT WAVEFORMS FOR AC TESTS

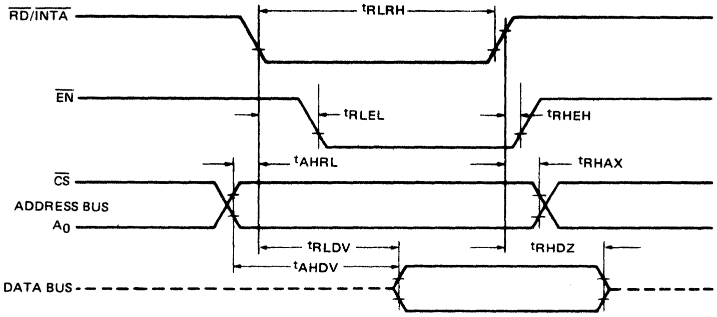


TIMING WAVEFORMS

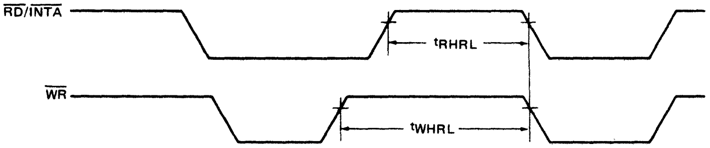
WRITE MODE



READ/$\overline{INTA}$ MODE

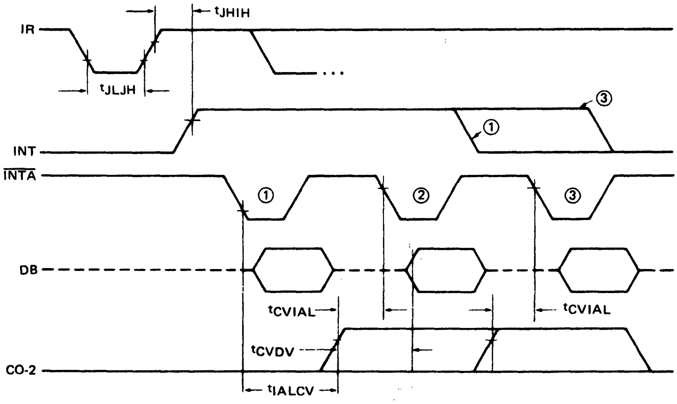


OTHER TIMING



TIMING WAVEFORMS (CONT.)

$\overline{\text{INTA}}$ SEQUENCE



DETAILED OPERATIONAL DESCRIPTION

The sequence used by the μPD8259A to handle an interrupt depends upon whether an 8080A/8085A or 8086/8088 CPU is being used.

The following sequence applies to 8080A/8085A systems:

The μPD8259A derives its versatility from programmable interrupt modes and the ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259A interacts with the processor.

1. An interrupt or interrupts appearing on $IR_{0\text{-}7}$ sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259A will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{\text{INTA}}$ to the μPD8259A when it receives the INT.
4. The $\overline{\text{INTA}}$ input to the μPD8259A from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The $\overline{\text{INTA}}$ also signals the μPD8259A to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{\text{INTA}}$ pulses to the μPD8259A.
6. The two $\overline{\text{INTA}}$ pulses signal the μPD8259A to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{\text{INTA}}$ releases the low-order 8-bits of the address and the second $\overline{\text{INTA}}$ releases the high-order 8-bits.
7. The μPD8259A's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259A at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259A to service the next interrupt.

For 8086/8088 systems the first three steps are the same as described above, then the following sequence occurs:

4. During the first $\overline{\text{INTA}}$ from the processor, the μPD8259A does not drive the data bus. The highest priority ISR bit is set and the corresponding IRR bit is reset.
5. The μPD8259A puts vector onto the data bus on the second $\overline{\text{INTA}}$ pulse from the 8086/8088.
6. There is no third $\overline{\text{INTA}}$ pulse in this mode. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse, or it remains set until an EOI command is issued.

INTERRUPT SEQUENCE

8080A/8085A MODE

For these processors, the μPD8259A is controlled by three $\overline{\text{INTA}}$ pulses. The first $\overline{\text{INTA}}$ pulse will cause the μPD8259A to put the CALL op-code onto the data bus. The second and third $\overline{\text{INTA}}$ pulses will cause the upper and lower address of the interrupt vector to be released on the bus.

FIRST $\overline{\text{INTA}}$

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

SECOND $\overline{\text{INTA}}$

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

THIRD $\overline{\text{INTA}}$

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

In this mode only two $\overline{\text{INTA}}$ pulses are sent to the μPD8259A. After the first $\overline{\text{INTA}}$ pulse, the μPD8259A does not output a CALL but internally sets priority resolution. If it is a master, it sets the cascade lines. The interrupt vector is output to the data bus on the second $\overline{\text{INTA}}$ pulse.

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

INITIALIZATION COMMAND WORDS

ICW1 AND ICW2

A_5-A_{15}. *Page starting address of service routines.* In an 8085A system, the 8 request levels generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the μPD8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the μPD8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval maintains compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system, T7-T3 are inserted in the five most significant bits of the vectoring byte and the μPD8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address Interval) has no effect.

LTIM: If LTIM = 1, then the μPD8259A operates in the level interrupt mode. Edge detect logic on the interrupt inputs is disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only μPD8259A in the system. If SNGL = 1 no ICW3 is issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

ICW3

This word is read only when there is more than one μPD8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then releases byte 1 of the call sequence (for 8085A system) and enables the corresponding slave to release bytes 2 and 3 (for 8086/8088 only byte 2) through the cascade lines.

b. In the slave mode (either when SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the CALL sequence (or just byte 2 for 8086/8088) are released by it on the Data Bus.

ICW4

SFNM: If SFNM = 1 the special fully nested mode is programmed.

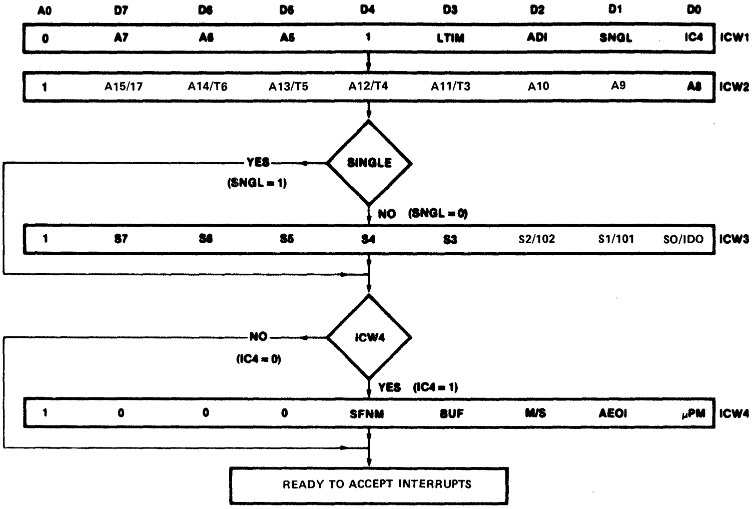
BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the μPD8259A is programmed to be a master, M/S = 0 means the μPD8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the μPD8259A for 8085A system operation, μPM = 1 sets the μPD8259A for 8086 system operation.

INITIALIZATION SEQUENCE


A0 D7 D6 D5 D4 D3 D2 D1 D0
0 A7 A6 A5 1 LTIM ADI SNGL IC4 ICW1
1 A15/17 A14/T6 A13/T5 A12/T4 A11/T3 A10 A9 A8 ICW2
SINGLE
YES
(SNGL = 1)
NO (SNGL = 0)
1 S7 S6 S5 S4 S3 S2/102 S1/101 SO/IDO ICW3
ICW4
NO
(IC4 = 0)
YES (IC4 = 1)
1 0 0 0 SFNM BUF M/S AEOI μPM ICW4
READY TO ACCEPT INTERRUPTS

OPPERATIONAL COMMAND WORDS (OCW's) ②

Once the μPD8259A has been programmed with Initialization Command Words, it can be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259A can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCWs.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259A has acknowledged an interrupt, i.e., the μPD8259A has sent an INT signal to the processor and the system controller has sent it an $\overline{\text{INTA}}$ signal, the interrupt input, although it is masked, inhibits lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259A's basic operating mode. It will operate in this mode after the initialization sequence, without requiring Operation Command Words for formatting. Priorities are set IR_0 through IR_7, with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an INTA, the priority resolver determines the priority of the interrupt, sets the corresponding IR bit, and outputs the vector address to the Data bus. The EOI command resets the corresponding ISR bits at the end of its service routines.

Notes: ① Reference Figure 2
② Reference Figure 3

OPERATIONAL COMMAND WORDS (CONT.)

ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	1	0	0
Priority Status Register	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	IR_0

→ Highest Priority

   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	0	0	0
Priority Status Register	IR_2	IR_1	IR_0	IR_7	IR_6	IR_5	IR_4	IR_3

→ Highest Priority

   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259A is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259A then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

OPERATIONAL COMMAND WORDS (CONT.)

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259A is ready to service the next interrupt.

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259A's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command automatically resets the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" inhibits lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259A remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

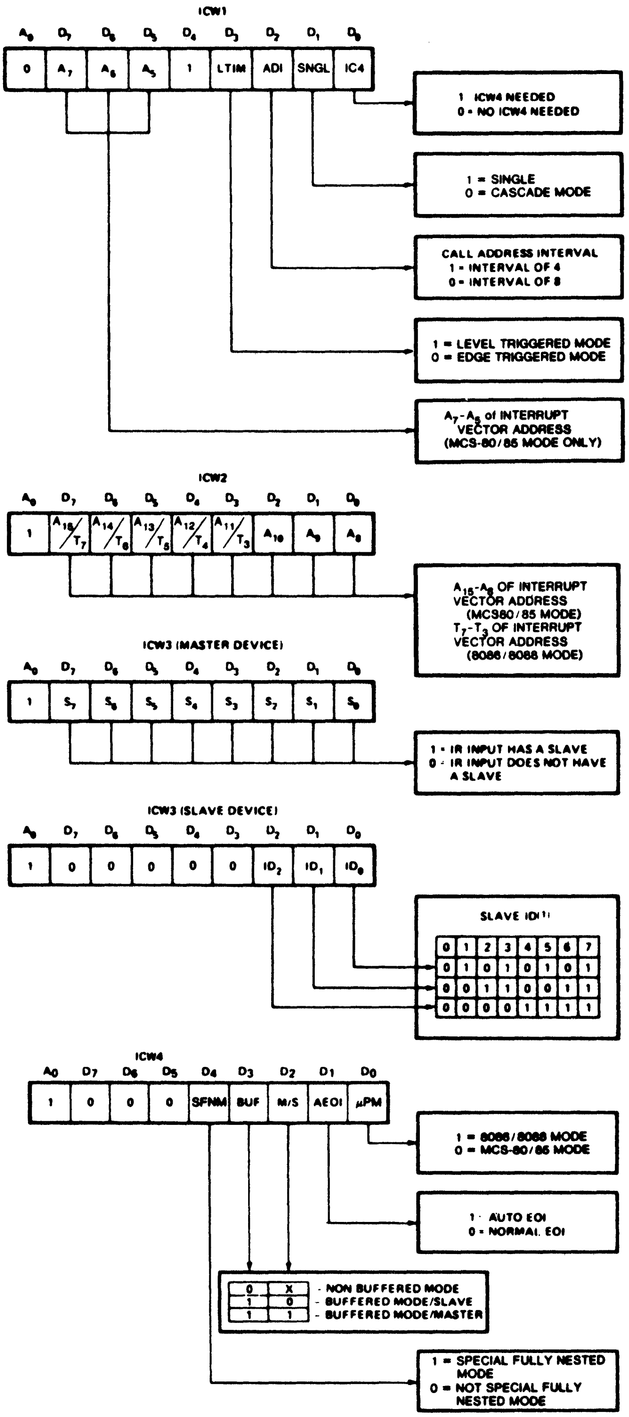
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required, thus saving in ROM space. Poll Mode can also be used to expand the number of interrupts beyond 64.

INITIALIZATION COMMAND WORD FORMAT



ICW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	LTIM	ADI	SNGL	IC4

1 ICW4 NEEDED
0 = NO ICW4 NEEDED

1 = SINGLE
0 = CASCADE MODE

CALL ADDRESS INTERVAL
1 = INTERVAL OF 4
0 = INTERVAL OF 8

1 = LEVEL TRIGGERED MODE
0 = EDGE TRIGGERED MODE

A_7-A_5 of INTERRUPT VECTOR ADDRESS (MCS-80/85 MODE ONLY)

ICW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	A_{15}/T_7	A_{14}/T_6	A_{13}/T_5	A_{12}/T_4	A_{11}/T_3	A_{10}	A_9	A_8

A_{15}-A_8 OF INTERRUPT VECTOR ADDRESS (MCS80/85 MODE)
T_7-T_3 OF INTERRUPT VECTOR ADDRESS (8086/8088 MODE)

ICW3 (MASTER DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_7	S_1	S_0

1 = IR INPUT HAS A SLAVE
0 = IR INPUT DOES NOT HAVE A SLAVE

ICW3 (SLAVE DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

SLAVE ID[1]

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

ICW4

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SFNM	BUF	M/S	AEOI	μPM

1 = 8086/8088 MODE
0 = MCS-80/85 MODE

1 AUTO EOI
0 = NORMAL EOI

0	X	- NON BUFFERED MODE
1	0	- BUFFERED MODE/SLAVE
1	1	- BUFFERED MODE/MASTER

1 = SPECIAL FULLY NESTED MODE
0 = NOT SPECIAL FULLY NESTED MODE

NOTE 1: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

READING μPD8259 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. The highest priority in-service bit is reset once it has been acknowledged. (Note that the Interrupt Mask Register has no effect on the IRR.) A WR command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

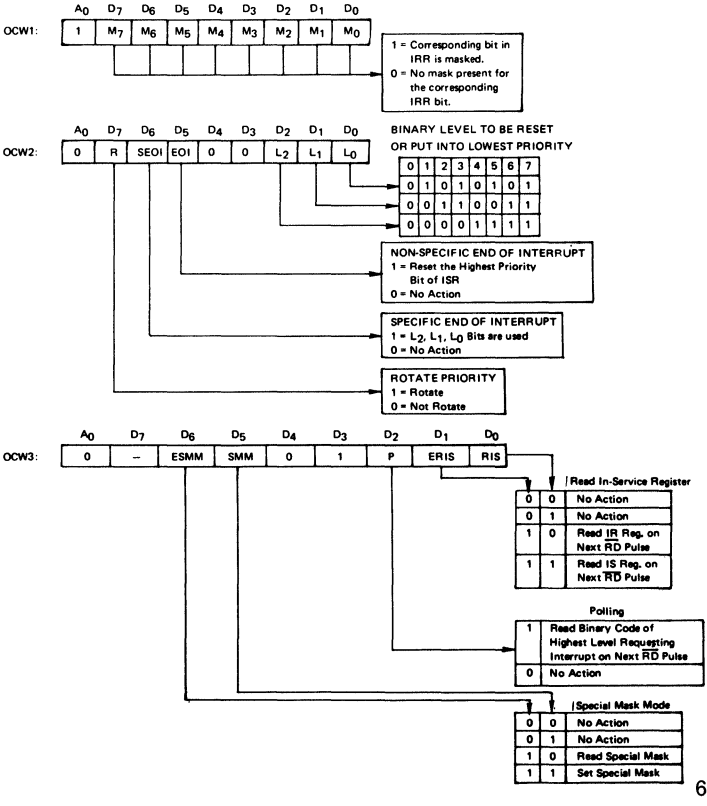
The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode when bits P and ERIS of OCW3 are set to a logic "1."

OPERATION COMMAND WORD FORMAT



OCW1:
A_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
1 M_7 M_6 M_5 M_4 M_3 M_2 M_1 M_0
1 = Corresponding bit in IRR is masked.
0 = No mask present for the corresponding IRR bit.
OCW2:
A_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0 R SEOI EOI 0 0 L_2 L_1 L_0
BINARY LEVEL TO BE RESET OR PUT INTO LOWEST PRIORITY
0 1 2 3 4 5 6 7
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1
NON-SPECIFIC END OF INTERRUPT
1 = Reset the Highest Priority Bit of ISR
0 = No Action
SPECIFIC END OF INTERRUPT
1 = L_2, L_1, L_0 Bits are used
0 = No Action
ROTATE PRIORITY
1 = Rotate
0 = Not Rotate
OCW3:
A_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0 – ESMM SMM 0 1 P ERIS RIS
Read In-Service Register
0 0 No Action
0 1 No Action
1 0 Read IR Reg. on Next $\overline{RD}$ Pulse
1 1 Read IS Reg. on Next $\overline{RD}$ Pulse
Polling
1 Read Binary Code of Highest Level Requesting Interrupt on Next $\overline{RD}$ Pulse
0 No Action
Special Mask Mode
0 0 No Action
0 1 No Action
1 0 Reset Special Mask
1 1 Set Special Mask

9

SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic		A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description	
1	ICW1	A	0	A7	A6	A5	1	0	1	1	0		Format = 4, single, edge triggered
2	ICW1	B	0	A7	A6	A5	1	1	1	1	0		Format = 4, single, level triggered
3	ICW1	C	0	A7	A6	A5	1	0	1	0	0	Byte 1 Initialization	Format = 4, not single, edge triggered
4	ICW1	D	0	A7	A6	A5	1	1	1	0	0		Format = 4, not single, level triggered
5	ICW1	E	0	A7	A6	0	1	0	0	1	0	No ICW4 Requirpd	Format = 8, single, edge triggered
6	ICW1	F	0	A7	A6	0	1	1	0	1	0		Format = 8, single, level triggered
7	ICW1	G	0	A7	A6	0	1	0	0	0	0		Format = 8, not single, edge triggered
8	ICW1	H	0	A7	A6	0	1	1	0	0	0		Format = 8, not single, level triggered
9	ICW1	I	0	A7	A6	A5	1	0	1	1	1		Format = 4, single, edge triggered
10	ICW1	J	0	A7	A6	A5	1	1	1	1	1		Format = 4, single, level triggered
11	ICW1	K	0	A7	A6	A5	1	0	1	0	1	Byte 1 Initialization	Format = 4, not single, edge triggered
12	ICW1	L	0	A7	A6	A5	1	1	1	0	1		Format = 4, not single, level triggered
13	ICW1	M	0	A7	A6	0	1	0	0	1	1	ICW4 Required	Format = 8, single, edge triggered
14	ICW1	N	0	A7	A6	0	1	1	0	1	1		Format = 8, single, level triggered
15	ICW1	O	0	A7	A6	0	1	0	0	0	1		Format = 8, not single, edge triggered
16	ICW1	P	0	A7	A6	0	1	1	0	0	1		Format = 8, not single, level triggered
17	ICW2		1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization	
18	ICW3	M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master	
19	ICW3	S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave	
20	ICW4	A	1	0	0	0	0	0	0	0	0	No action, redundant	
21	ICW4	B	1	0	0	0	0	0	0	0	1	Non-buffered mode, no AEOI, 8086/8088	
22	ICW4	C	1	0	0	0	0	0	0	1	0	Non-buffered mode, AEOI, 80/85	
23	ICW4	D	1	0	0	0	0	0	0	1	1	Non-buffered mode, AEOI, 8086/8088	
24	ICW4	E	1	0	0	0	0	0	1	0	0	No action, redundant	
25	ICW4	F	1	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOI, 8086/8088	
26	ICW4	G	1	0	0	0	0	0	1	1	0	Non-buffered mode, AEOI, 80/85	
27	ICW4	H	1	0	0	0	0	0	1	1	1	Non-buffered mode, AEOI, 8086/8088	
28	ICW4	I	1	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOI, 80/85	
29	ICW4	J	1	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOI, 8086/8088	
30	ICW4	K	1	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOI, 80/85	
31	ICW4	L	1	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOI, 8086/8088	
32	ICW4	M	1	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOI, 80/85	
33	ICW4	N	1	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOI, 8086/8088	
34	ICW4	O	1	0	0	0	0	1	1	1	0	Buffered mode, master, AEOI, 80/85	
35	ICW4	P	1	0	0	0	0	1	1	1	1	Buffered mode, master AEOI, 8086, 8088	
36	ICW4	NA	1	0	0	0	1	0	0	0	0	Fully nested mode, 8085A, non-buffered, no AEOI	
37	ICW4	NB	1	0	0	0	1	0	0	0	1	ICW4 NB through ICW4 ND are identical to ICW4 B through ICW4 D with the addition of Fully Nested Mode	
38	ICW4	NC	1	0	0	0	1	0	0	1	0		
39	ICW4	ND	1	0	0	0	1	0	0	1	1		
40	ICW4	NE	1	0	0	0	1	0	1	0	0	Fully Nested Mode, 80/85, non-buffered, no AEOI	
41	ICW4	NF	1	0	0	0	1	0	1	0	1	ICW4 NF through ICW4 NP are identical to ICW4 F through ICW4 P with the addition of Fully Nested Mode	
42	ICW4	NG	1	0	0	0	1	0	1	1	0		
43	ICW4	NH	1	0	0	0	1	0	1	1	1		
44	ICW4	NI	1	0	0	0	1	1	0	0	0		
45	ICW4	NJ	1	0	0	0	1	1	0	0	1		
46	ICW4	NK	1	0	0	0	1	1	0	1	0		
47	ICW4	NL	1	0	0	0	1	1	0	1	1		
48	ICW4	NM	1	0	0	0	1	1	1	0	0		
49	ICW4	NN	1	0	0	0	1	1	1	0	1		
50	ICW4	NO	1	0	0	0	1	1	1	1	0		
51	ICW4	NP	1	0	0	0	1	1	1	1	1		
52	OCW1		1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mark register	
53	OCW2	E	0	0	0	1	0	0	0	0	0	Non-specific EOI	
54	OCW2	SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI, L0-L2 code of IS FF to be reset	
55	OCW2	RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI	
56	OCW2	RSE	0	1	1	1	0	0	L2	L1	L0	Rotate on Specific EOI L0-L2 code of line	
57	OCW2	R	0	1	0	0	0	0	0	0	0	Rotate in Auto EOI (set)	
58	OCW2	CR	0	0	0	0	0	0	0	0	0	Rotate in Auto EOI (clear)	
59	OCW2	RS	0	1	1	0	0	0	L2	L1	L0	Set Priority Command	
60	OCW3	P	0	0	0	0	0	1	1	0	0	Poll mode	
61	OCW3	RIS	0	0	0	0	0	1	0	1	1	Read IS register	

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

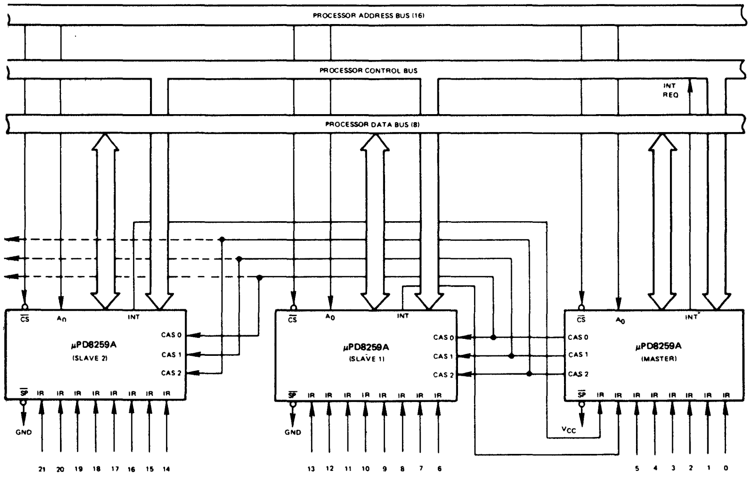
	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

LOWER MEMORY INTERRUPT VECTOR ADDRESS

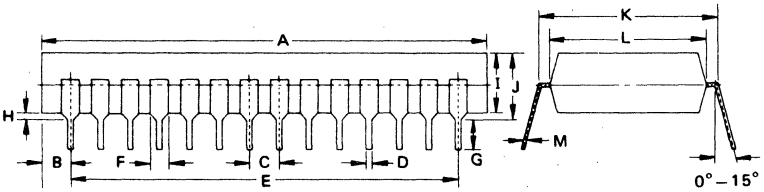
	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259As.



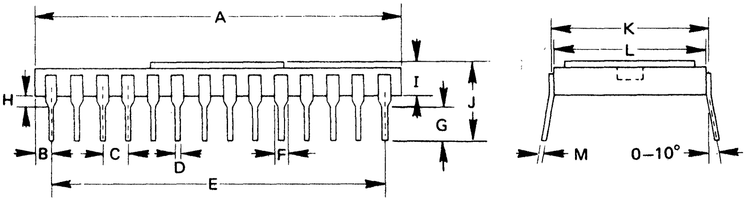
PACKAGE OUTLINE
μPD8259AC



(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

μPD8259AD



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
. L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002