

5400 PIXELS \times 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μ PD8861 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μ PD8861 has 3 rows of 5400 pixels, and each row has a single-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

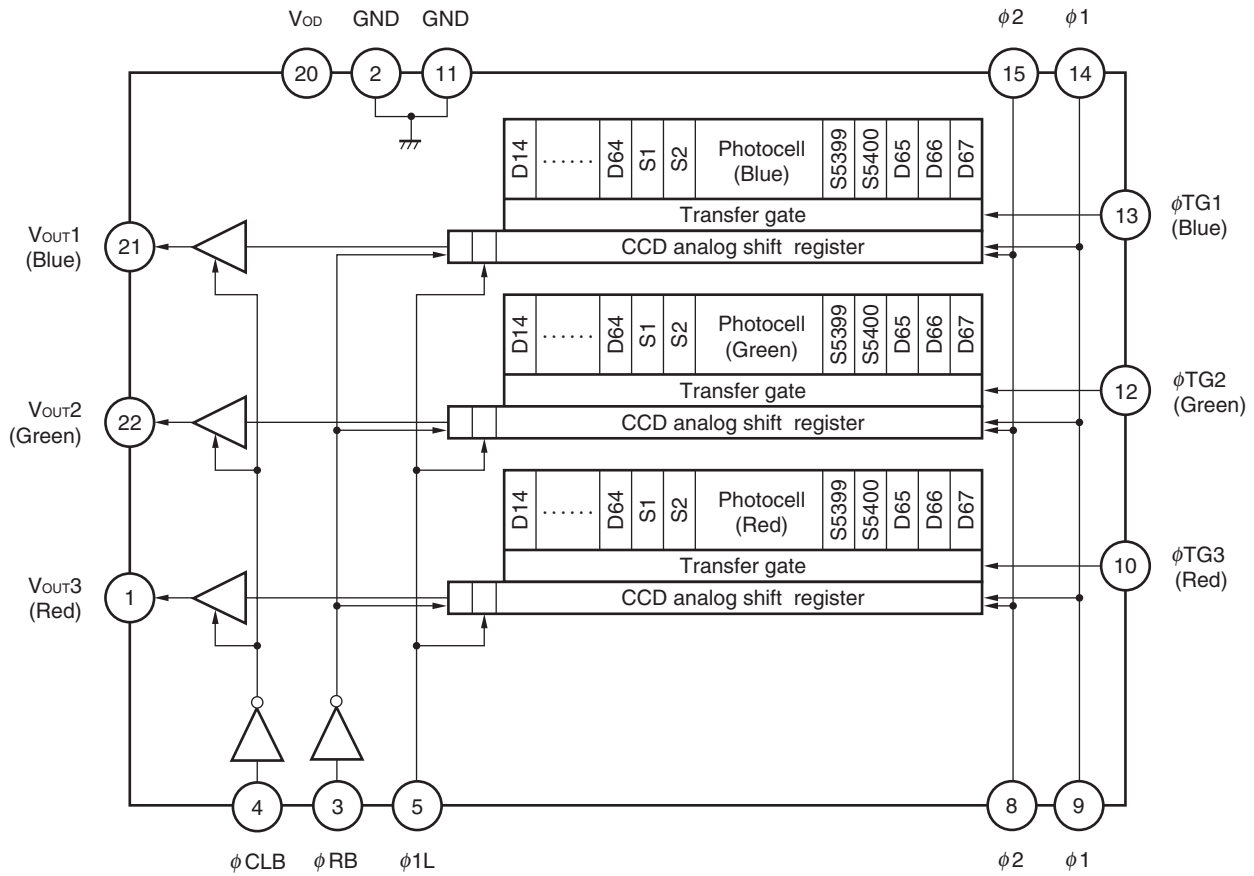
- Valid photocell : 5400 pixels \times 3
- Photocell pitch : 5.25 μ m
- Photocell size : 5.25 \times 5.25 μ m²
- Line spacing : 42 μ m (8 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10⁷ lx•hour)
- Resolution : 24 dot/mm A4 (210 \times 297 mm) size (shorter side)
600 dpi US letter (8.5" \times 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 6 MHz Max.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μ PD8861CY	CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

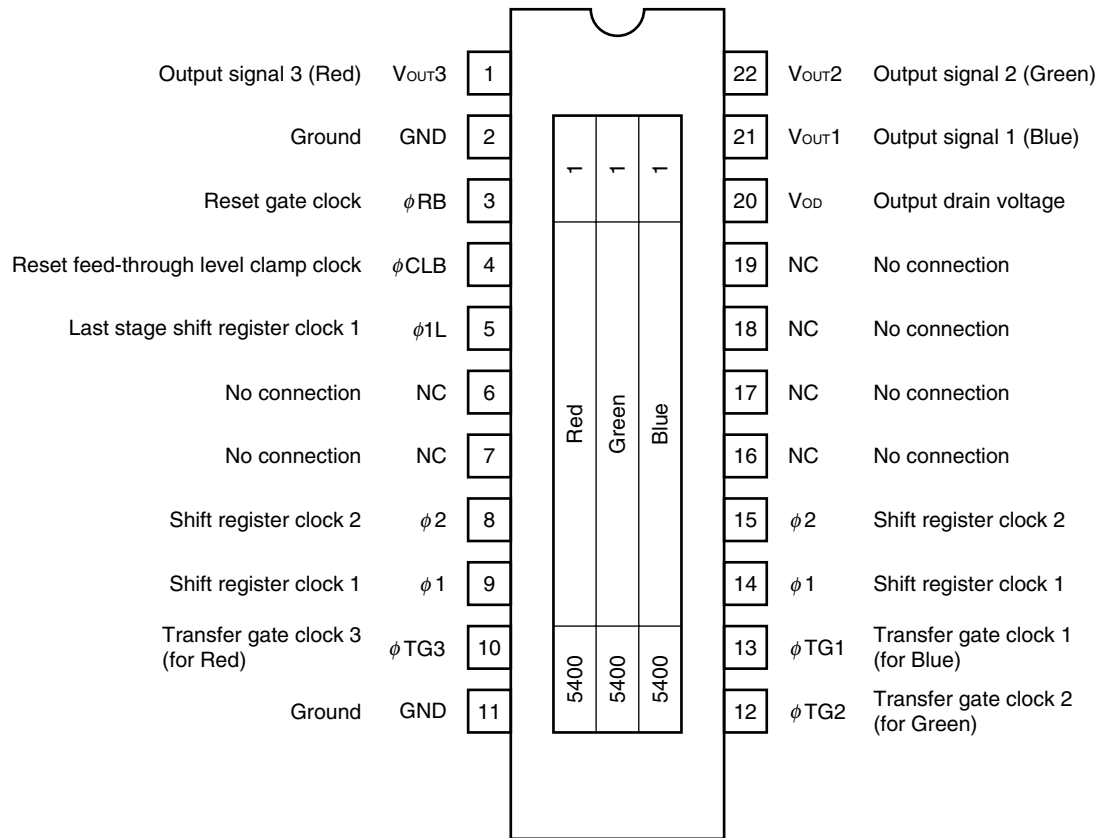
BLOCK DIAGRAM



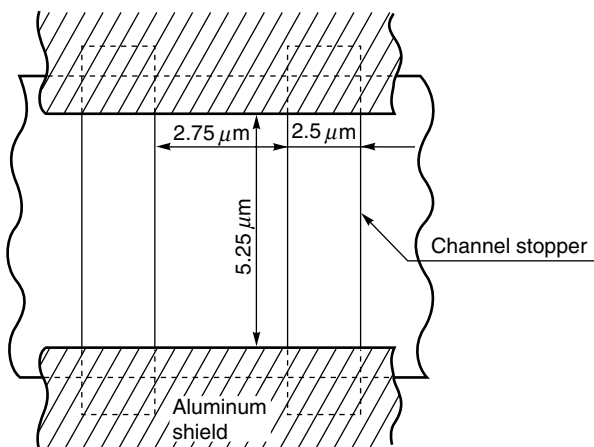
PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

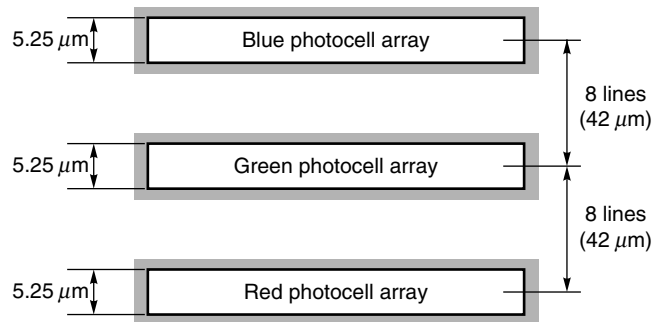
• μPD8861CY



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V _{OD}	-0.3 to +15	V
Shift register clock voltage	V _{φ1} , V _{φ2} , V _{φ1L}	-0.3 to +8	V
Reset gate clock voltage	V _{φRB}	-0.3 to +8	V
Reset feed-through level clamp clock voltage	V _{φCLB}	-0.3 to +8	V
Transfer gate clock voltage	V _{φTG1} to V _{φTG3}	-0.3 to +8	V
Operating ambient temperature	T _A	0 to +60	°C
Storage temperature	T _{stg}	-40 to +70	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V _{OD}	11.4	12.0	12.6	V
Shift register clock high level	V _{φ1H} , V _{φ2H} , V _{φ1LH}	4.5	5.0	5.5	V
Shift register clock low level	V _{φ1L} , V _{φ2L} , V _{φ1LL}	-0.3	0	+0.5	V
Reset gate clock high level	V _{φRBH}	4.5	5.0	5.5	V
Reset gate clock low level	V _{φRBL}	-0.3	0	+0.5	V
Reset feed-through level clamp clock high level	V _{φCLBH}	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	V _{φCLBL}	-0.3	0	+0.5	V
Transfer gate clock high level	V _{φTG1H} to V _{φTG3H}	4.5	V _{φ1H} ^{Note}	V _{φ1H} ^{Note}	V
Transfer gate clock low level	V _{φTG1L} to V _{φTG3L}	-0.3	0	+0.3	V
Data rate	f _{φRB}	-	1.0	6.0	MHz

Note When Transfer gate clock high level (V_{φTG1H} to V_{φTG3H}) is higher than Shift register clock high level (V_{φ1H}), Image lag can increase.

ELECTRICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$, $V_{OD} = 12\text{ V}$, data rate ($f_{\phi RB}$) = 1 MHz, storage time = 5.5 ms, input signal clock = 5 V_{p-p},
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage	V_{sat}		2.0	2.5	–	V
Saturation exposure	Red	SER	–	0.420	–	lx•s
	Green	SEG	–	0.429	–	lx•s
	Blue	SEB	–	0.739	–	lx•s
Photo response non-uniformity	PRNU	$V_{OUT} = 1.0\text{ V}$	–	6	20	%
Average dark signal	ADS	Light shielding	–	0.2	2.0	mV
Dark signal non-uniformity	DSNU	Light shielding	–	1.5	5.0	mV
Power consumption	P_w		–	360	540	mW
Output impedance	Z_o		–	0.35	1	kΩ
Response	Red	R_R	4.15	5.94	7.72	V/lx•s
	Green	R_G	4.07	5.82	7.57	V/lx•s
	Blue	R_B	2.36	3.38	4.39	V/lx•s
Image lag	IL	$V_{OUT} = 1.0\text{ V}$	–	1.5	7.0	%
Offset level ^{Note 1}	V_{OS}		4.0	5.5	7.0	V
Output fall delay time ^{Note 2}	t_d	$V_{OUT} = 1.0\text{ V}$	–	25	–	ns
Total transfer efficiency	TTE	$V_{OUT} = 1.0\text{ V}$, data rate = 6 MHz	92	98	–	%
Response peak	Red		–	630	–	nm
	Green		–	540	–	nm
	Blue		–	460	–	nm
Dynamic range	DR1	$V_{sat}/DSNU$	–	1666	–	times
	DR2	V_{sat}/σ_{CDS}	–	2777	–	times
Reset feed-through noise ^{Note 1}	RFTN	Light shielding	0	750	1500	mV
Random noise (CDS)	σ_{CDS}	Light shielding, bit clamp mode	–	0.9	–	mV

Notes 1. Refer to **TIMING CHART 2, 3.**

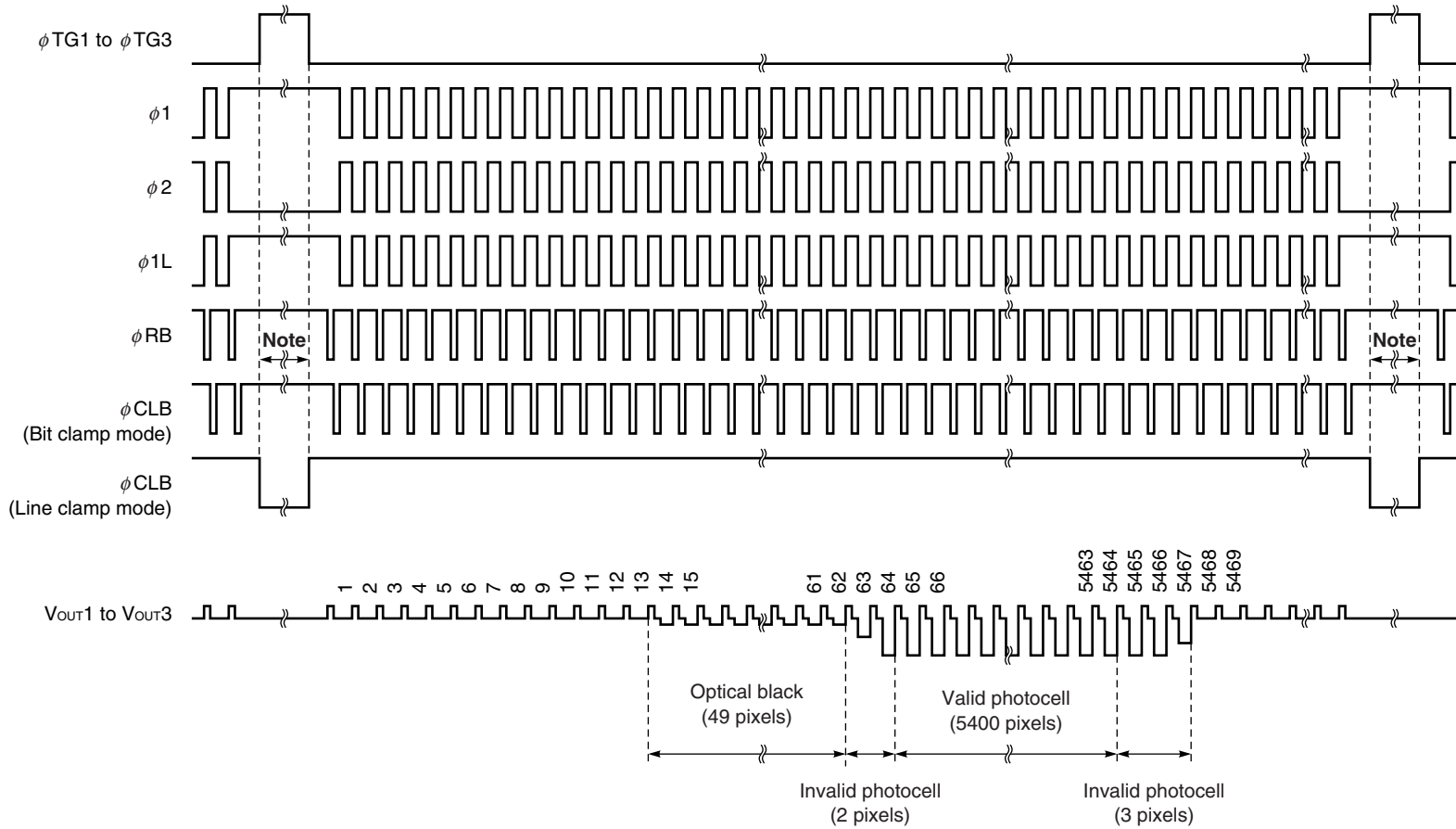
2. When the fall time of $\phi 1L$ ($t'1$) is the Typ. value (refer to **TIMING CHART 2, 3**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	C _{φ1}	φ 1	9	–	300	–	pF
			14	–	300	–	pF
Shift register clock pin capacitance 2	C _{φ2}	φ 2	8	–	300	–	pF
			15	–	300	–	pF
Last stage shift register clock pin capacitance	C _{φL}	φ 1L	5	–	10	–	pF
Reset gate clock pin capacitance	C _{φRB}	φ RB	3	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	C _{φCLB}	φ CLB	4	–	10	–	pF
Transfer gate clock pin capacitance	C _{φTG}	φ TG1	13	–	100	–	pF
		φ TG2	12	–	100	–	pF
		φ TG3	10	–	100	–	pF

Remark Pin 9 and 14 (φ1), 8 and 15 (φ2) are each connected inside of the device.

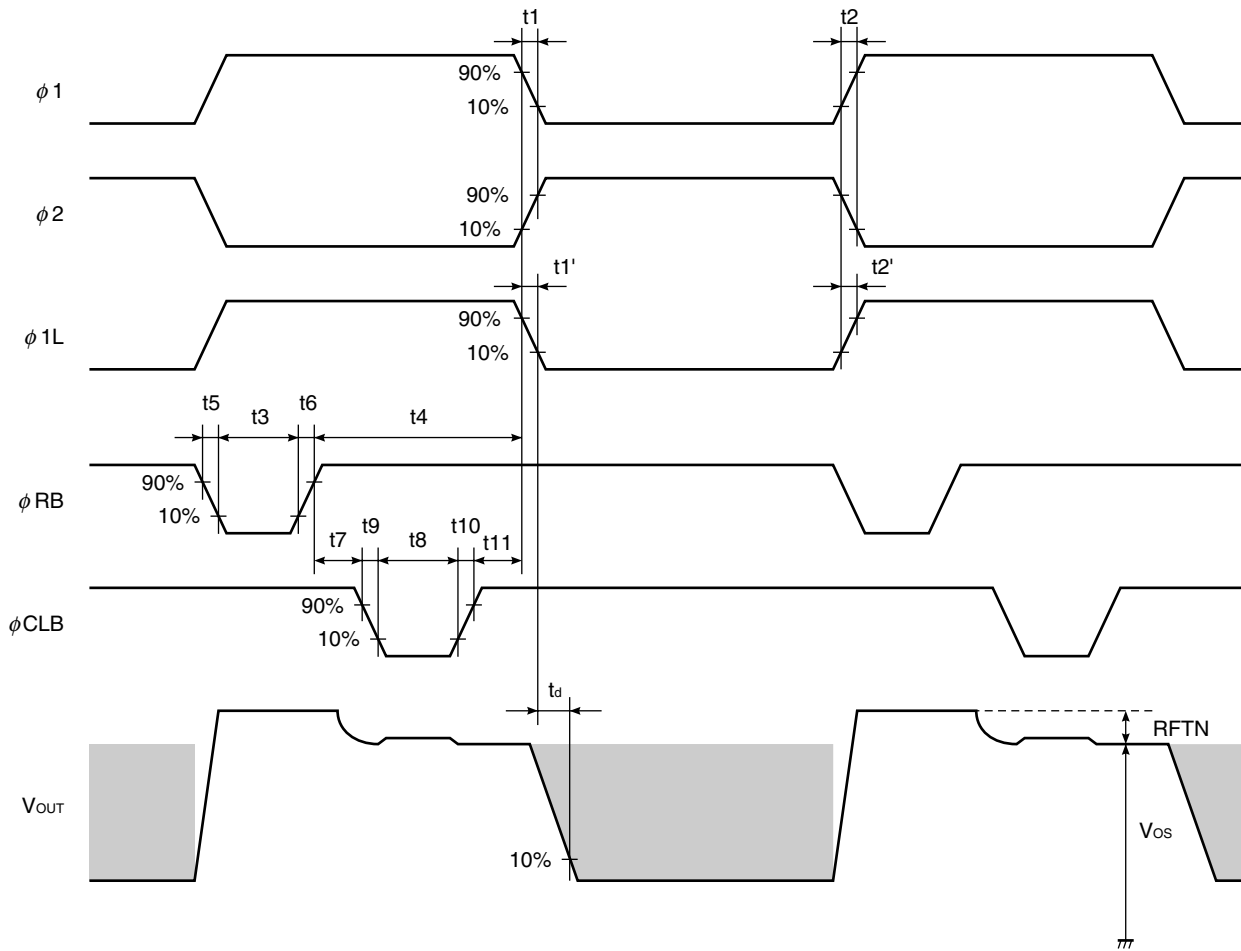
TIMING CHART 1 (for each color)



Note Set the ϕ RB and ϕ CLB (Bit clamp mode) to high level during this period.
 And stop the ϕ RB pulse while the ϕ CLB pulse is low level at line clamp mode.

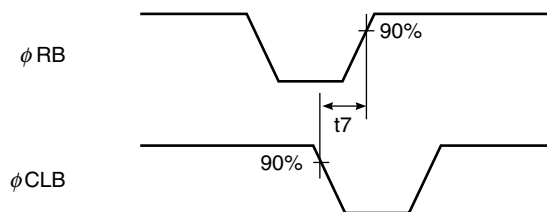
Remark Inverse pulse of the ϕ TG1 to ϕ TG3 can be used as ϕ CLB at line clamp mode.

TIMING CHART 2 (Bit clamp mode, for each color)

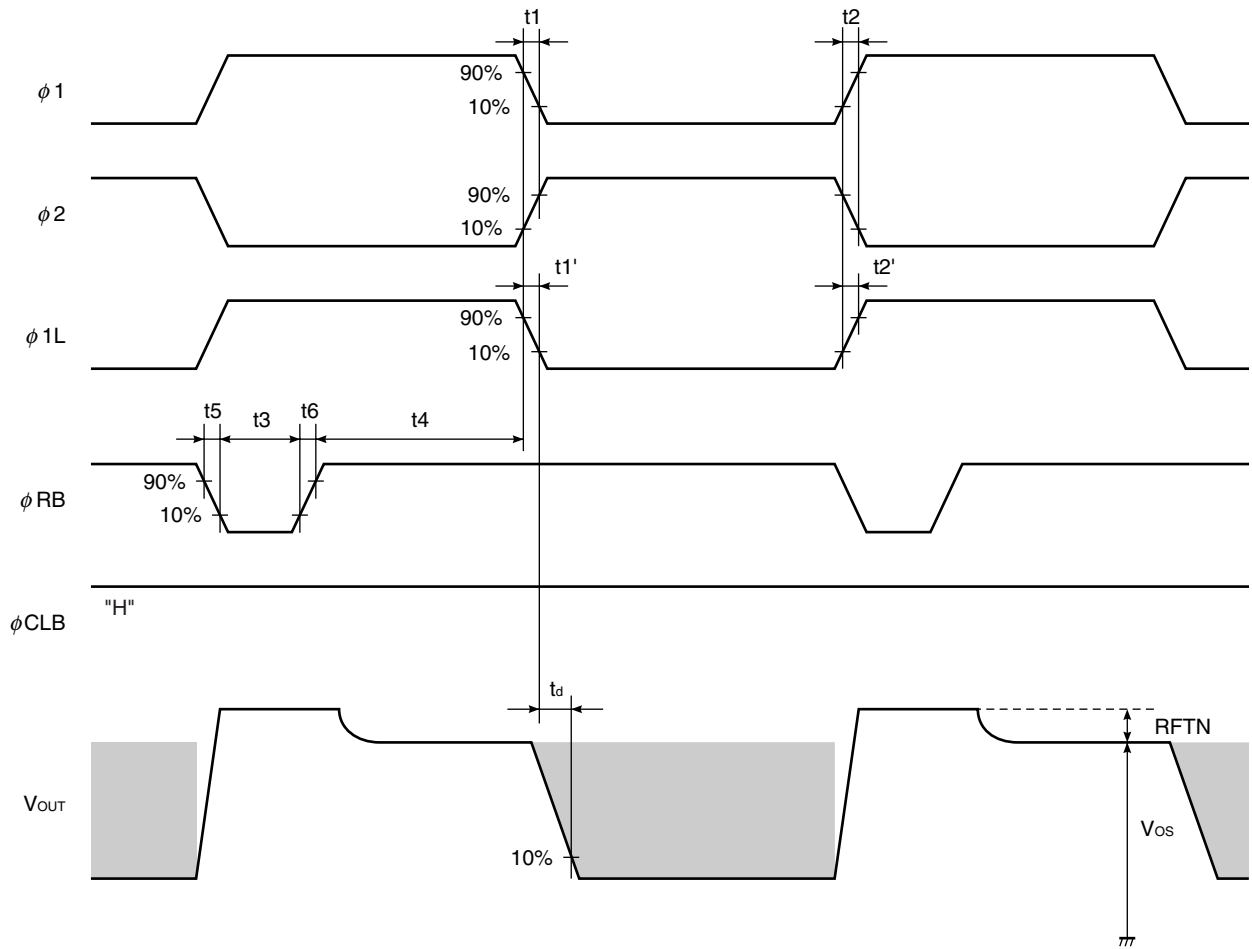


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	200	–	ns
t4	40	300	–	ns
t5, t6	0	5	–	ns
t7	-5 ^{Note}	50	–	ns
t8	35	200	–	ns
t9, t10	0	5	–	ns
t11	10	50	–	ns

Note Min. of t7 shows that the ϕRB and ϕCLB overlap each other.

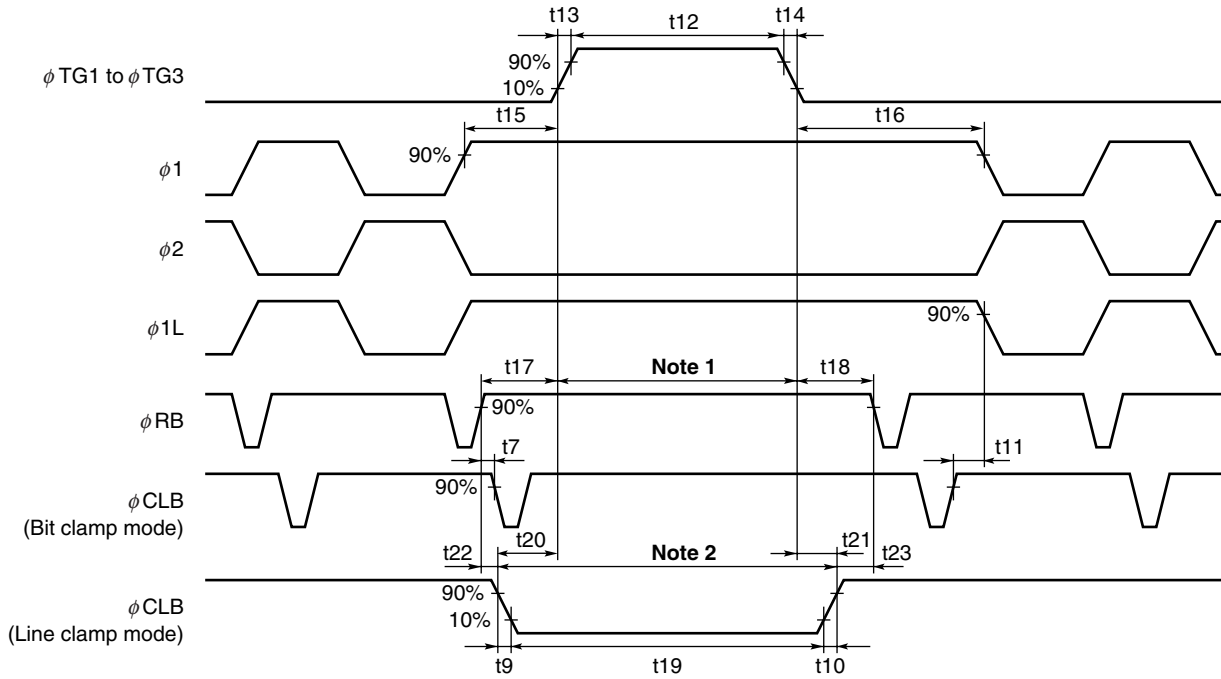


TIMING CHART 3 (Line clamp mode, for each color)



Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	200	–	ns
t4	40	300	–	ns
t5, t6	0	5	–	ns

★ TIMING CHART 4

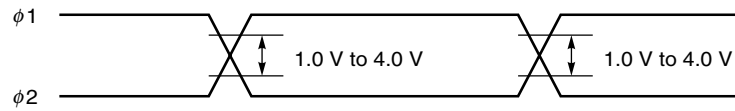


Symbol	Min.	Typ.	Max.	Unit
t7	-5 ^{Note 3}	50	-	ns
t9, t10	0	5	-	ns
t11	10	50	-	ns
t12	3000	10000	50000	ns
t13, t14	0	50	-	ns
t15, t16	900	1000	-	ns
t17, t18	200	400	-	ns
t19	t12	t12	50000	ns
t20, t21	0	50	-	ns
t22, t23	0	350	-	ns

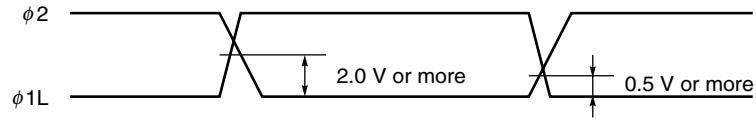
- Notes**
1. Set the ϕ RB and ϕ CLB (Bit clamp mode) to high level during this period.
 2. Stop the ϕ RB pulse during this period.
 3. Min. of t7 shows that the ϕ RB and ϕ CLB overlap each other.

Remark Inverse pulse of the ϕ TG1 to ϕ TG3 can be used as ϕ CLB.

★ $\phi 1, \phi 2$ cross points



$\phi 1L, \phi 2$ cross points



Remark Adjust cross points ($\phi 1, \phi 2$) and ($\phi 1L, \phi 2$) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

- 1. Saturation voltage : **V_{sat}**

Output signal voltage at which the response linearity is lost.

- 2. Saturation exposure : **SE**

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

- 3. Photo response non-uniformity : **PRNU**

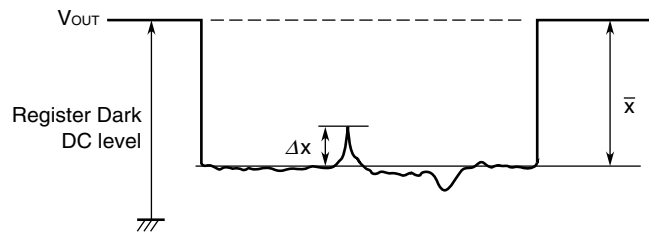
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

Δx : maximum of $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{5400} x_j}{5400}$$

x_j : Output voltage of valid pixel number j



- 4. Average dark signal : **ADS**

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{5400} d_j}{5400}$$

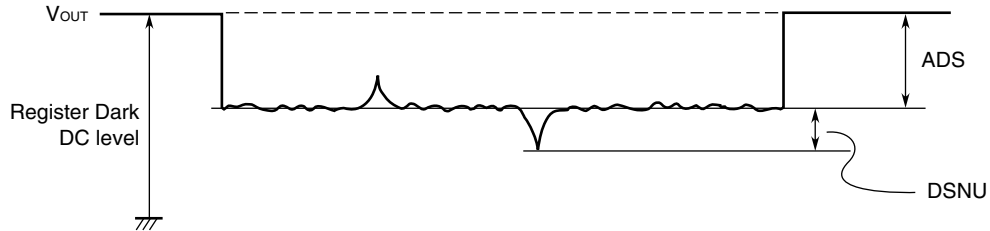
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}|_{j=1 \text{ to } 5400}$$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

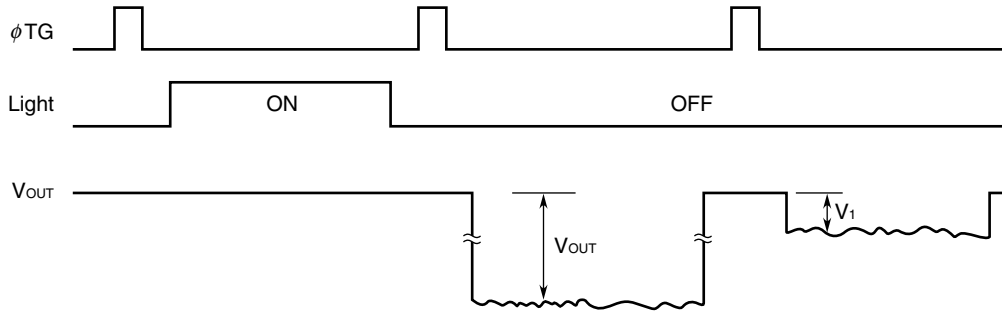
7. Response : **R**

Output voltage divided by exposure ($I \times s$).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{\text{OUT}}} \times 100$$

9. Random noise (CDS) : σ_{CDS}

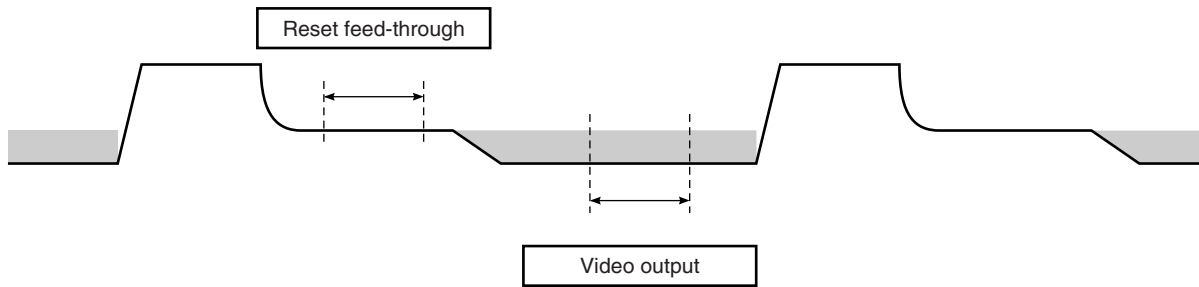
Random noise σ_{CDS} is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). σ_{CDS} is calculated by the following procedure.

1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get "VD_i".
3. The output level is measured during the video output time averaged over 100 ns to get "VO_i".
4. The correlated double sampling output is defined by the following formula.

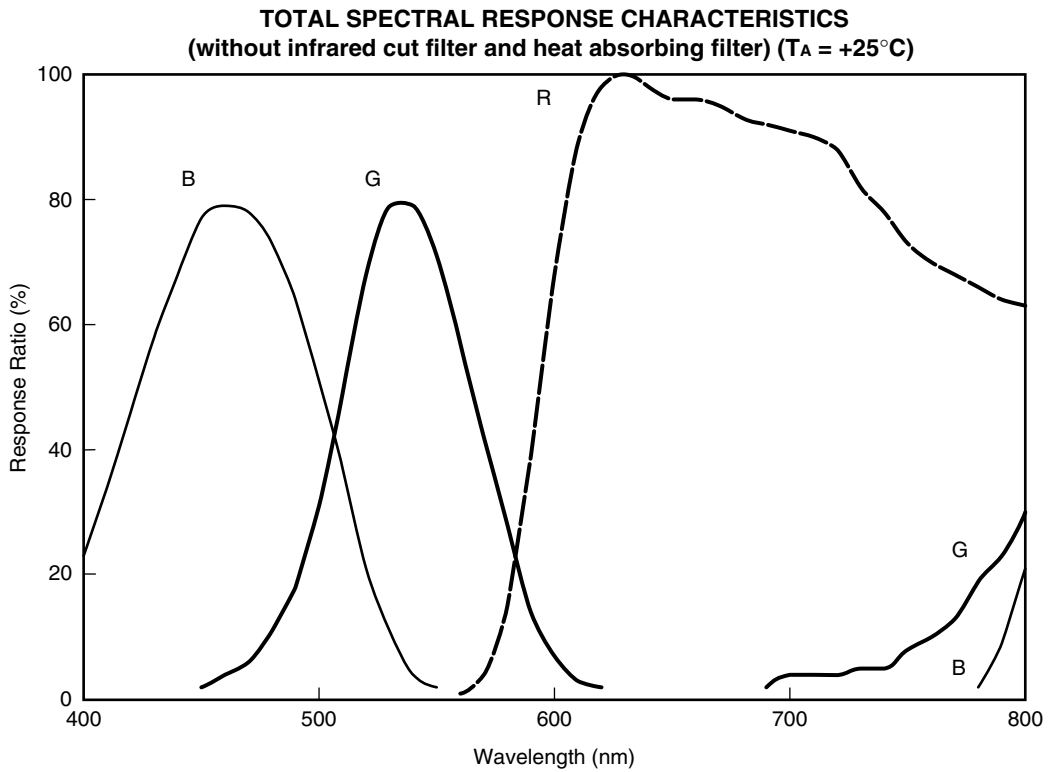
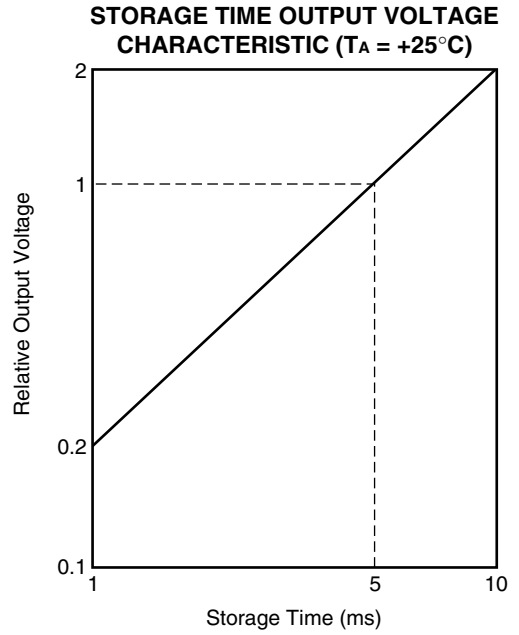
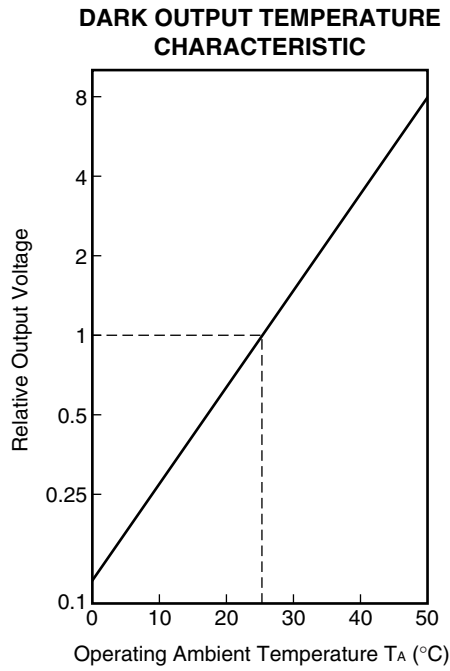
$$VCDS_i = VD_i - VO_i$$

5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σ_{CDS} using the following formula equation.

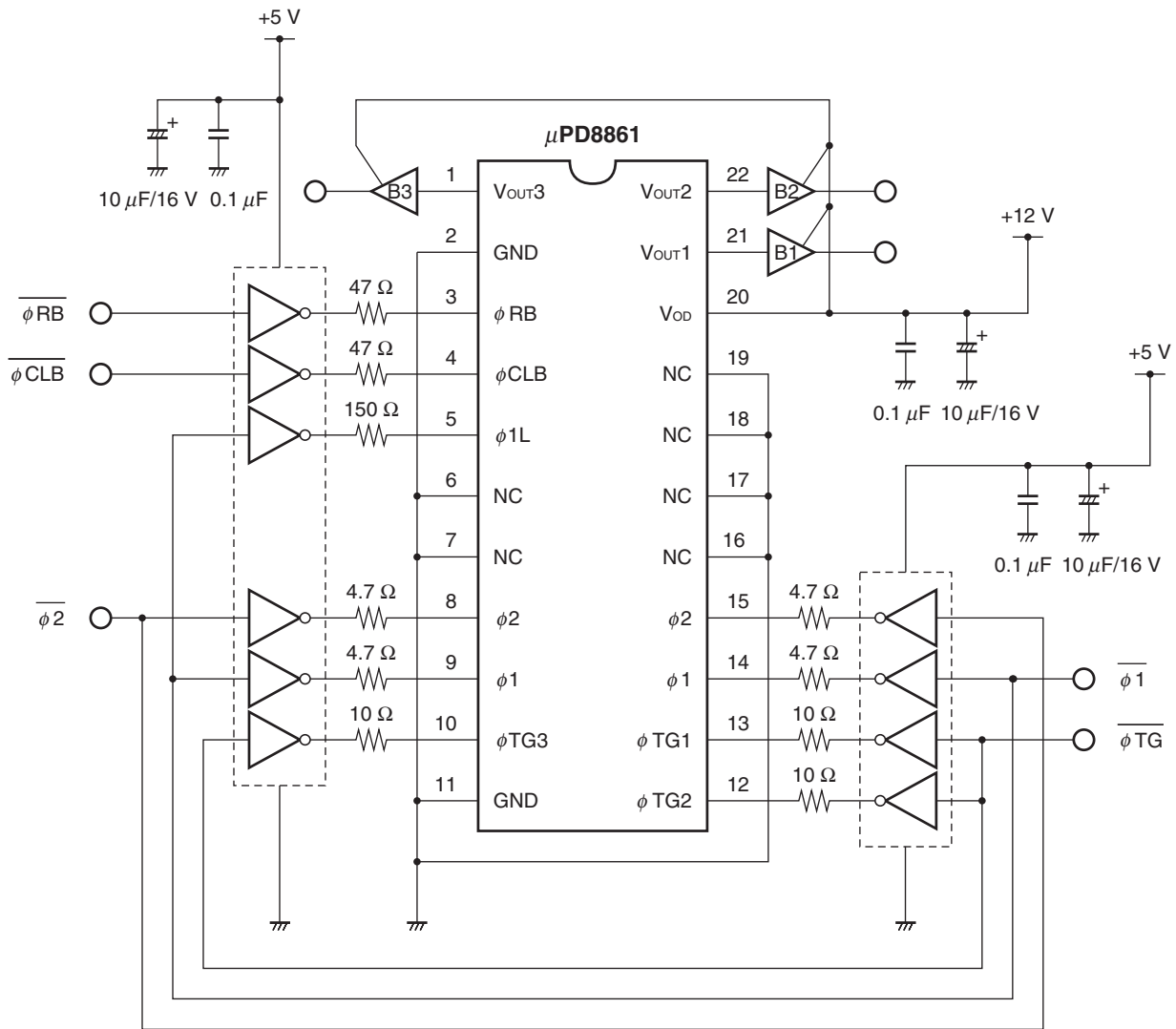
$$\sigma_{CDS} \text{ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (VCDS_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} VCDS_i$$



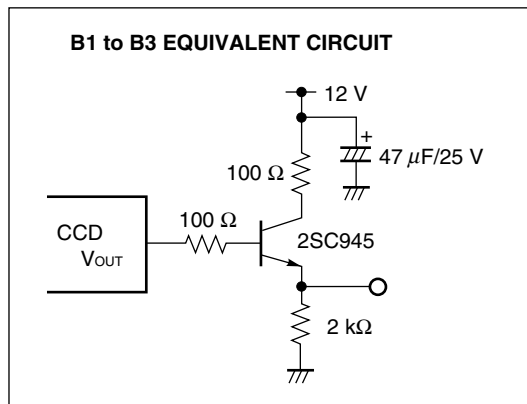
STANDARD CHARACTERISTIC CURVES (Nominal)



APPLICATION CIRCUIT EXAMPLE



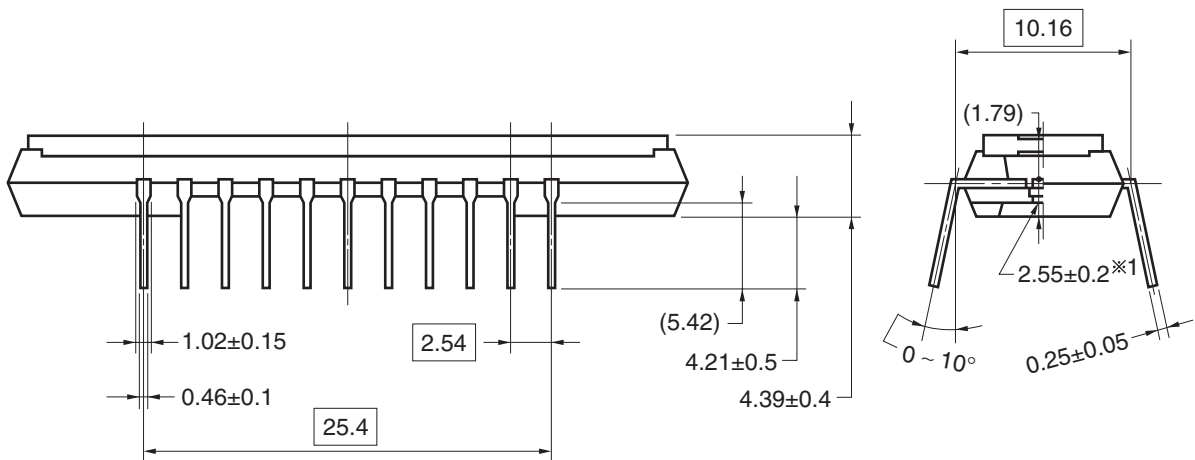
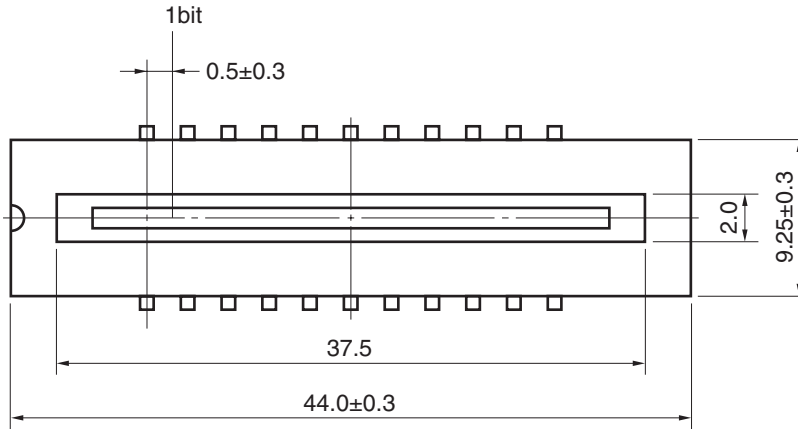
Remark The inverters shown in the above application circuit example are the 74HC04 (data rate < 2 MHz) or the 74AC04 (2 MHz ≤ data rate < 6 MHz).



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.9 × 8.35 × 0.7 ^{※2}	1.5

※1 The bottom of the package ↔ The surface of the chip

※2 The thickness of the cap over the chip

22C-1CCD-PKG6-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document “**Semiconductor Device Mounting Technology Manual**” (C10535E).

Type of Through-hole Device

μ PD8861CY : CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

Caution During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

NOTES ON CLEANING THE PLASTIC CAP

① CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

② RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap. Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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 - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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