DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD8884A

(10680 PIXELS × 4 LINES) × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8884A is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD8884A has 3 rows of (10680 × 4) staggered pixels, and each row has a dual-sided readout-type charge transfer register. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 4800 dpi/A4 color image scanners.

FEATURES

- Valid photocell : (10680 pixels × 4) × 3
- Photocell's size : 4 μm
- Line spacing : Quad staggered pixels
  96 μm (24 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 192 dot/mm A4 (210 × 297 mm) size (shorter side)
  4800 dpi US letter (8.5" × 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 5.0 MHz Max.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8884ACY-A	CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Remark The μPD8884ACY-A is a lead-free product.

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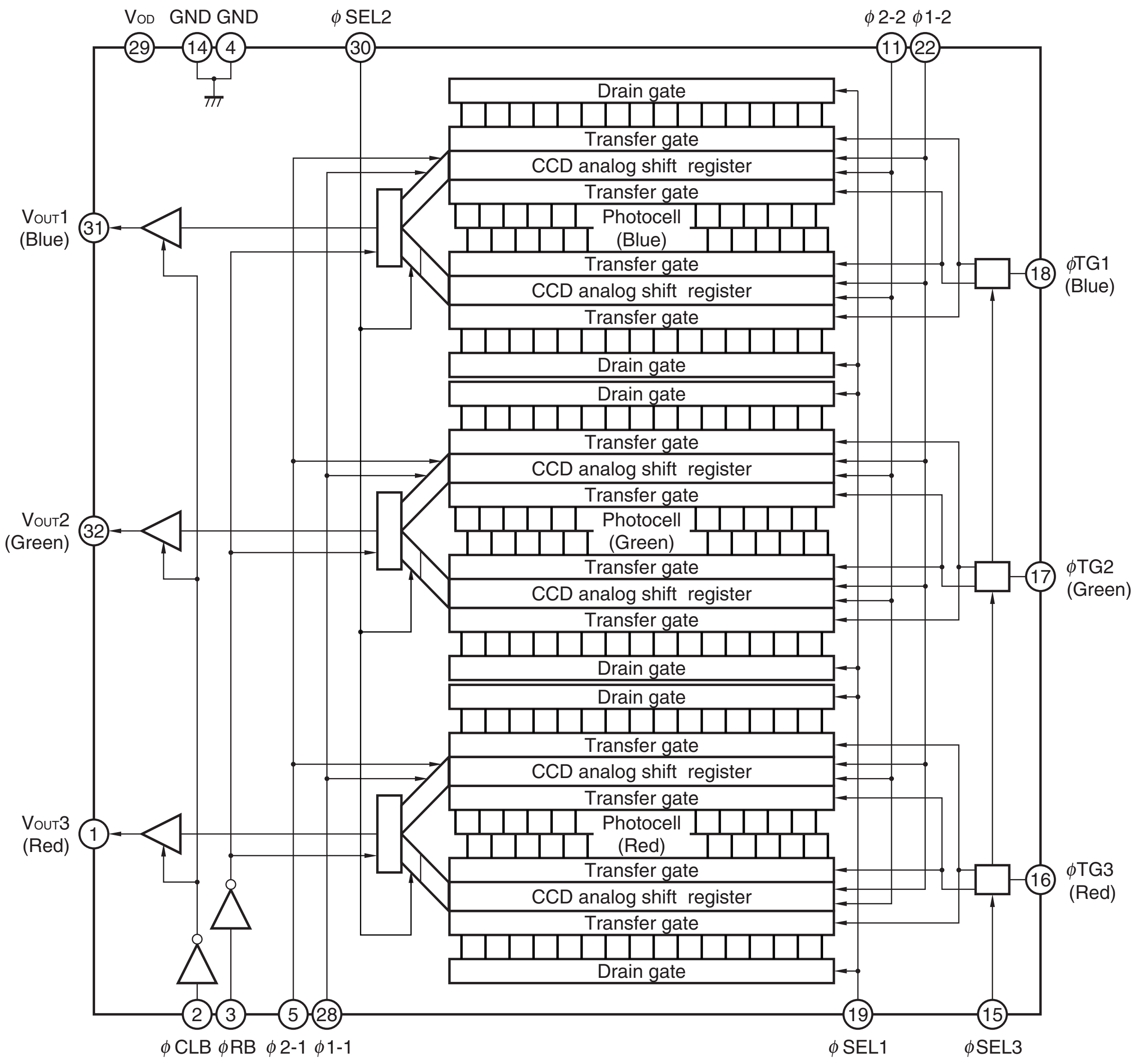
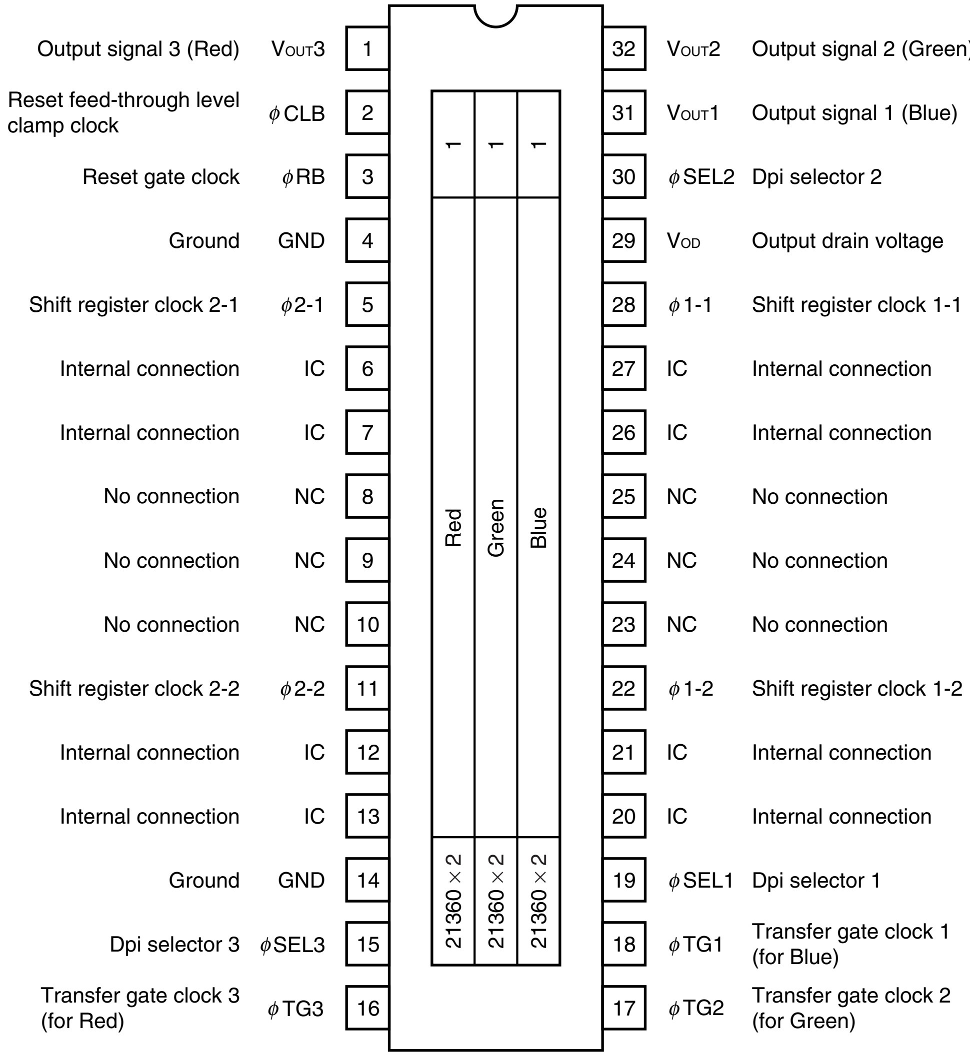
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

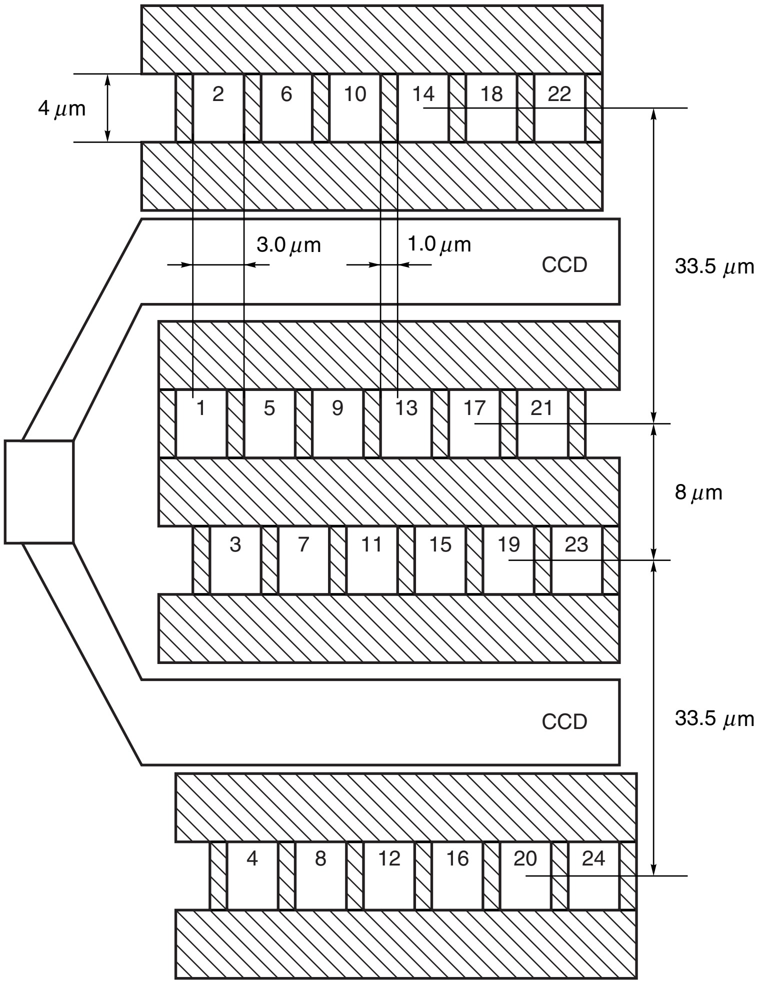
- μPD8884ACY-A



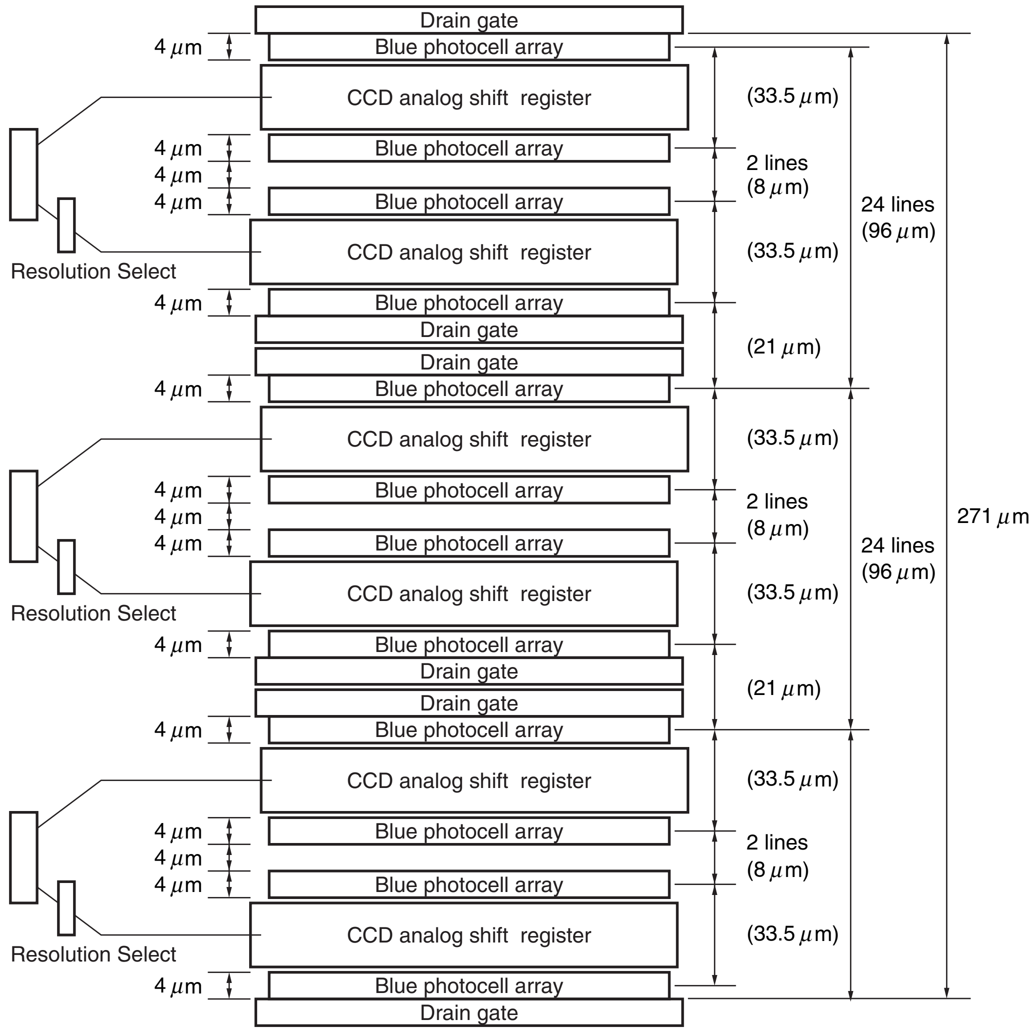
Cautions 1. Leave pins 6, 7, 12, 13, 20, 21, 26, 27 (IC) unconnected.

2. Connect the No connection pins (NC) to GND.

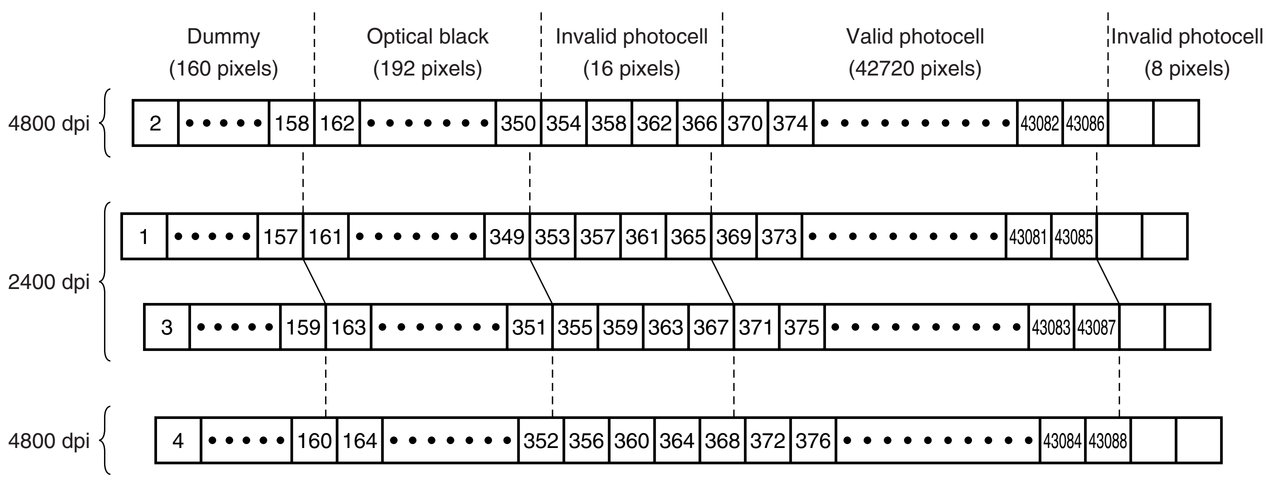
PHOTOCELL STRUCTURE DIAGRAM (4800 dpi, for each color)



PHOTOCELL ARRAY STRUCTURE DIAGRAM-1 (Line spacing)



PHOTOCELL ARRAY STRUCTURE DIAGRAM-2 (Dummy, OB, for each color)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	–0.3 to +8	V
Dpi select signal voltage	$V_{\phi SEL1}$ to $V_{\phi SEL3}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +8	V
Operating ambient temperature Note	T_A	0 to +60	°C
Storage temperature	T_{stg}	–40 to +70	°C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	11.5	12.0	12.5	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$	4.75	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$	–0.3	0	+0.3	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	–0.3	0	+0.3	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	–0.3	0	+0.3	V
Dpi select signal high level	$V_{\phi SEL1H}$ to $V_{\phi SEL3H}$	4.5	5.0	5.5	V
Dpi select signal low level	$V_{\phi SEL1L}$ to $V_{\phi SEL3L}$	–0.3	0	+0.3	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.5	5.0	5.5	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	–0.3	0	+0.3	V
Data rate	$f_{\phi RB}$	–	2.0	5.0	MHz
Clock pulse frequency	$f_{\phi 1}$, $f_{\phi 2}$	–	1.0	10.0	MHz

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 2 MHz, storage time = 11.0 ms, input signal clock = 5 V_{p-p},
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}		2.3	2.7	–	V
Saturation exposure	Red	SER		–	0.79	–	lx•s
	Green	SEG		–	0.87	–	lx•s
	Blue	SEB		–	1.35	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6	20	%
Average dark signal		ADS	Light shielding	–	0.1	4.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	2.0	8.0	mV
Power consumption		P_W		–	380	540	mW
Output impedance		Z_O		–	0.4	1.0	kΩ
Response	Red	R_R		2.38	3.40	4.42	V/lx•s
	Green	R_G		2.17	3.10	4.03	V/lx•s
	Blue	R_B		1.40	2.00	2.60	V/lx•s
Offset level Note		V_{OS}		4.5	6.0	7.5	V
Total transfer efficiency		TTE	V_{OUT} = 1.0 V Clock pulse frequency = 10 MHz	92	98	–	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	460	–	nm
Image lag		IL	V_{OUT} = 1.0 V	–	0.05	3.0	%
Response difference between inside and outside		RDIO	V_{OUT} = 1.0 V	–	1.0	6.0	%
Potocell array imbalance		PAI_{IN}	V_{OUT} = 1.0 V	–	1.0	6.0	%
		PAI_{OUT}	V_{OUT} = 1.0 V	–	1.0	6.0	%
Reset feed-through noise Note		RFTN	Light shielding	–	–500	+1000	mV
Random noise (CDS)		σCDS	Light shielding	–	1.2	–	mV

Note Refer to **TIMING CHART 2-1** to **2-3**.

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

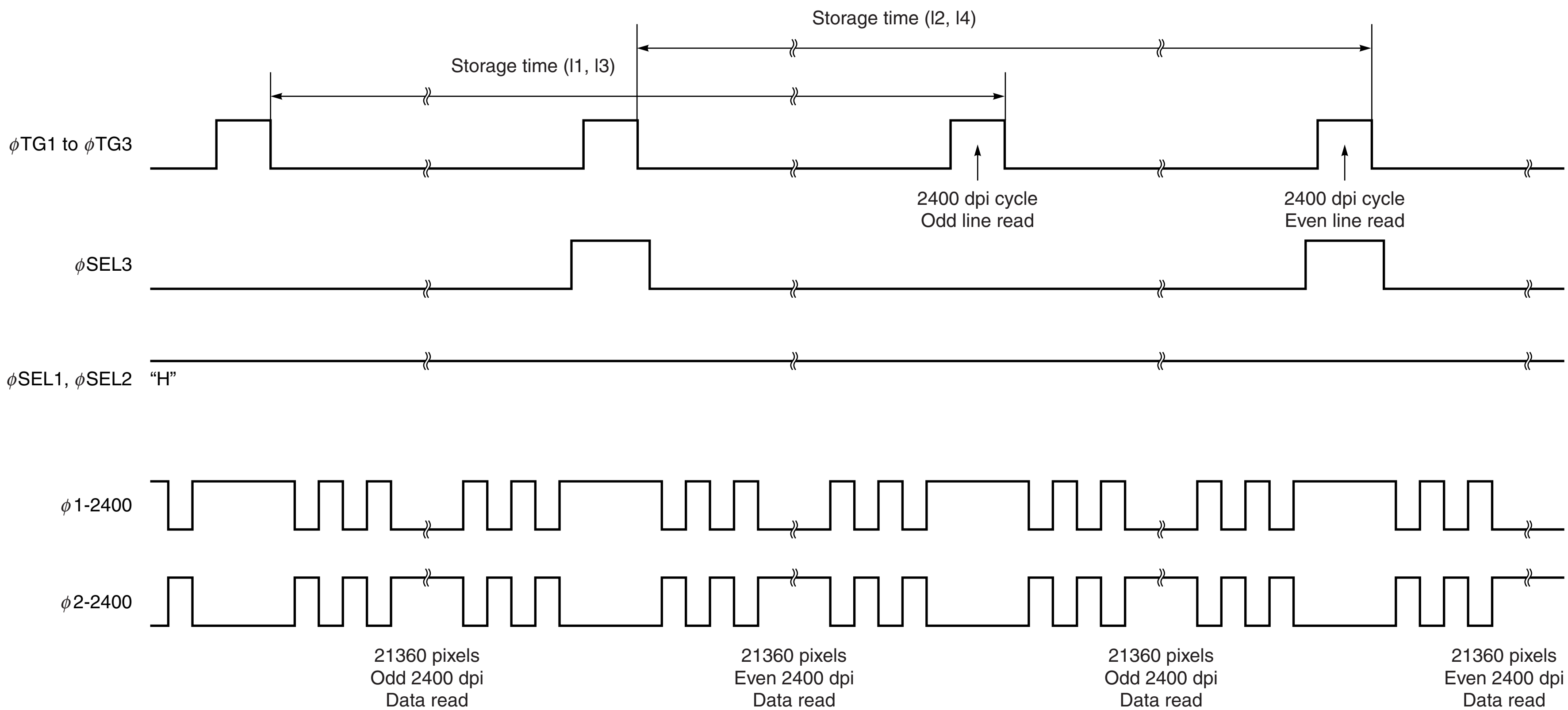
Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1\text{-}1}$	φ1-1	28	–	750	–	pF
Shift register clock pin capacitance 2	$C_{\phi 1\text{-}2}$	φ1-2	22	–	750	–	pF
Shift register clock pin capacitance 3	$C_{\phi 2\text{-}1}$	φ2-1	5	–	750	–	pF
Shift register clock pin capacitance 4	$C_{\phi 2\text{-}2}$	φ2-2	11	–	750	–	pF
Reset gate clock pin capacitance	$C_{\phi RB}$	φRB	3	–	20	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	φCLB	2	–	20	–	pF
Select signal and gain pin capacitance	$C_{\phi SEL1}$	φSEL1	19	–	20	–	pF
	$C_{\phi SEL2}$	φSEL2	30	–	20	–	pF
	$C_{\phi SEL3}$	φSEL3	15	–	20	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	φTG1	18	–	20	–	pF
		φTG2	17	–	20	–	pF
		φTG3	16	–	20	–	pF

Remark $C_{\phi 1\text{-}1}$ to $C_{\phi 2\text{-}2}$ show the equivalent capacity of the real drive including the capacity of between each clock pin (φ1-1, φ1-2, φ2-1 and φ2-2).

INPUT SIGNAL TABLE

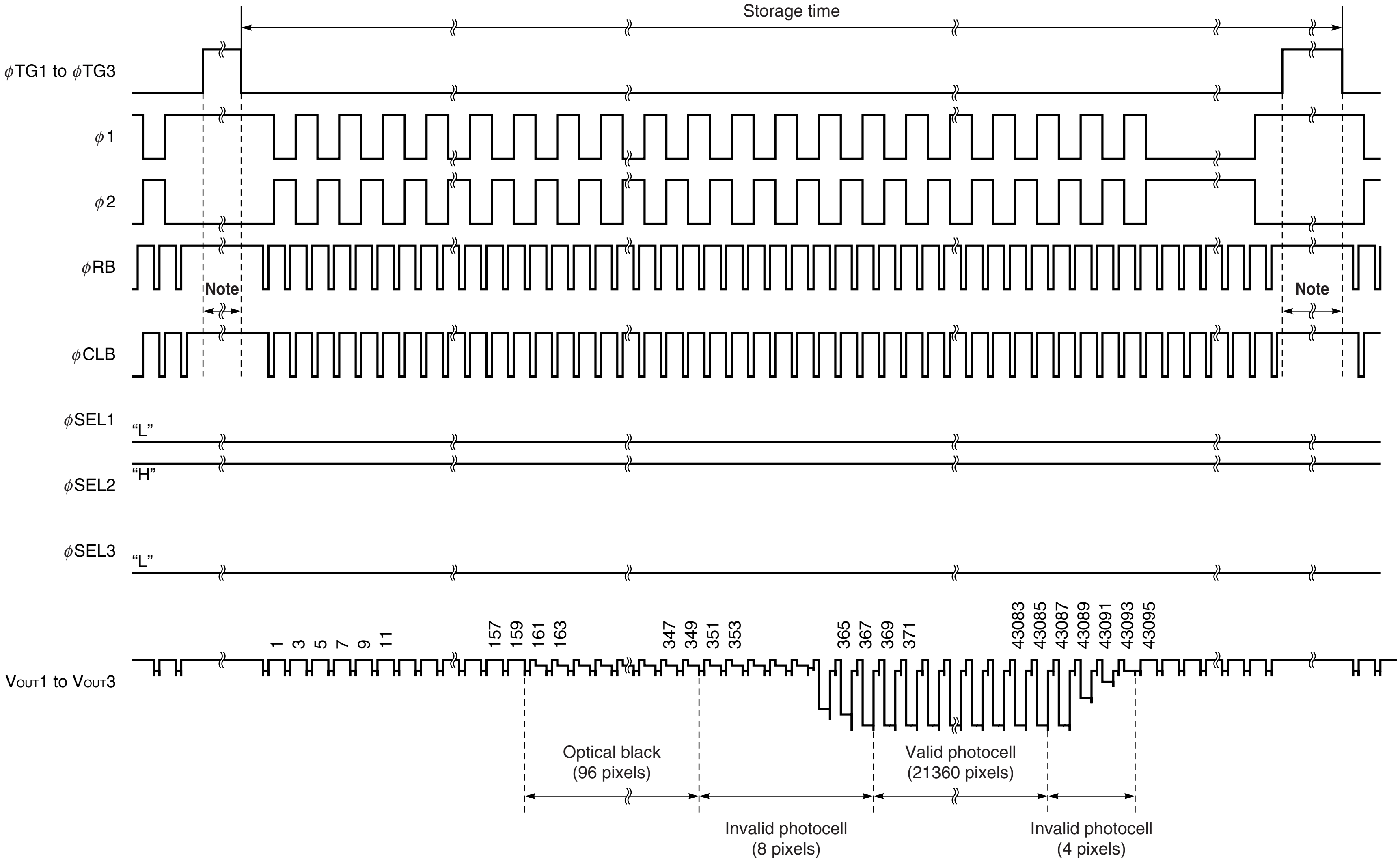
Mode	φSEL1 (Even-line enable switch)	φSEL2 (CCD-drain switch)	φSEL3 (TG-select switch)	Note
4800 dpi	High level	High level	High level	Even-line electron read photodiode to CCD
	High level	High level	Low level	Odd-line electron read photodiode to CCD
2400 dpi	Low level	High level	Low level	Odd-line electron read photodiode to CCD
				Even-line electron sink to drain
1200 dpi	Low level	Low level	Low level	1, 5, 9, 13, … : Line photodiode use 2 to 4, 6 to 8, 10 to 12, … : Sink to drain
600 dpi				

TIMING CHART 1-1 (4800 dpi, for each color)



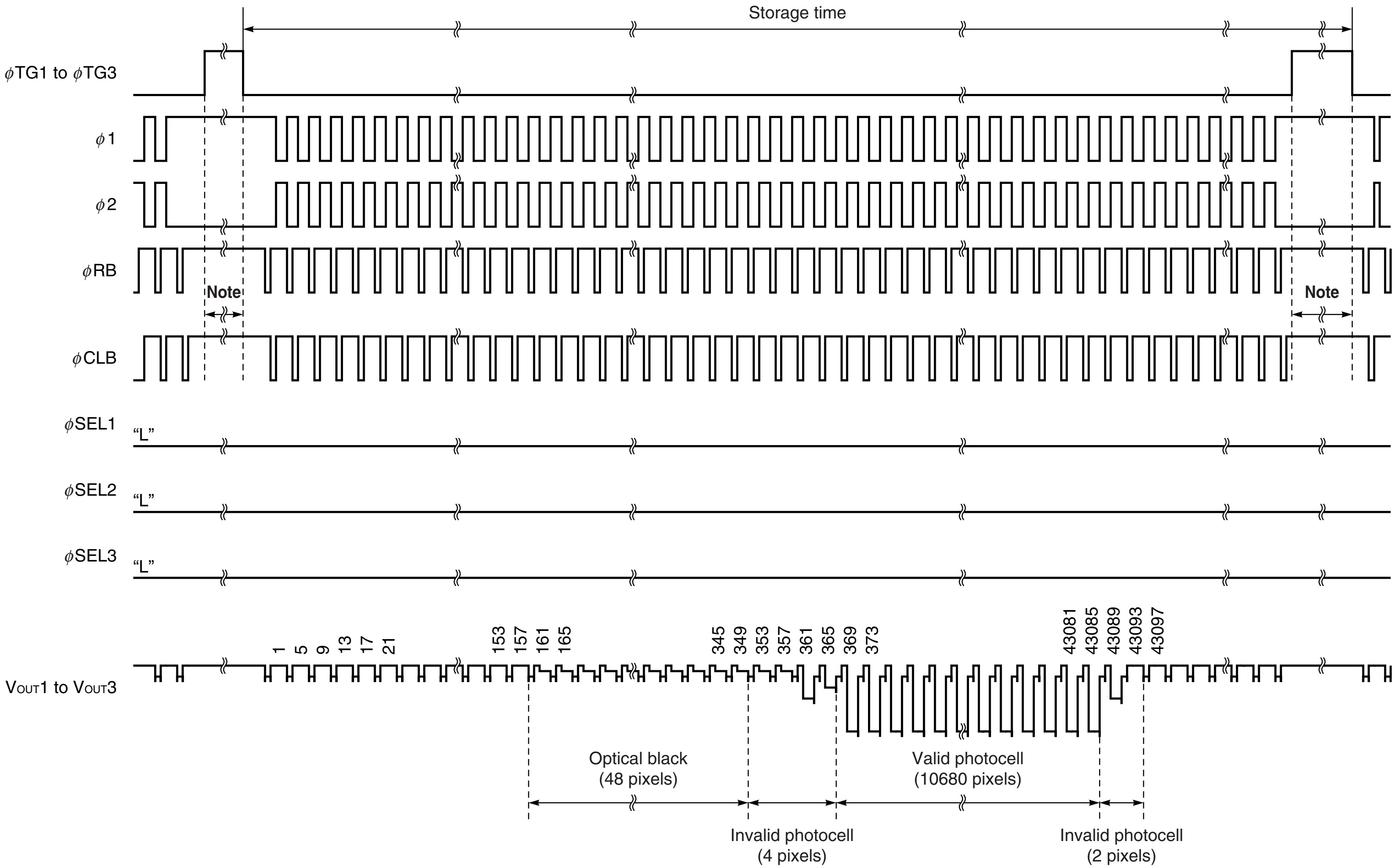
Remark Above means, storage time of each photocell array is "TG period × 2". And storage time of (I1, I3) and (I2, I4) is a half overlap each other.

TIMING CHART 1-2 (2400 dpi, for each color)



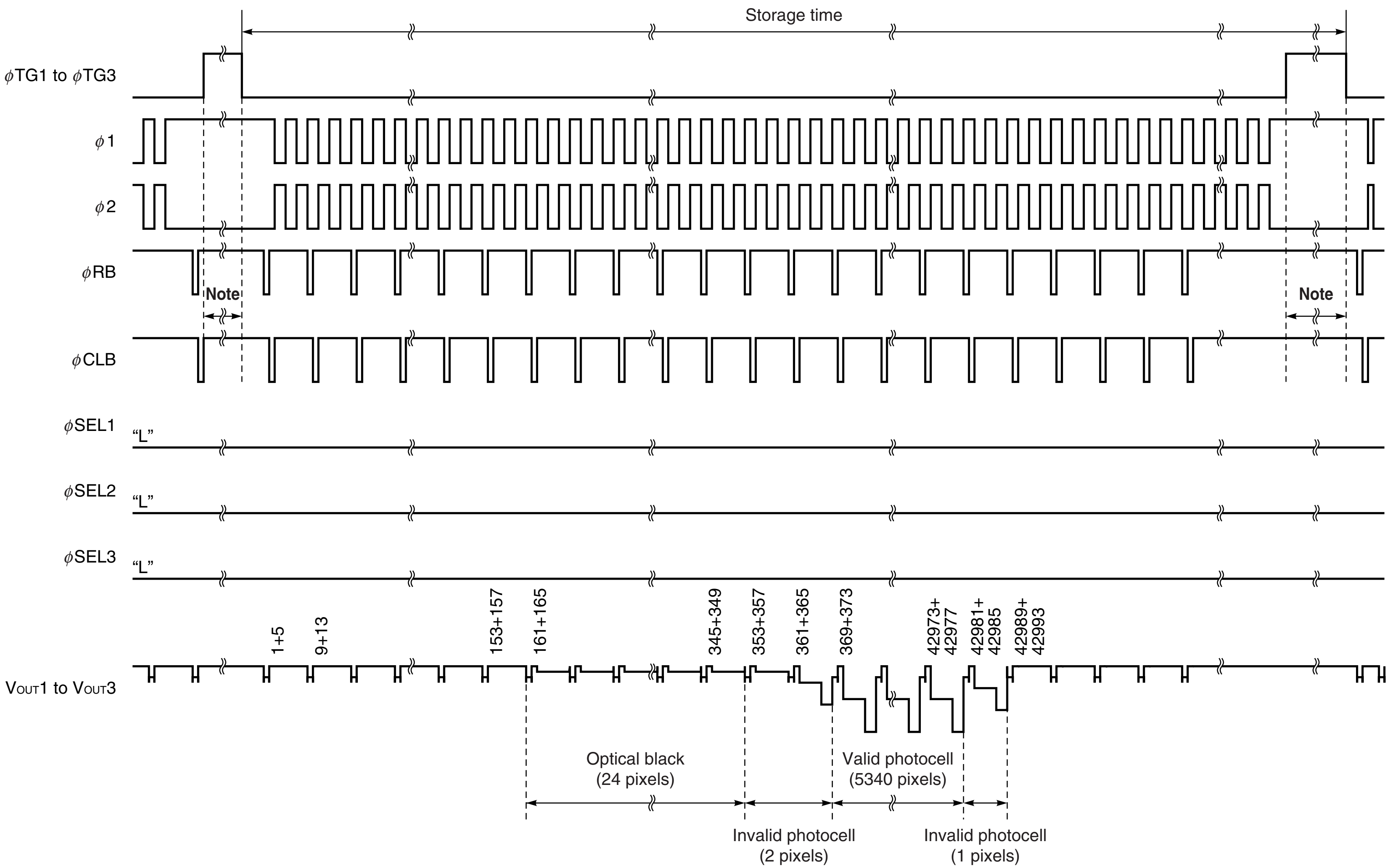
Note Set the φRB and the φCLB to high level during this period.

TIMING CHART 1-3 (1200 dpi, for each color)



Note Set the φRB and the φCLB to high level during this period.

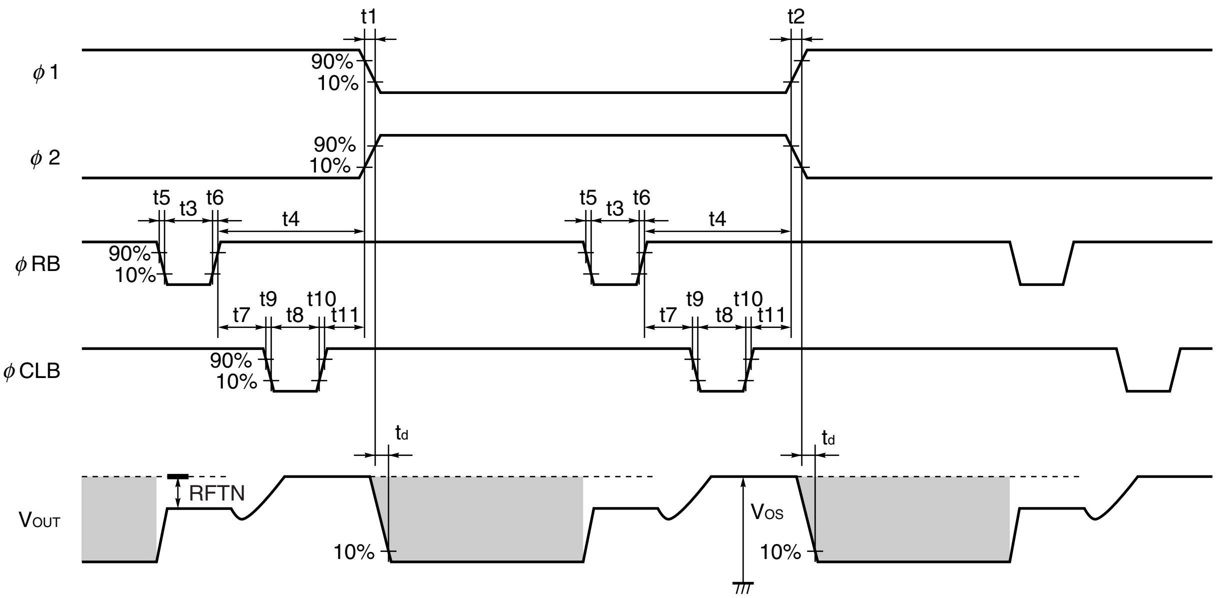
TIMING CHART 1-4 (600 dpi, for each color)



Note Set the φRB and the φCLB to high level during this period.

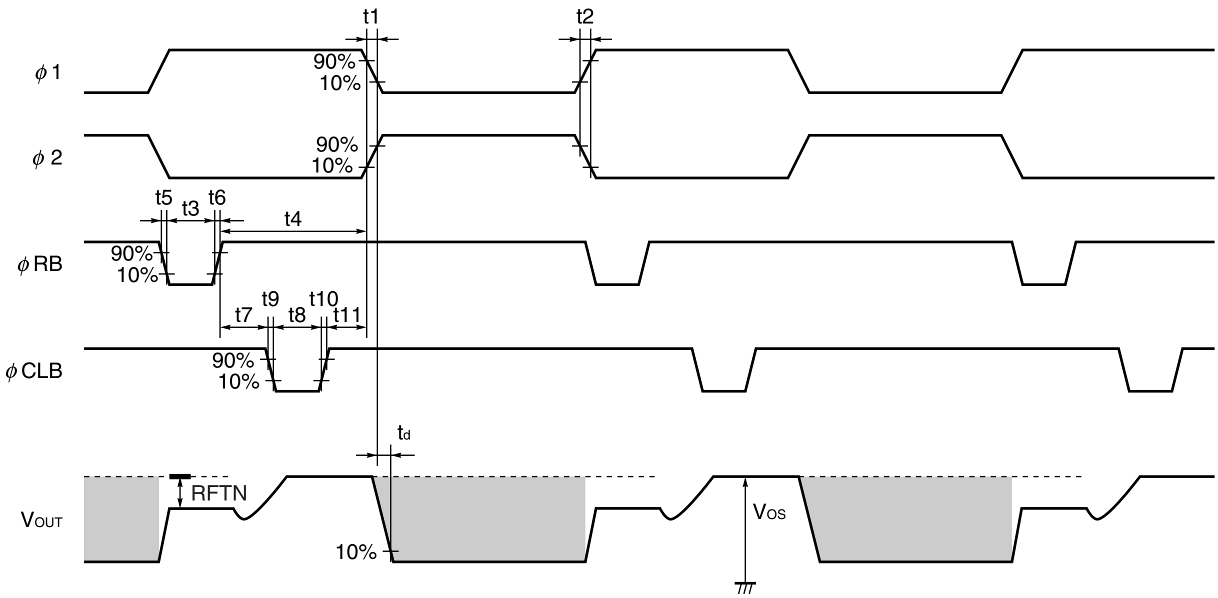
Remark 2 pixels data merge at the charge detected capacitance.

TIMING CHART 2-1 (4800 dpi / 2400 dpi, for each color)



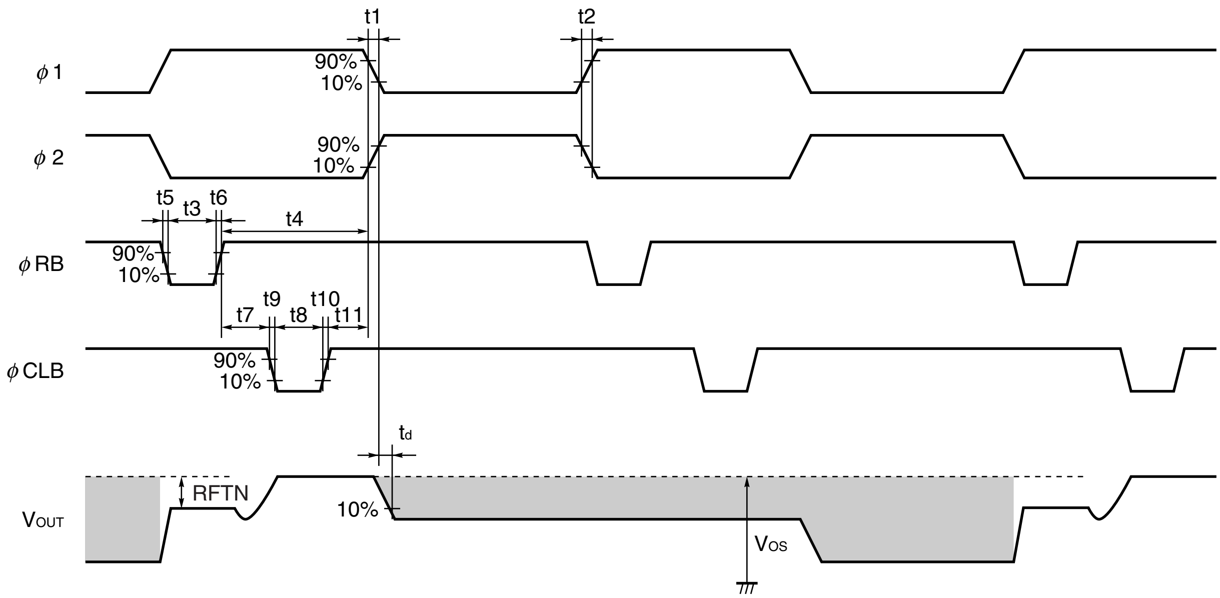
Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	30	–	ns
t3	20	100	–	ns
t4	40	150	–	ns
t5, t6	0	10	–	ns
t7	–10	+25	–	ns
t8	20	100	–	ns
t9, t10	0	10	–	ns
t11	10	25	–	ns
t_d	–	15	–	ns

TIMING CHART 2-2 (1200 dpi, for each color)



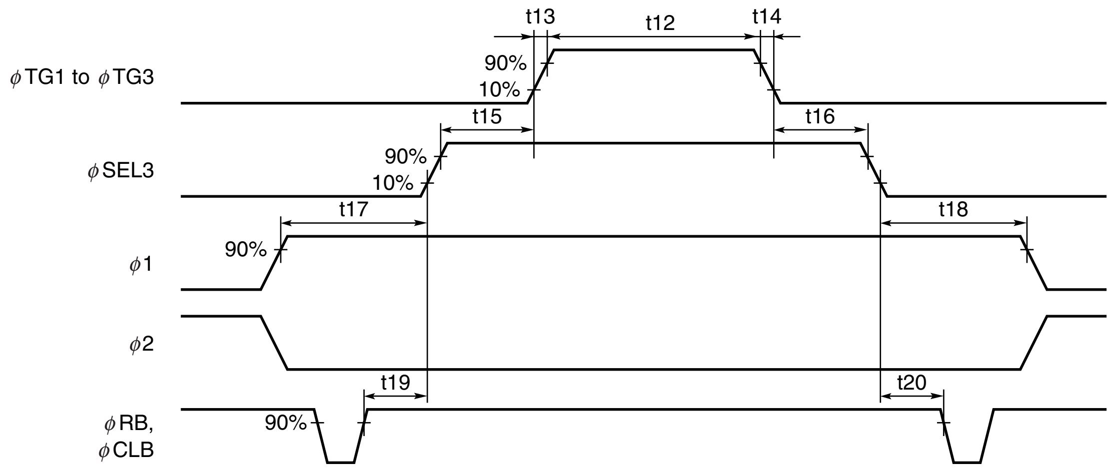
Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	30	–	ns
t3	20	100	–	ns
t4	40	150	–	ns
t5, t6	0	10	–	ns
t7	−10	+25	–	ns
t8	20	100	–	ns
t9, t10	0	10	–	ns
t11	10	25	–	ns
t_d	–	15	–	ns

TIMING CHART 2-3 (600 dpi, for each color)



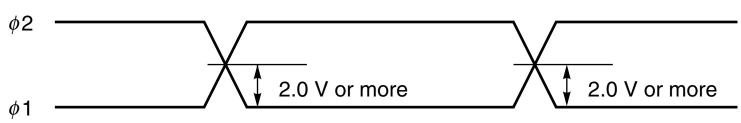
Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	30	–	ns
t3	20	100	–	ns
t4	40	150	–	ns
t5, t6	0	10	–	ns
t7	–10	+25	–	ns
t8	20	100	–	ns
t9, t10	0	10	–	ns
t11	10	25	–	ns
t_d	–	15	–	ns

TIMING CHART 3 (readout)



Symbol	Min.	Typ.	Max.	Unit
t12	8000	15000	(50000)	ns
t13, t14	0	50	–	ns
t15, t16	1000	2000	–	ns
t17	1000	2000	–	ns
t18	7000	10000	–	ns
t19, t20	500	1000	–	ns

ϕ1, ϕ2 CROSS POINTS



Remark Adjust cross points of ϕ1 and ϕ2 with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**

   Output signal voltage at which the response linearity is lost.

   Photo pixel and CCD register electron saturate level.

2. Saturation exposure : **SE**

   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : **PRNU**

   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. PRNU of 4800 dpi is calculated by the following formula.

$$PRNU_{IN}\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{IV} x_j}{IV}$$

x_j : Output voltage of valid pixel number j

IV : Number of inside valid pixels (21360 bits)

$$PRNU_{OUT}\ (\%) = \frac{\Delta y}{\overline{y}} \times 100$$

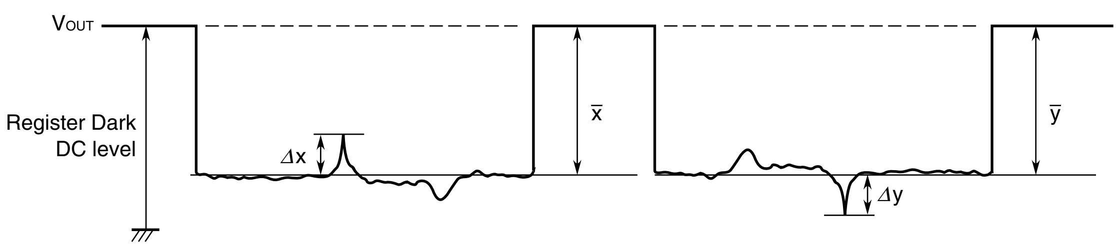
Δx : maximum of $|y_j - \overline{y}|$

$$\overline{y} = \frac{\sum_{j=1}^{IO} y_j}{IO}$$

y_j : Output voltage of valid pixel number j

IO : Number of outside valid pixels (21360 bits)

The following figure shows output waveform of 4800 dpi mode.



Inside 2400 dpi data set

Outnside 2400 dpi data set

4. Average dark signal : **ADS**

   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{\text{Vaild pixels}} d_j}{\text{Valid pixels}}$$

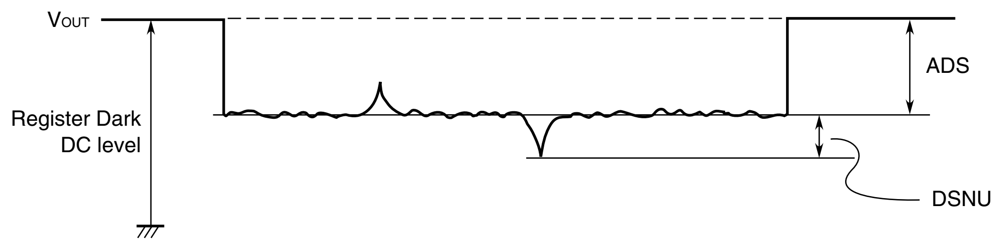
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV) : maximum of $|d_j - ADS|_{j = 1 \text{ to Valid pixels}}$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

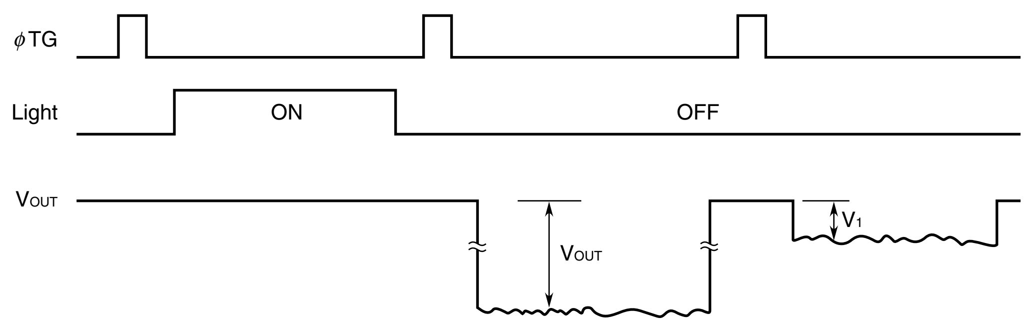
7. Response : **R**

Output voltage divided by exposure (lx•s). Note that the response varies with a light source (spectral characteristic). R of 4800 dpi is defined as following (refer to **3. Photo response non-uniformity**).

R_{IN} : $\overline{x}$ divided by exposure (lx•s)
R_{OUT} : $\overline{y}$ divided by exposure (lx•s)

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Response difference between inside and outside : **RDIO**

Difference of average output voltage between inside 2400 dpi and outside 2400 dpi (refer to **3. Photo response non-uniformity**).

$$\text{RDIO (\%)} = \frac{2\,|\,\overline{x} - \overline{y}\,|}{\overline{x} + \overline{y}} \times 100$$

10. Photocell array imbalance : **PAI**

PAI is calculated by following formula (refer to **3. Photo response non-uniformity**).

$$\text{PAI}_{\text{IN}}\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (x_{2j-1} - x_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} x_j} \times 100 \qquad \text{PAI}_{\text{OUT}}\ (\%) = \frac{\frac{2}{m}\left|\sum_{j=1}^{\frac{m}{2}} (y_{2j-1} - y_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{m} y_j} \times 100$$

x_j : Output voltage of each pixel
n : Number of valid pixels (21360 bits)

y_j : Output voltage of each pixel
m : Number of valid pixels (21360 bits)

11. Offset level : **V_{OS}**

DC level of output signal is defined as follows.

12. Reset feed-through noise : **RFTN**

Reset feed-through noise (RFTN) are defined as follows.

13. Random noise (CDS) : **σCDS**

Random noise σCDS is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). σCDS is calculated by the following procedure.

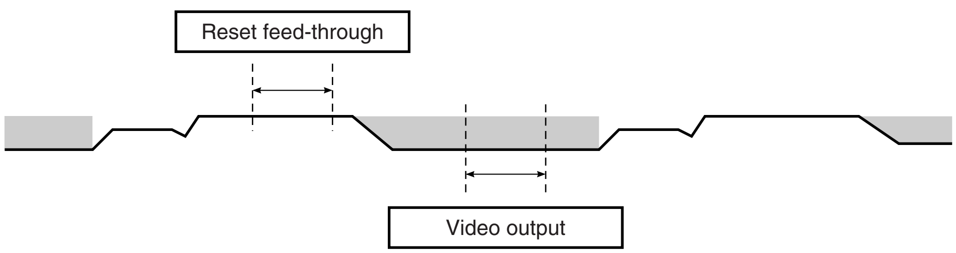
1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get "VD_i".
3. The output level is measured during the video output time averaged over 100 ns to get "VO_i".
4. The correlated double sampling output is defined by the following formula.

$$VCDS_i = VD_i - VO_i$$

5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σCDS using the following formula equation.

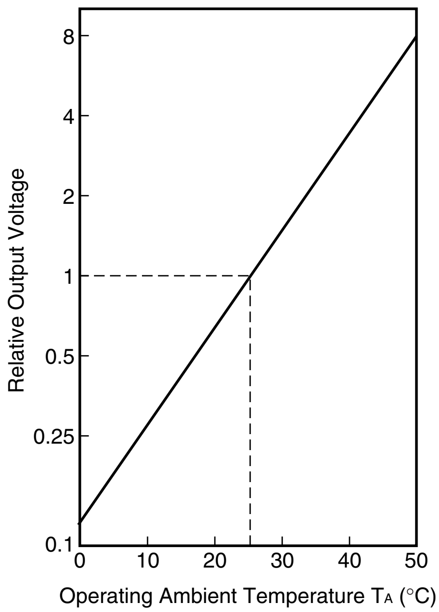
$$\sigma\text{CDS (mV)} = \sqrt{\frac{\sum_{i=1}^{100}(VCDS_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} VCDS_i$$

The following figure shows output waveform (valid photocell under dark condition).

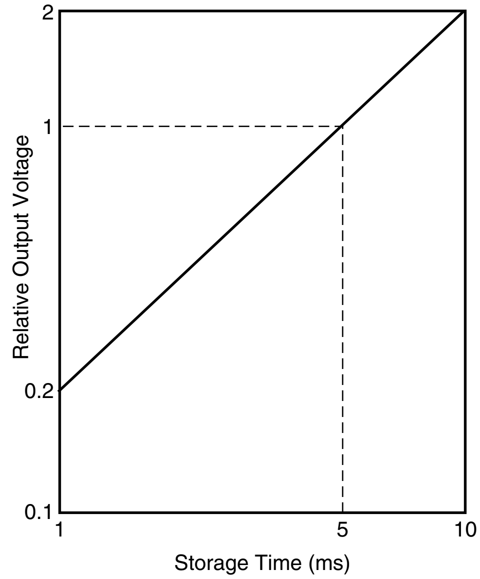


STANDARD CHARACTERISTIC CURVES (Reference Value)

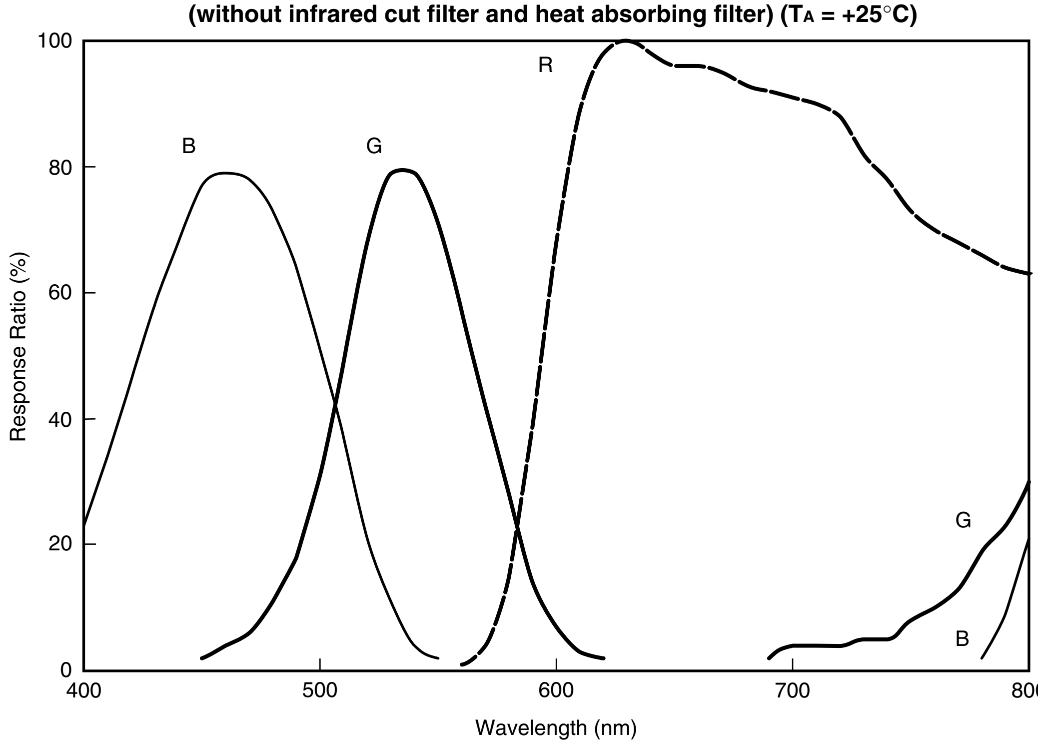
DARK OUTPUT TEMPERATURE CHARACTERISTIC



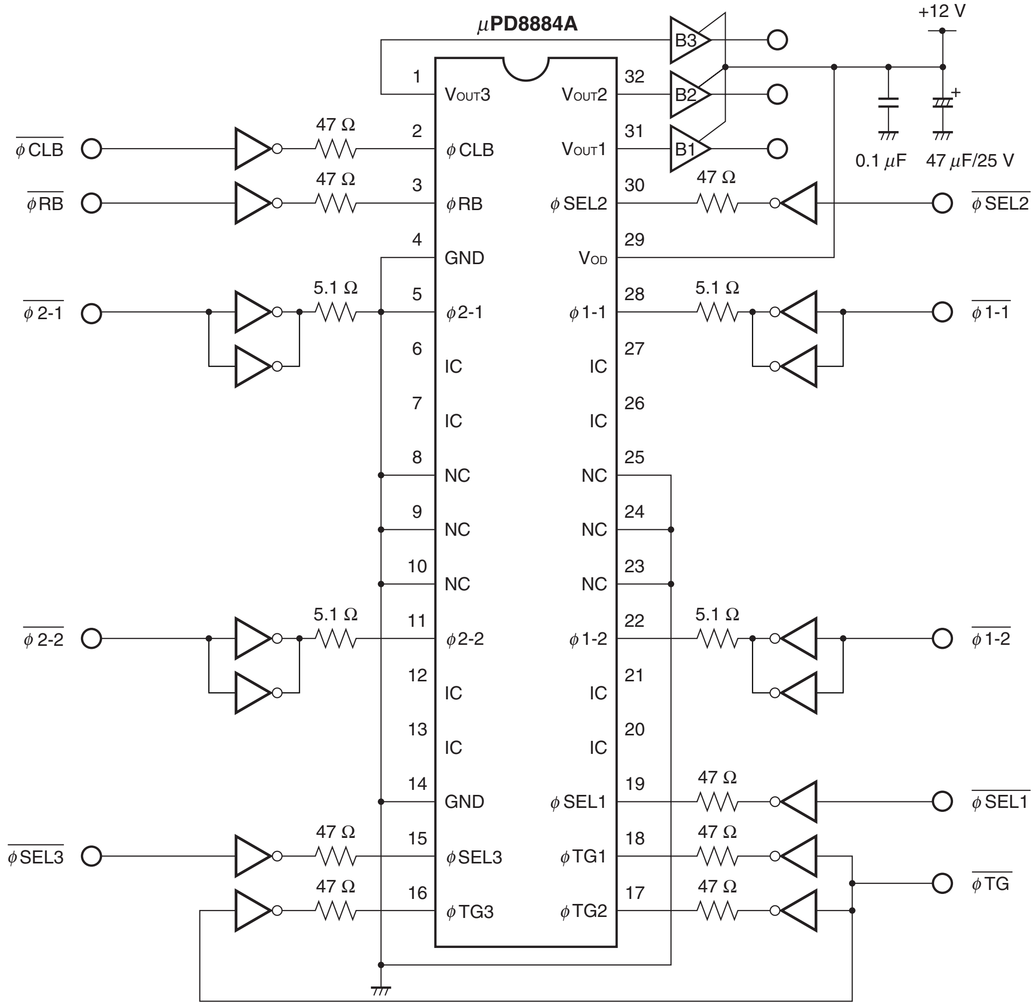
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (TA = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (TA = +25°C)



APPLICATION CIRCUIT EXAMPLE



Cautions 1. Leave pins 6, 7, 12, 13, 20, 21, 26, 27 (IC) unconnected.

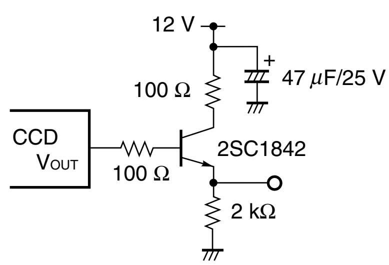
2. Connect the No connection pins (NC) to GND.

Remarks 1. φRB, φCLB, φTG1 to φTG3 and φSEL1 to φSEL3 driving inverters shown in the above application circuit example are the 74HC04.

φ1-1 to φ2-2 driving inverters shown in the above application circuit example are the 74HC04 (≤ 2.0 MHz) or the 74AC04 (> 2.0 MHz).

2. Inverters B1 to B3 in the above application circuit example are shown in the figure below.

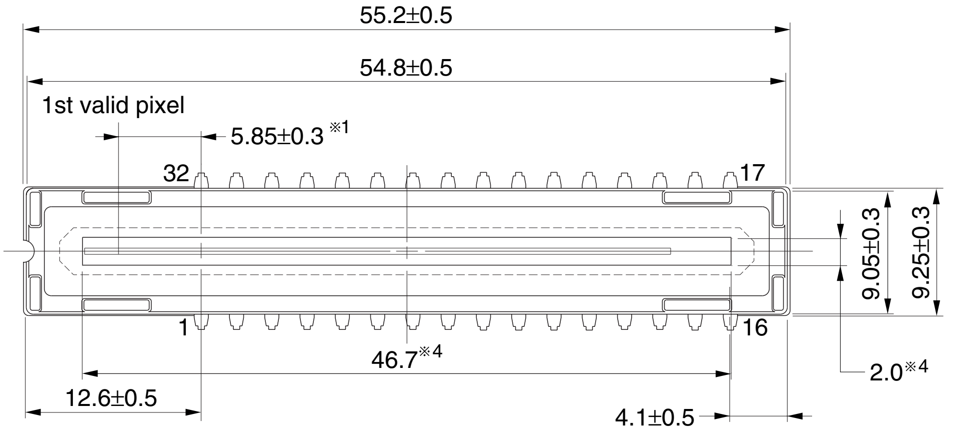
B1 to B3 EQUIVALENT CIRCUIT

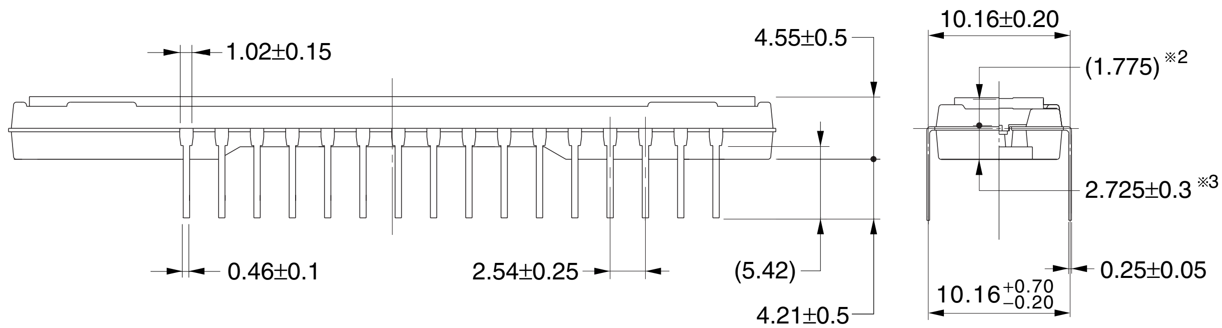


PACKAGE DRAWING

μPD8884ACY
CCD LINEAR IMAGE SENSOR 32-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)





Name	Dimensions	Refractive index
Plastic cap	52.2×6.4×0.8 (0.7※5)	1.5

※1 1st valid pixel ←→ The center of the pin1
※2 The surface of the CCD chip ←→ The top of the cap
※3 The bottom of the package ←→ The surface of the CCD chip
※4 Mirror finishied surface
※5 Thickness of mirror finished surface

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Through-hole Device

μPD8884ACY-A : CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.

Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.