

February 1988

### Description

The  $\mu$ PD9601AD and  $\mu$ PD9602AD are PCM codec-filter combo chips. A-law and  $\mu$ -law compatible, respectively. These monolithic CMOS LSIs include phase-locked loops (PLL) that derive internal signal processing clocks from the transmit and receive frame sync clock inputs.

### Features

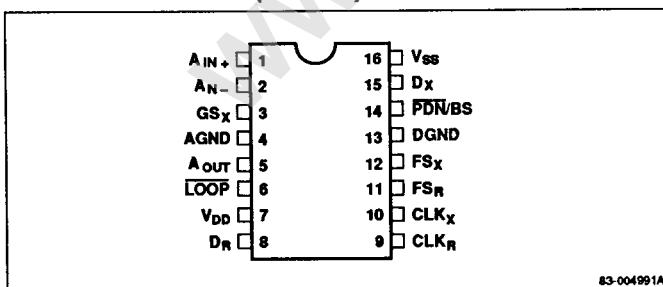
- Transmit input operational amplifier
- Transmit active lowpass filter and switched-capacitor bandpass filter
- Autozero circuit
- Receive unbalanced 600- $\Omega$  output power amplifier
- Receive switched-capacitor lowpass filter
- Digital serial I/O interface circuit
- A-law (9601AD) and  $\mu$ -law (9602AD) companding
- Precision reference voltage circuit
- Synchronous or asynchronous operation
- Data rate, 64 kb/s to 2.048 Mb/s
- Low power dissipation
  - 50 mW normal mode
  - 5 mW power-down or standby mode
- 16-pin ceramic DIP

### Ordering Information

Part No.	Companding	Package Type
$\mu$ PD9601AD	A-law	16-pin ceramic DIP (300 mil)
$\mu$ PD9602AD	$\mu$ -law	

### Pin Configuration

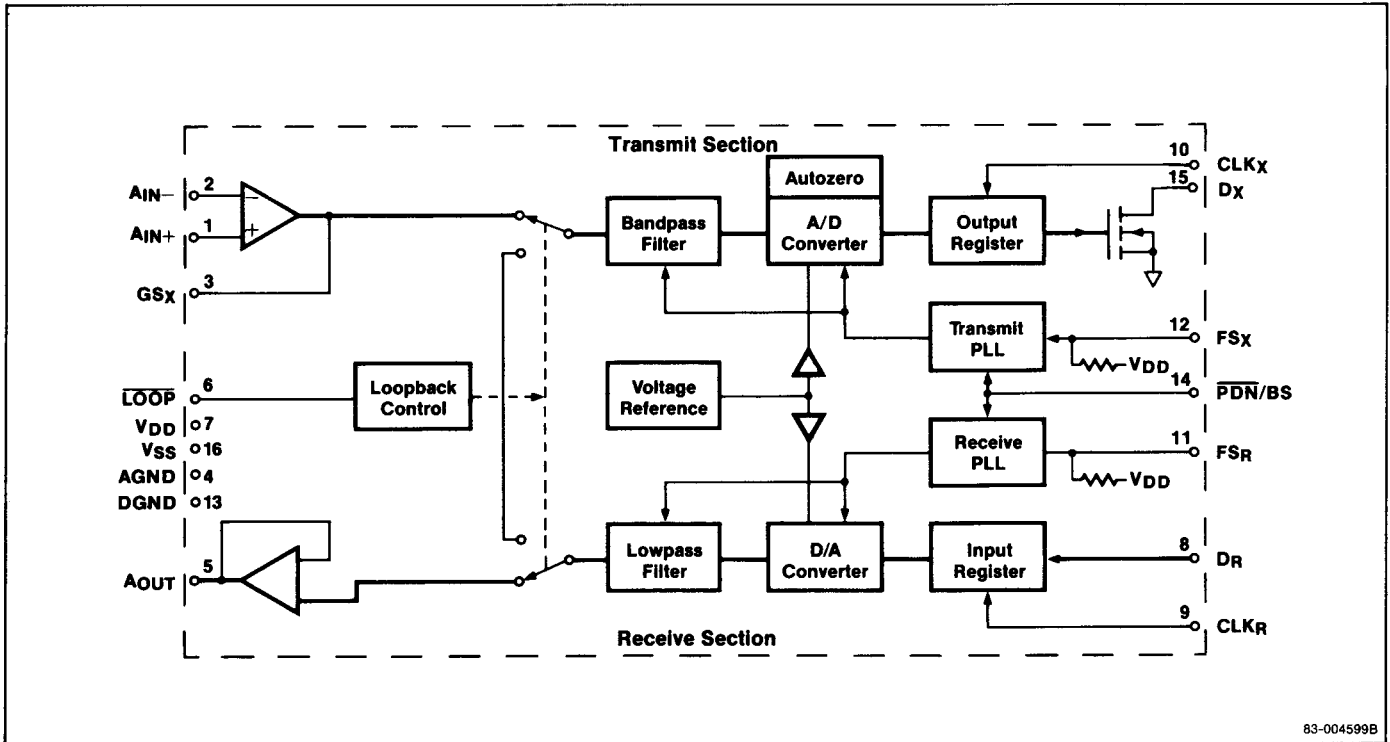
#### 16-Pin Ceramic DIP (300 mil)



### Pin Identification

Pin No.	Symbol	Function
1	AIN+	Transmit analog input; noninverting input to opamp.
2	AIN-	Transmit analog input; inverting input to opamp.
3	GS <sub>X</sub>	Transmit opamp external gain setting resistor.
4	AGND	Analog ground; no internal connection to digital ground.
5	AOUT	Receive analog output from power amplifier; unbalanced 600 $\Omega$ .
6	LOOP	Input control for analog loopback test. TTL level; internal pullup. An open or connection to V <sub>SS</sub> disables loopback.
7	V <sub>DD</sub>	Positive 5-volt power supply (+5 $\pm$ 0.25).
8	D <sub>R</sub>	Receive PCM data input; TTL level.
9	CLK <sub>R</sub>	Receive data clock input, 64 kHz to 2.048 MHz; TTL level. For CLK <sub>X</sub> , either synchronous or asynchronous operation can be used; however, for FS <sub>R</sub> , only synchronous operation can be used.
10	CLK <sub>X</sub>	Transmit data clock input, 64 kHz to 2.048 MHz; TTL level. For CLK <sub>R</sub> , either synchronous or asynchronous operation can be used; however, for FS <sub>X</sub> , only synchronous operation can be used.
11	FS <sub>R</sub>	Receive frame sync clock input. TTL level; internal pullup.
12	FS <sub>X</sub>	Transmit frame sync clock input. TTL level; internal pullup.
13	DGND	Digital ground; no internal connection to analog ground.
14	P $\overline{D}$ N/BS	Control input for power-down (9601AD, 9602AD) and bit steal (9602AD); TTL level. On 9601AD, a low level initiates power-down. On 9602AD, the low level must be maintained for more than seven frames; a low-to-high or high-to-low transition within six frames activates bit steal.
15	D <sub>X</sub>	Transmit PCM data output (open drain).
16	V <sub>SS</sub>	Negative 5-volt power supply (-5 $\pm$ 0.25).

**Block Diagram**



83-004599B

**Operational Description**

**Power-Up**

The μPD9601AD and μPD9602AD have internal reset circuits that protect other devices on the PCM highway during the power-up sequence. For about 5 ms after power is applied, digital output D<sub>X</sub> is held in a high-impedance state. Analog circuits such as filters, sample-and-hold, and D/A converters begin functioning after a 15-ms settling period.

**Power-Down Mode**

Setting the PDN/BS pin to TTL low level initiates the power-down mode. Digital output D<sub>X</sub> goes to high-impedance state and all circuits are disabled except the power-down controller, data clocks, frame sync buffers, and PLLs.

A TTL high level on the PDN/BS pin restores normal operation after the same delays as in power-up, but without the PLL lock-in time.

**Standby Mode**

In standby mode, each section is powered down independently by an open circuit or a TTL low level on FS<sub>X</sub> (transmit section) or FS<sub>R</sub> (receive section).

**PCM Data Transmission**

As shown in the transmit 1 timing waveform, if FS<sub>X</sub> is high at the rising edge of CLK<sub>X</sub>, the MSB of the channel PCM word is output at the D<sub>X</sub> pin. Similarly, bits 2 through 8 are output at the next seven rising edges of CLK<sub>X</sub>, after which the D<sub>X</sub> pin is restored to the high-impedance state.

The transmit 2 timing waveform shows the condition in which CLK<sub>X</sub> leads FS<sub>X</sub>. In either transmit 1 or transmit 2, the overlapping high-level width of the two clocks is at least 100 ns.

The receive timing waveforms are similar to the transmit timing waveforms except data is clocked in and latched on the falling edge of CLK<sub>R</sub>.

## Bit Stealing, μPD9602AD Only

Over a 12-frame interval, in frames 1-5 and 7-11, the receive section decodes the vf information in the 8-bit channel pcm words. In signaling frames 6 and 12, the LSB (bit 8) is assigned to convey the channel signaling state. (Bit 8 is "stolen," leaving just 7 bits for vf information.) Although the μPD9602AD does not have a channel signaling interface, it performs 7-bit vf decoding in signaling frames 6 and 12. Design of the D/A converter minimizes the deterioration of gain tracking and signal-to-distortion characteristics resulting from 7-bit vf transmission in one frame out of every six.

To activate bit stealing, the associated digital equipment applies a control signal to the PDN/BS pin. As shown in the receive timing waveforms, the BS signal is low and high in alternate signaling frames. In the next time slot after bit 8 of each channel pcm word in signaling frames, a pulse in the BS signal tells the decoder to ignore bit 8 and decode bits 1-7.

If the signal on the PDN/BS pin is a low level for more than seven frames, the μPD9602AD goes into the power-down mode.

## Analog Loopback Test

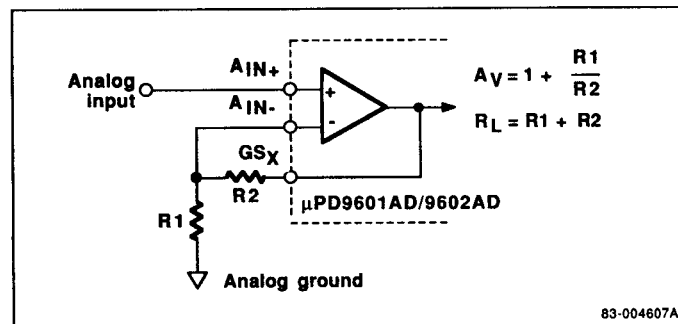
Setting the LOOP pin to TTL low level establishes the analog loopback test mode in which vf receive is looped to vf transmit internally. A 0-dBm0 digital tone input at D<sub>R</sub> should emerge as a 0-dBm0 digital tone output at D<sub>X</sub>.

The LOOP pin, which is pulled up internally, should be left open or connected to V<sub>SS</sub> when the channel is not in this test mode.

## Transmit Gain

Figure 1 shows the transmit opamp connected in the noninverting mode and gives formulas for voltage gain A<sub>V</sub> and load resistance R<sub>L</sub>. By selecting the values of resistors R1 and R2, voltage gain can be set between 0 and 15 dB. Load resistance should be 10 kΩ to 20 kΩ, and load capacitance C<sub>L</sub> should be less than 100 pF.

Figure 1. Transmit Gain Setting



## Ground

In the board layout, the AGND and DGND pins should be connected together and tied to the analog ground bus beneath the chip at the midpoint between the two pins.

## Power-Up Sequence

In the power-up process, the two power pins and two ground pins should be activated in one of the five sequences listed below.

- V<sub>SS</sub>, AGND, DGND, V<sub>DD</sub>
- V<sub>SS</sub>, AGND-DGND, V<sub>DD</sub>
- V<sub>SS</sub>, V<sub>DD</sub>, AGND-DGND
- V<sub>DD</sub>, V<sub>SS</sub>, AGND-DGND
- AGND-DGND, V<sub>SS</sub>, V<sub>DD</sub>

## Absolute Maximum Ratings

T<sub>A</sub> = +25°C; V<sub>DG</sub> = V<sub>AG</sub> = 0

Parameter	Symbol	Rating	Conditions
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0 V	
	V <sub>SS</sub>	-7.0 to +0.3 V	
Analog input voltage	V <sub>AIN</sub>	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3 V	Pins A <sub>IN+</sub> , A <sub>IN-</sub> , GS <sub>X</sub> , GS <sub>R</sub>
Digital input voltage	V <sub>DIN</sub>	-0.3 to V <sub>DD</sub> + 0.3 V	
Voltage applied to digital output pin D <sub>X</sub>	V <sub>DOUT</sub>	-0.3 to V <sub>DD</sub> + 0.3 V	
Power dissipation	P <sub>T</sub>	500 mW	
Operating temperature	T <sub>OPT</sub>	0 to +70°C	
Storage temperature	T <sub>STG</sub>	-65 to +150°C	
Soldering temperature	T <sub>SOLD</sub>	+260°C	Less than 10 seconds

**Recommended Operating Conditions**

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{DD} = +5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{SS} = -5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{DG} = V_{AG} = 0$  (Note 1)

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
<b>Power</b>						
Supply voltage	$V_{DD}$	+4.75	+5.00	+5.25	V	
	$V_{SS}$	-5.25	-5.00	-4.75	V	
<b>Analog</b>						
Transmit amplifier						
Input analog voltage	$V_{AX}$	-3.0		3.0	V	Pin $A_{IN+}$
Gain setting range	$GR_{AX}$	0		15	dB	
Load resistance	$RL_{AX}$	10			kΩ	Pins $GS_X$ , $A_{IN-}$ (Note 2)
Load capacitance	$CL_{AX}$			100	pF	
Receive amplifier						
Load resistance	$RL_{AR}$	600	160		Ω	
Load capacitance	$CL_{AR}$			100	pF	
<b>Digital</b>						
Input at digital pins						
Low voltage	$V_{IL}$	0		0.8	V	
High voltage	$V_{IH}$	2.0		$V_{DD}$	V	
<b>Clock</b>						
Data clock frequency	$f_{CLK}$ ( $1/t_{CY}$ )	64		2048	kHz	
Data clock width	$t_{CLK}$	200			ns	
Frame synchronous clock						
Frequency	$f_S$		8.0		kHz	
High-level width	$t_{WHS}$	200			ns	
Low-level width	$t_{WLS}$	8			μs	
Frame sync clock and data clock, overlapping high-level width	$t_{WHSC}$	100			ns	
Clock rise time	$t_R$			50	ns	
Clock fall time	$t_F$			50	ns	
Synchronous timing margin						
	$t_{CSD1}$			100	ns	
	$t_{CSD2}$	40			ns	
$D_R$ setup time	$t_{DSR}$	65			ns	Note 3
$D_R$ hold time	$t_{DHR}$	120			ns	
BS setup time	$t_{BSR}$	200			ns	
BS hold time	$t_{BHR}$	200			ns	

**Notes:**

- (1) Pins AGND and DGND should be connected together close to the device's analog ground pin.
- (2) Pins  $GS_X$  and  $A_{IN-}$  should be connected together if the input gain is 0 dB.
- (3) The rise/fall time of the digital input and clock signals used in timing tests is about 5 ns.

## DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{DD} = +5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{SS} = -5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{DG} = V_{AG} = 0$ ;

$f_{CLKR} = f_{CLKX} = 2048\text{ kHz}$

All outputs are unloaded unless otherwise specified.

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
<b>Power</b>						
Normal operating current	$I_{DD}$		5.0	10.0	mA	
	$ I_{SS} $		5.0	10.0	mA	
Power-down current	$I_{DDPD1}$			1.0	mA	100 ms after $\overline{P\overline{D}N}$ is set to low
	$ I_{SSPD1} $			0.2	mA	
Standby current	$ I_{DDPD2} $			1.0	mA	100 ms after $FS_X$ and $FS_R$ are set to low
	$ I_{SSPD2} $			0.2	mA	
<b>Digital Interface</b>						
Digital input current	$I_{ID}$	-10		10	$\mu\text{A}$	Pins $\overline{P\overline{D}N}/BS$ , $D_R$ , $CLK_X$ , $CLK_R$ ; $V_{DIN} = 0$ to $V_{DD}$
Pullup current	$I_{IL}$	-100	-4	-0.5	$\mu\text{A}$	Pins $FS_X$ , $FS_R$ , $\overline{L\overline{O\overline{O}P}}$ ; $V_{DIN} = 0\text{ V}$
Digital output leakage current	$I_L$	-10		10	$\mu\text{A}$	Pin $D_X$ ; $V_{DIN} = 0$ to $V_{DD}$
Output low voltage	$V_{OL}$			0.4	V	Pin $D_X$ ; $R_L = 500\ \Omega$ ; $I_{OL} = 0.8\text{ mA}$
Output high voltage	$V_{OH}$	$V_{DD} - 0.3$			V	Pin $D_X$ ; $I_{OH} \leq 150\ \mu\text{A}$
Digital output capacitance	$C_{OD}$			15	pF	$f = 1\text{ MHz}$
Digital input capacitance	$C_{ID}$			10	pF	
<b>Transmit Amplifier</b>						
Input leakage current	$I_B$	-10	0	10	$\mu\text{A}$	Pins $A_{IN+}$ , $A_{IN-}$ ; $V_{AIN} = -3.0$ to $3.0\text{ V}$
Input resistance	$R_{IN}$	50			k $\Omega$	$f = 1\text{ MHz}$
Input offset voltage	$V_{IO}$	-500		500	mV	Pin $A_{IN+}$
Output offset voltage	$V_{OG}$	-50		50	mV	Pin $GS_X$ ; $R_L = 10\text{ k}\Omega$
Maximum output voltage	$V_{OM}$	-3.0		3.0	V	
Input capacitance	$C_{AIN}$			10	pF	
<b>Receive Power Amplifier</b>						
Output offset voltage	$V_{OA}$	-50		50	mV	Pin $A_{OUT}$ ; $D_R = +0$ code
Maximum output voltage	$V_{OM}$	-2.5		2.5	V	$R_L \geq 600\ \Omega$
Output resistance	$R_{ORR}$		1		$\Omega$	

**AC Characteristics**

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{DD} = +5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{SS} = -5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{DG} = V_{AG} = 0$ ;  
 $f_{CLKR} = f_{CLKX} = 2048\text{ kHz}$ ;  $R_L = 500\ \Omega$ ;  $C_L = 165\text{ pF}$ ;  $I_{OL} = 0.8\text{ mA}$ ;  $I_{OH} \leq 150\ \mu\text{A}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data enable time 1	$t_{DZX1}$			170	ns	Pin $D_X$ ; from $FS_X$ to $D_X$
Data enable time 2	$t_{DZX2}$			170	ns	Pin $D_X$ ; from $CLK_X$ to $D_X$
Data delay time	$t_{DDX}$			180	ns	Pin $D_X$
Data hold time	$t_{HZX}$		50		ns	Pin $D_X$

**Transmission Characteristics, μPD9601AD**

$T_A = +25^\circ\text{C}$ ;  $V_{DD} = +5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{SS} = -5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{DG} = V_{AG} = 0$   
 Analog input signal level  $V_{IN} = 0\text{ dBm0}$  ( $f = 820\text{ Hz}$ ); analog input gain =  $0\text{ dB}$ ; digital input signal level =  $0\text{ dBm0}$  ( $f = 820\text{ Hz}$ )

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
<b>Zero Transmission Level Point</b>						
Transmit	$0TLP_X$		+4.02		dBm	
Receive	$0TLP_R$		+4.02		dBm	

**Gain**

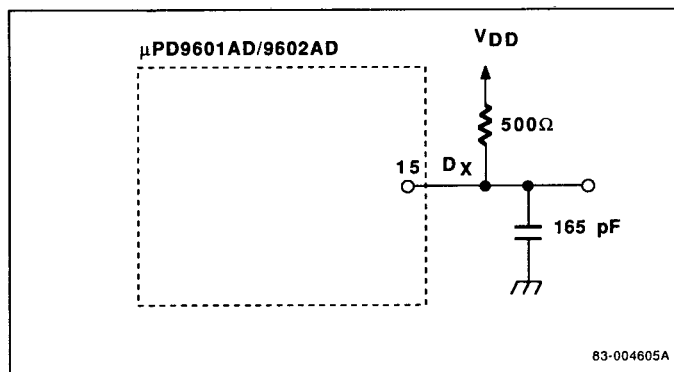
Transmit gain tolerance	$G_X$	-0.1		+0.1	dB	Referenced to $0TLP_X$ ; $V_{DD} = +5\text{ V}$ ; $V_{SS} = -5\text{ V}$
Receive gain tolerance	$G_R$	-0.1		+0.1	dB	Referenced to $0TLP_R$ ; $V_{DD} = +5\text{ V}$ ; $V_{SS} = -5\text{ V}$
$G_X$ variation with temperature and power supply	$\Delta G_X$	-0.2		+0.2	dB	$T_A = 0$ to $+70^\circ\text{C}$
$G_R$ variation with temperature and power supply	$\Delta G_R$	-0.2		+0.2	dB	

**Gain Tracking**

Variation of gain with input level

Transmit gain tracking CCITT G.714, Method 2	$GT_X$	-0.2		+0.2	dB	+3 to -40 dBm0
		-0.4		+0.4	dB	-40 to -50 dBm0
		-0.8		+0.8	dB	-50 to -55 dBm0
CCITT G.714, Method 1	$GT_X$		0.0		dB	-10 to -40 dBm0
				0.0	dB	-40 to -50 dBm0
				0.0	dB	-50 to -55 dBm0

**$D_X$  Output Measurement**



## Transmission Characteristics, μPD9601AD (cont)

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
<b>Gain Tracking (cont)</b>						
Receive gain tracking CCITT G.714, Method 2	G <sub>TR</sub>	-0.2		+0.2	dB	+3 to -40 dBm0
		-0.4		+0.4	dB	-40 to -50 dBm0
		-0.8		+0.8	dB	-50 to -55 dBm0
CCITT G.714, Method 1	G <sub>TR</sub>		0.0		dB	-10 to -40 dBm0
			0.0		dB	-40 to -50 dBm0
			0.0		dB	-50 to -55 dBm0
<b>Frequency Response</b>						
Gain relative to gain at 820 Hz						
Transmit section	G <sub>RX1</sub>			-24	dB	60 Hz
	G <sub>RX2</sub>	-2.0		0	dB	200 Hz
	G <sub>RX3</sub>	-0.15		+0.15	dB	0.3 to 3.0 kHz
	G <sub>RX4</sub>	-0.65		+0.15	dB	3.2 kHz
	G <sub>RX5</sub>	-0.8		0	dB	3.4 kHz
	G <sub>RX6</sub>			-6.5	dB	3.78 kHz
Receive section	G <sub>RR1</sub>	-0.15		+0.15	dB	0 to 3.0 kHz
	G <sub>RR2</sub>	-0.65		+0.15	dB	3.2 kHz
	G <sub>RR3</sub>	-0.8		0	dB	3.4 kHz
	G <sub>RR4</sub>			-6.5	dB	3.78 kHz
<b>Noise</b>						
Transmit section	N <sub>XP</sub>			-80	dBm0p	A <sub>IN+</sub> is grounded to AGND; input amplifier gain = 0 dB
Receive section	N <sub>RP</sub>			-80	dBm0p	D <sub>R</sub> = +0 code
Single-frequency noise	N <sub>SF</sub>			-50	dBm0	End-to-end testing; CCITT G.712 4.2
Crosstalk, transmit to receive	CT <sub>TR</sub>			-65	dB	A <sub>IN+</sub> = 0 dBm0, 820 Hz; D <sub>R</sub> = lowest positive decode level
Crosstalk, receive to transmit	CT <sub>RT</sub>			-65	dB	A <sub>IN+</sub> is grounded to AGND; D <sub>R</sub> = 0-dBm0, 820-Hz digital input
Power supply rejection						
f = 0.3 to 3 kHz	PSRR <sub>1</sub>	30			dB	±100-mV zero-to-peak signal on V <sub>DD</sub> or V <sub>SS</sub>
f = 3 to 4 kHz	PSRR <sub>2</sub>	30			dB	
f = 4 to 50 kHz	PSRR <sub>3</sub>	30			dB	

**Transmission Characteristics, μPD9601AD (cont)**

Parameter	Symbol	Limits			Unit	Test Conditions	
		Min	Typ	Max			
<b>Distortion</b>							
Transmit signal-to-distortion ratio CCITT G.714, Method 2	SD <sub>X</sub>	36			dB	0 to -30 dBm0	
		31			dB	-30 to -40 dBm0	
		26			dB	-40 to -45 dBm0	
	CCITT G.714, Method 1	SD <sub>X</sub>		37		dB	-6 to -27 dBm0
				35		dB	-27 to -34 dBm0
				30		dB	-34 to -40 dBm0
				15		dB	-40 to -55 dBm0
	Receive signal-to-distortion ratio CCITT G.714, Method 2	SD <sub>R</sub>	36			dB	0 to -30 dBm0
			31			dB	-30 to -40 dBm0
26					dB	-40 to -45 dBm0	
CCITT G.714, Method 1		SD <sub>R</sub>		37		dB	-6 to -27 dBm0
				35		dB	-27 to -34 dBm0
				30		dB	-34 to -40 dBm0
				15		dB	-40 to -55 dBm0
Intermodulation distortion, end-to-end CCITT G.712 (7.1)		IMD <sub>1</sub>			-38	dB	
					-52	dBm0	
Absolute delay, A <sub>IN</sub> to A <sub>OUT</sub>	D <sub>A</sub>			480	μs		
Group delay, A <sub>IN</sub> to A <sub>OUT</sub>	D <sub>0</sub>			1.40	ms	500 Hz	
				0.70	ms	600 Hz	
				0.20	ms	1000 Hz	
				0.20	ms	2600 Hz	
				1.40	ms	2800 Hz	



## Transmission Characteristics, μPD9602AD

$T_A = +25^\circ\text{C}$ ;  $V_{DD} = +5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{SS} = -5.0\text{ V} \pm 0.25\text{ V}$ ;  $V_{DG} = V_{AG} = 0$ ;

Analog input signal level  $V_{IN} = 0\text{ dBm0}$  ( $f = 1020\text{ Hz}$ ); analog input gain =  $0\text{ dB}$ ; digital input signal level =  $0\text{ dBm0}$  ( $f = 1020\text{ Hz}$ )

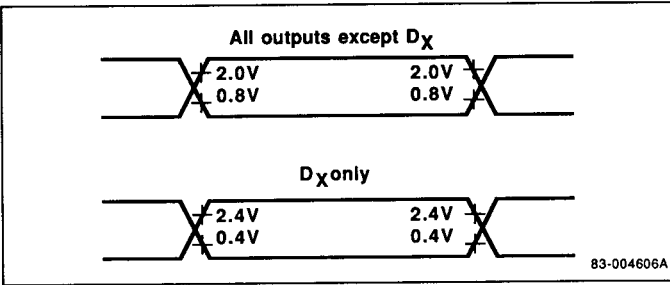
Parameter	Symbol	Limits			Unit	Test Conditions	
		Min	Typ	Max			
<b>Zero Transmission Level Point</b>							
Transmit	OTLP <sub>X</sub>		+3.99		dBm		
Receive	OTLP <sub>R</sub>		+3.99		dBm		
<b>Gain</b>							
Transmit gain tolerance	G <sub>X</sub>	-0.1		+0.1	dB	Referenced to OTLP <sub>X</sub> ; $V_{DD} = +5\text{ V}$ ; $V_{SS} = -5\text{ V}$	
Receive gain tolerance	G <sub>R</sub>	-0.1		+0.1	dB	Referenced to OTLP <sub>R</sub> ; $V_{DD} = +5\text{ V}$ ; $V_{SS} = -5\text{ V}$	
G <sub>X</sub> variation with temperature and power supply	ΔG <sub>X</sub>	-0.2		+0.2	dB	$T_A = 0\text{ to }+70^\circ\text{C}$	
G <sub>R</sub> variation with temperature and power supply	ΔG <sub>R</sub>	-0.2		+0.2	dB		
<b>Gain Tracking</b>							
Variation of gain with input level							
Transmit gain tracking	GT <sub>X</sub>		-0.2		+0.2	dB	+3 to -40 dBm0
			-0.4		+0.4	dB	-40 to -50 dBm0
			-0.8		+0.8	dB	-50 to -55 dBm0
Receive gain tracking	GT <sub>R</sub>		-0.2		+0.2	dB	+3 to -40 dBm0
			-0.4		+0.4	dB	-40 to -50 dBm0
			-0.8		+0.8	dB	-50 to -55 dBm0
<b>Frequency Response</b>							
Gain relative to gain at 1020 Hz							
Transmit section	G <sub>RX1</sub>				-24	dB	60 Hz
	G <sub>RX2</sub>		-2.0		0	dB	200 Hz
	G <sub>RX3</sub>		-0.15		+0.15	dB	0.3 to 3.0 kHz
	G <sub>RX4</sub>		-0.65		+0.15	dB	3.2 kHz
	G <sub>RX5</sub>		-0.8		0	dB	3.4 kHz
	G <sub>RX6</sub>					-6.5	dB
Receive section	G <sub>RR1</sub>		-0.15		+0.15	dB	0. to 3.0 kHz
	G <sub>RR2</sub>		-0.65		+0.15	dB	3.2 kHz
	G <sub>RR3</sub>		-0.8		0	dB	3.4 kHz
	G <sub>RR4</sub>					-6.5	dB

**Transmission Characteristics, μPD9602AD (cont)**

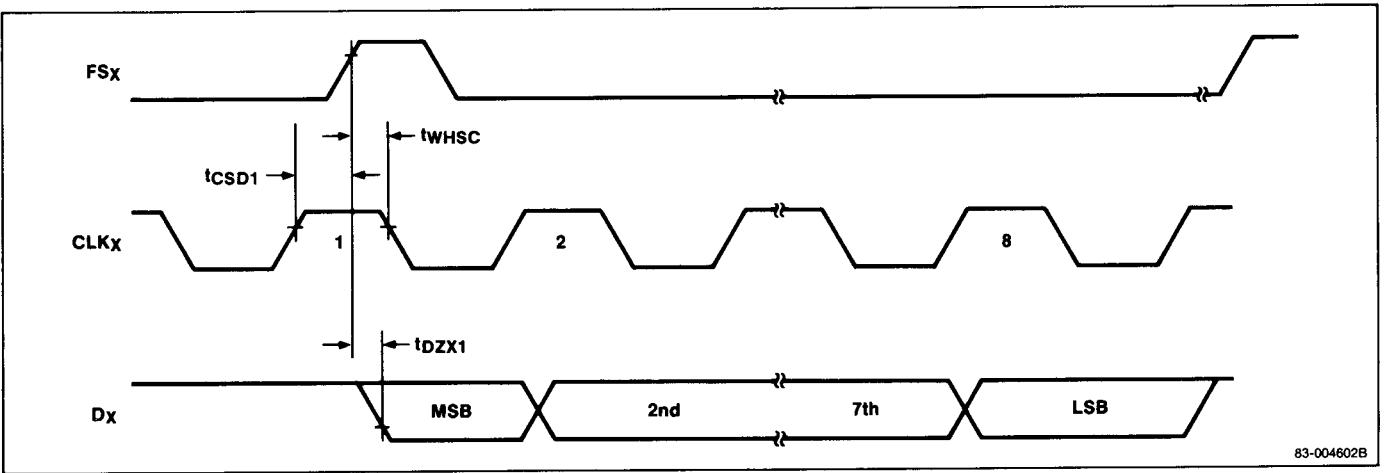
Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
<b>Noise</b>						
Transmit section	N <sub>XC</sub>			16	dBrnc0	A <sub>IN+</sub> is grounded to AGND; input amplifier gain = 0 dB
Receive section	N <sub>RC</sub>			10	dBrnc0	
Single-frequency noise	N <sub>SF</sub>			-50	dBm0	End-to-end testing; CCITT G.712 4.2
Crosstalk, transmit to receive	CT <sub>TR</sub>			-65	dB	A <sub>IN+</sub> = 0 dBm0, 1020 Hz; D <sub>R</sub> = lowest positive decode level
Crosstalk, receive to transmit	CT <sub>RT</sub>			-65	dB	A <sub>IN+</sub> is grounded to AGND; D <sub>R</sub> = 0-dBm0, 1020-Hz digital input
Power supply rejection						
f = 0.3 to 3 kHz	PSRR <sub>1</sub>	30			dB	±100-mV zero-to-peak signal on V <sub>DD</sub> or V <sub>SS</sub>
f = 3 to 4 kHz	PSRR <sub>2</sub>	20			dB	
f = 4 to 50 kHz	PSRR <sub>3</sub>	30			dB	
<b>Distortion</b>						
Transmit signal-to-distortion ratio, CCITT, G.714, Method 2	SD <sub>X</sub>	36			dB	0 to -30 dBm0
		31			dB	-30 to -40 dBm0
		26			dB	-40 to -45 dBm0
Receive signal-to-distortion ratio CCITT G.714, Method 2	SD <sub>R</sub>	36			dB	0 to -30 dBm0
		31			dB	-30 to -40 dBm0
		26			dB	-40 to -45 dBm0
Intermodulation distortion	IMD <sub>1</sub>			-38	dB	End-to-end measurement; CCITT G.712 (7.1)
				-52	dBm0	End-to-end measurement; CCITT G.712 (7.2)
Absolute delay, A <sub>IN</sub> to A <sub>OUT</sub>	D <sub>A</sub>			480	μs	
Group delay, A <sub>IN</sub> to A <sub>OUT</sub>	D <sub>0</sub>			1.40	ms	500 Hz
				0.70	ms	600 Hz
				0.20	ms	1000 Hz
				0.20	ms	2600 Hz
				1.40	ms	2800 Hz

## Timing Waveforms

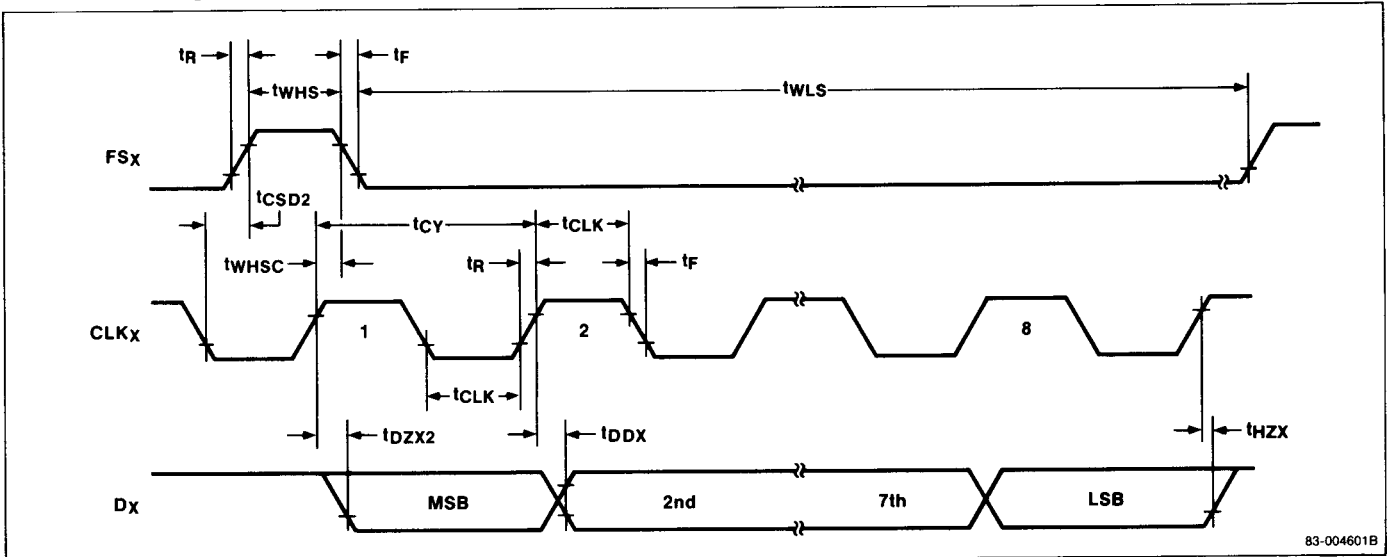
### Timing Measurement Points



### Transmit Timing 1

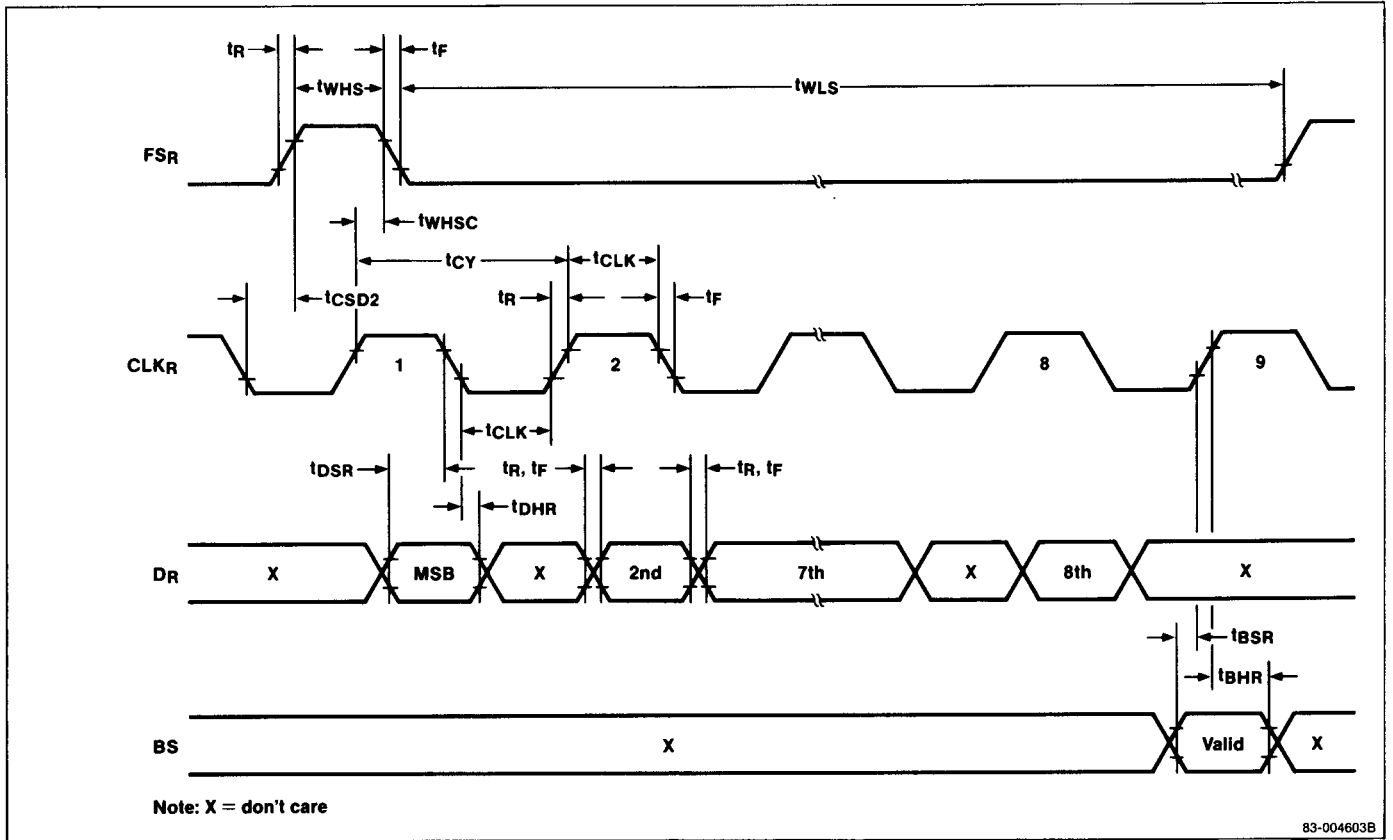


### Transmit Timing 2

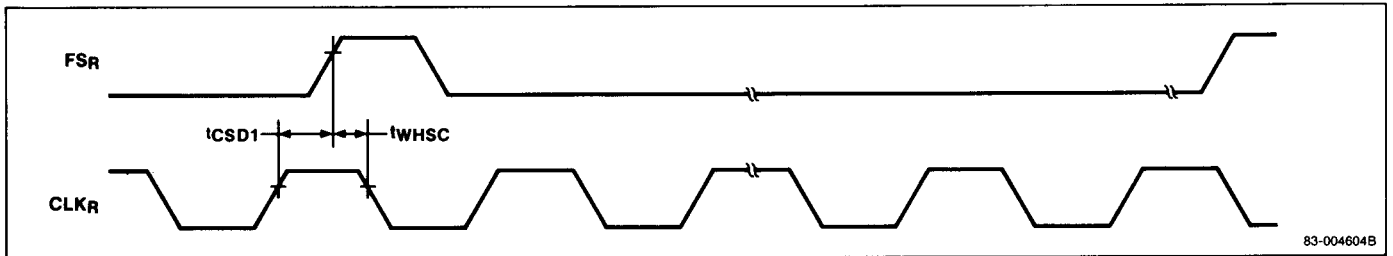


**Timing Waveforms (cont)**

**Receive Timing 1**



**Receive Timing 2**



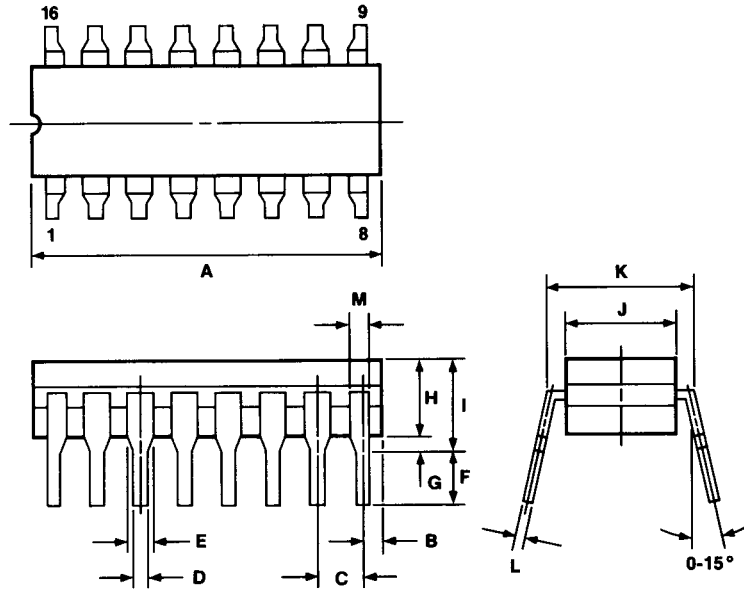
## Package Drawing

### 16-Pin Ceramic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.46 ±0.05	.018 ±.002
E	1.42 min	.056 min
F	3.5 ±0.3	.138 ±.012
G	0.51 min	.020 min
H	3.80	.150
I	5.08 max	.200 max
J	7.32	.288
K	7.62 [TP]	.300 [TP]
L	0.25 ±0.05	.010 ±.002
M	0.89 min	.035 min

**Notes:**

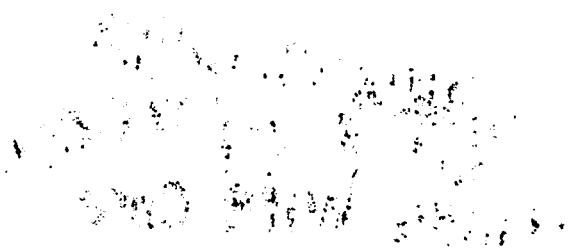
- [1] Each lead centerline is located within 0.25 mm [.01 inch] of its true position [TP] at maximum material condition.
- [2] Item "K" to center of leads when formed parallel.



83-004657B







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