

μ PD9903 ANALOG SUBSCRIBER LINE LSI (DIGITAL CODEC)

The μ PD9903 is a digital CODEC that can be used in analog subscriber circuits such as private branch exchangers (PBXs) and switching equipment for central offices. It features three of the functions required for analog subscriber circuits: 2W/4W conversion, CODEC supervision, and subscriber line supervision.

Use of the μ PD9903 in combination with a BS-SLIC (μ PC7073) can reduce the number of components required in analog subscriber circuits.

FEATURES

- Single-chip monolithic LSI (CMOS)
- PCM CODEC \rightarrow oversampling-type A/D and D/A converters
- Programmable functions
 - Termination impedance
 - Hybrid balance network
 - Feed resistance
 - Feed current
 - PAD control
 - A-law and μ -law
- Digital gain set function
- Ring-Trip function
- Single power supply (+5 V)
- Low power consumption during standby mode: 20 mW (TYP.)

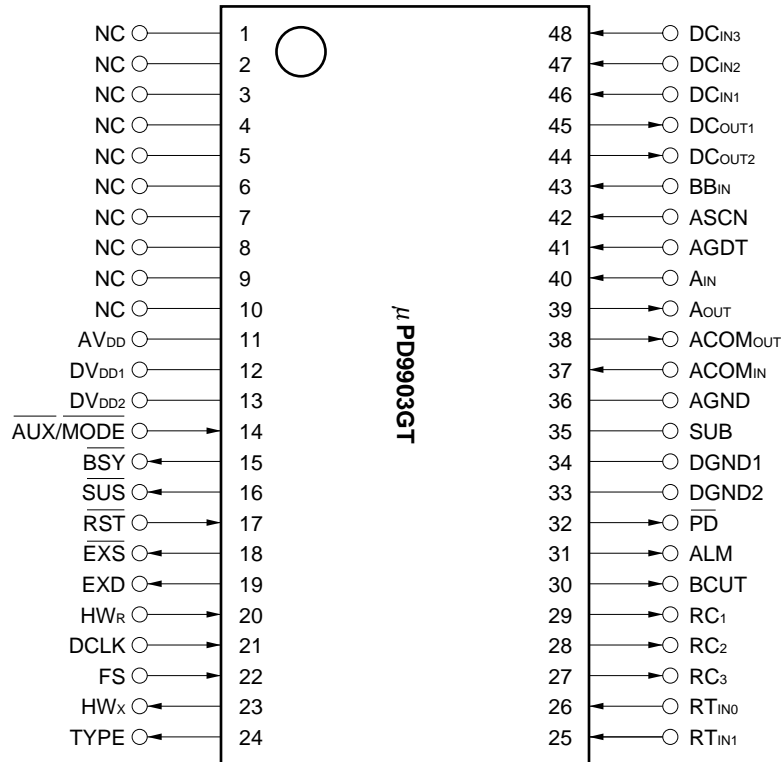
ORDERING INFORMATION

Part Number	Package
μ PD9903GT	48-pin plastic shrink SOP (375 mil)

The information in this document is subject to change without notice.

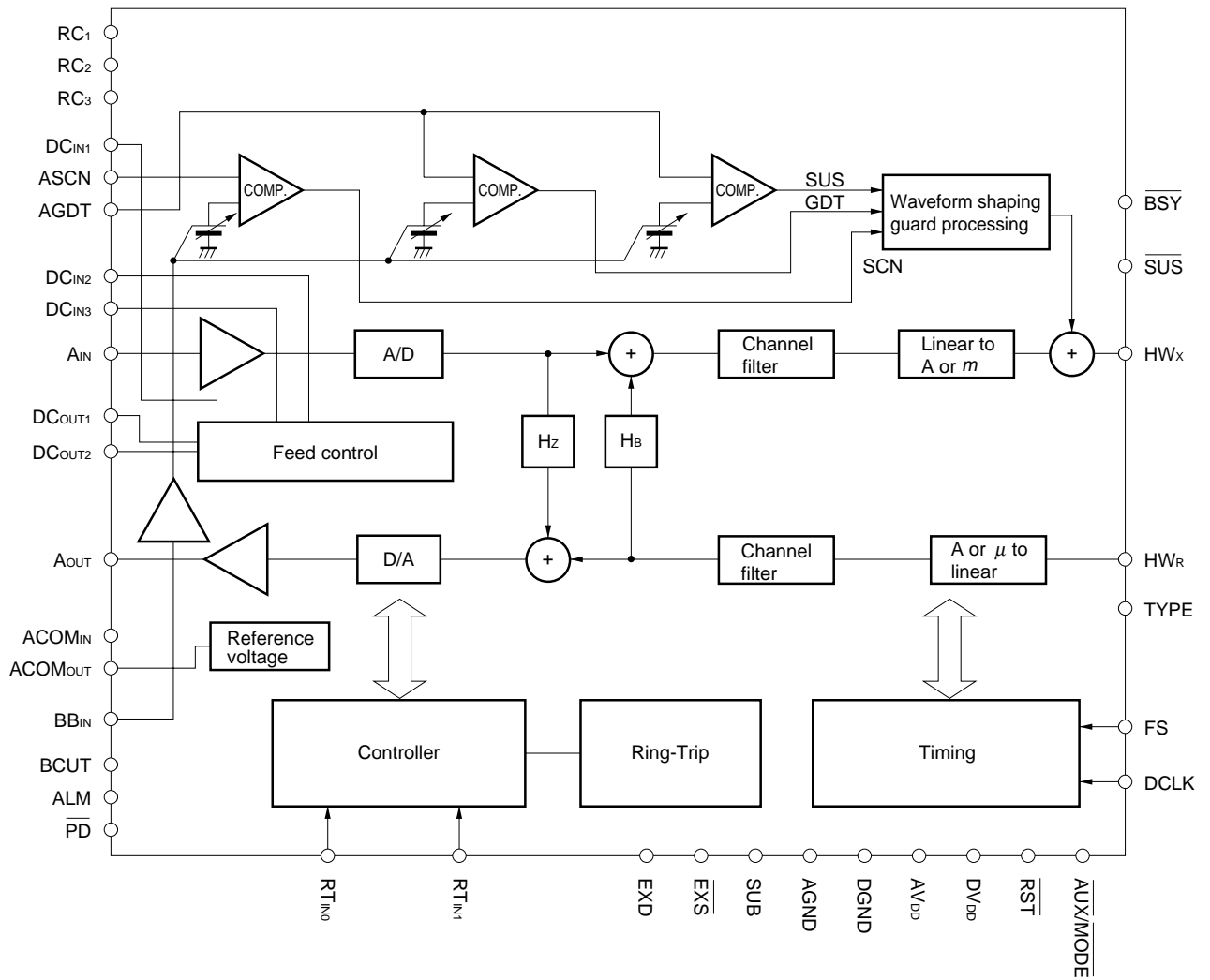
PIN CONFIGURATION (Top View)

48-pin plastic shrink SOP (375 mil)



- | | | | |
|---|--|---------------------------------------|----------------------------------|
| ACOM _{IN} | : ANALOG COMMON VOLTAGE IN | DGND1, DGND2 | : DIGITAL GROUND |
| ACOM _{OUT} | : ANALOG COMMON VOLTAGE OUT | DVDD1, DVDD2 | : DIGITAL POSITIVE POWER SUPPLY |
| AGDT | : ANALOG GROUND DETECTION SIGNAL IN | EXD | : EXPANSION PORT DATA |
| AGND | : ANALOG GROUND | EXS | : EXPANSION PORT SYNCHRONIZATION |
| A _{IN} | : ANALOG SIGNAL IN | FS | : FRAME SYNCHRONOUS CLOCK IN |
| ALM | : ALARM OUT | HW _R | : RECEIVE HIGHWAY DATA IN |
| A _{OUT} | : ANALOG SIGNAL OUT | HW _X | : TRANSMIT HIGHWAY DATA OUT |
| ASCN | : ANALOG LOOP DETECTION SIGNAL IN | NC | : NO CONNECTION |
| AUX/MODE | : EXTERNAL SIGNAL IN/MODE CONTROL SET | PD | : POWER DOWN CONTROL OUT |
| AV _{DD} | : ANALOG POSITIVE POWER SUPPLY | RC ₁ - RC ₃ | : RELAY CONTROL OUT |
| BB _{IN} | : V _{BB} VOLTAGE INFORMATION IN | RST | : RESET IN |
| BCUT | : BATTERY FEED CUT SIGNAL OUT | RT _{IN0} , RT _{IN1} | : RING TRIP SIGNAL IN |
| BSY | : BUSY SIGNAL OUT | SUB | : SUB GROUND |
| DC _{IN1} - DC _{IN3} | : DC FEEDBACK CONTROL IN | SUS | : SUSPEND SIGNAL OUT |
| DCLK | : DATA CLOCK IN | TYPE | : TYPE SIGNAL OUT |
| DC _{OUT1} , DC _{OUT2} | : DC FEEDBACK CONTROL OUT | | |

BLOCK DIAGRAM



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1. PIN FUNCTIONS

Number	Pin Name	I/O	Function
1-10	NC	–	Leave this pin open.
11	AV _{DD}	–	+5 V power supply (analog)
12	DV _{DD1}	–	+5 V power supply (digital)
13	DV _{DD2}	–	+5 V power supply (digital)
14	AUX/MODE	I	External signaling input
15	BSY	O	BUSY LED driver output
16	SUS	O	SUS LED driver output
17	RST	I	Pin for reset input and power-on reset H: HW _x valid, L: HW _x output's internal F/F clear status
18	EXS	O	SIPO sync signal output for expansion port Note 1
19	EXD	O	SIPO serial data output for expansion port Note 1
20	HW _R	I	Reception highway input [PCM data (8-bit) + CTL data (8-bit)]
21	DCLK	I	Clock input (2.048 MHz)
22	FS	I	8-kHz sync input Rising: HW _R PCM data input start Rising: HW _x PCM data output start Falling: HW _R CTL data input start Falling: HW _x SCN data output start
23	HW _x	O	Transmission highway output [PCM data (8-bit) + SCN data (8-bit)]
24	TYPE	O	HW _x data enable
25	RT _{IN1}	I	Ring-Trip signal input 2
26	RT _{IN0}	I	Ring-Trip signal input 1
27	RC ₃	O	Relay control for network testing [to the μ PC7073's pin 22]
28	RC ₂	O	Relay control for line testing [to the μ PC7073's pin 21]
29	RC ₁	O	Relay control for ringer transmit [to the μ PC7073's pin 20]
30	BCUT	O	High and wet control output [to the μ PC7073's pin 19]
31	ALM	O	Control output for ground-fault/power line contact protection mode [to the μ PC7073's pin 18]
32	PD	O	Power-down control output [to the μ PC7073's pin 17]
33	DGND2	–	Digital ground 2 Note 2
34	DGND1	–	Digital ground 1 Note 2
35	SUB	–	Substrate ground Note 2
36	AGND	–	Analog ground Note 2
37	ACOM _{IN}	I	Signal ground input Note 3 [to the μ PC7073's pin 11]
38	ACOM _{OUT}	O	Signal ground output Note 3 [to the μ PC7073's pin 11]
39	A _{OUT}	O	Analog signal output for receive side [to the μ PC7073's pin 10]
40	A _{IN}	I	Analog signal input for transmit side [to the μ PC7073's pin 9]
41	AGDT	I	Tip-Ring sum current detection input [to the μ PC7073's pin 8]
42	ASCN	I	Tip-Ring difference current detection input [to the μ PC7073's pin 7]
43	BB _{IN}	I	V _{BB} voltage information input [to the μ PC7073's pin 6]

Notes 1. SIPO: Serial In Parallel Out

2. Short AGND, DGND1, DGND2, and SUB directly under the IC and connect them to an analog ground.

3. Short ACOM_{IN} and ACOM_{OUT} directly under the IC.

Number	Pin Name	I/O	Function
44	DC _{OUT2}	O	DC feedback bias voltage output [to the μ PC7073's pin 5]
45	DC _{OUT1}	O	DC feedback control output [to the μ PC7073's pin 4]
46	DC _{IN1}	I	DC feedback control input 1 [to the μ PC7073's pin 3]
47	DC _{IN2}	I	DC feedback control input 2 [to the μ PC7073's pin 2]
48	DC _{IN3}	I	DC feedback control input 3 [to the μ PC7073's pin 1]

2. USE CAUTIONS

(1) Combined characteristics of the μ PC9903 and μ PD7073

- The μ PD9903 is designed to be used in combination with the μ PC7073. Therefore, the first half of the electrical specifications described below are ratings for the μ PD9903 as a discrete unit while the second half are combined ratings with the μ PC7073.
- Subscriber circuit constants that are determined by factors such as termination impedance are configured to enable setting by external order parameters. Consequently, input of an order that is not suitable for the target impedance may result in failure to obtain the required characteristics.

(2) Absolute maximum ratings

Application of voltage or current in excess of the absolute maximum ratings may result in damage. Be especially cautious about surges, etc.

(3) Load of by-pass capacitor

Because the μ PC7073 and μ PD9903 use several internal high-frequency operational amplifiers, high power supply impedance can cause instability in these internal operational amplifiers (such as oscillation). To suppress such instability and eliminate power supply noise, connect by-pass capacitors (C_{ACOM} = approximate 0.1 μ F) having superior high frequency characteristics as close as possible to the μ PC7073's power supply pins (V_{BB} and V_{CC}) and the μ PD9903's power supply pins (AV_{DD} and DV_{DD}).

(4) Addition of ACOM pin connection capacitor

The voltage of the ACOM pin between the μ PC7073 and μ PD9903 is the reference voltage of the signal source between the μ PC9903 and μ PC7073. Superposing of noise on this pin may have adverse effects on transmission characteristics. Therefore, make the wires between the ACOM pins of the two LSIs as short as possible, and connect capacitors (C_{ACOM} = approximate 0.1 μ F) having superior high frequency characteristics as close as possible to the pins.

3. ELECTRICAL SPECIFICATIONS

3.1 Discrete unit Ratings

Absolute maximum ratings (T_A = +25 °C)

Parameter	Symbol	Conditions	Rating	Units
Power supply voltage	V _{DD}	AV _{DD} , DV _{DD1} , DV _{DD2}	-0.3 to +7.0	V
Analog input voltage	V _{AIN}	A _{IN} , ASCN, AGDT, ACOM _{IN} , BB _{IN} , DC _{IN1} , DC _{IN2} , and DC _{IN3} pins	-0.3 to V _{DD} + 0.3	
Digital input voltage	V _{DIN}	HW _R , DCLK, FS, RST, $\overline{\text{AUX/MODE}}$, RT _{IN0} , and RT _{IN1} pins	-0.3 to V _{DD} + 0.3	
Applied voltage to analog output pin	V _{AOUT}	A _{OUT} , DC _{OUT1} , DC _{OUT2} , and ACOM _{OUT} pins	-0.3 to V _{DD} + 0.3	
Applied voltage to digital output pin	V _{DOUT}	HW _X , $\overline{\text{BSY}}$, $\overline{\text{SUS}}$, RC ₁ , RC ₂ , RC ₃ , $\overline{\text{EXS}}$, EXD, BCUT, ALM, $\overline{\text{PD}}$, and TYPE pins	-0.3 to V _{DD} + 0.3	
Power dissipation	P _T		500	mW
Ambient operating temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-65 to +150	

Caution If the absolute maximum rating for any of the above parameters is exceeded even momentarily, it may adversely affect the quality of this product. In other words, these absolute maximum ratings have been set to prevent physical damage to the product. Do not use the product in such a way as to exceed any of these ratings.

Recommended operating conditions (T_A = 0 to 70 °C, V_{DD} = 5 V ± 5 %, GND = 0 V)

(1) DC conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Ambient operating temperature	T _A		0	25	70	°C
Power supply voltage	V _{DD}		4.75	5.0	5.25	V
Analog input voltage	V _{AI}	ASCN, and AGDT pins	0		V _{DD}	
Analog input driving resistance	R _{LA1}	ASCN, and AGDT pins			20	kΩ
Analog output load resistance	R _{LOAD}	A _{OUT} pin	100			pF
Analog output load capacitance	C _{LOAD}				100	
Low level input voltage	V _{IL1}	FS, DCLK, HW _R , and $\overline{\text{AUX/MODE}}$ pins	0		0.8	V
	V _{IL2}	$\overline{\text{RST}}$, RT _{IN0} , and RT _{IN1} pins	0		0.2 × V _{DD}	
High level input voltage	V _{IH1}	FS, DCLK, HW _R , and $\overline{\text{AUX/MODE}}$ pins	2.0		V _{DD}	
	V _{IH2}	$\overline{\text{RST}}$, RT _{IN0} , and RT _{IN1} pins	0.8 × V _{DD}		V _{DD}	

(2) AC conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Data clock frequency	f _{DCLK}	(= 1/t _{cy}) ± 50 ppm		2048		kHz
Data clock pulse width	t _{DCLK}		200			ns
Frame sync clock frequency	f _s	± 50 ppm		8.0		kHz
High level frame sync pulse width	t _{WHS}		t _{cy} × 8			ns
Low level frame sync pulse width	t _{WLS}		t _{cy} × 8			ns
Clock rise time	t _R				30	ns
Clock fall time	t _F				30	ns
Float in sync timing	t _{CSD1}				100	ns
	t _{CSD2}		40			ns
High level width of frame sync clock and data clock	t _{WHSC}		100			ns
HW _R set-up time	t _{DSR}	Note 1	65			ns
HW _R hold time	t _{DHR}	Note 1	120			ns
Minimum width of reset pulse	PW _{RST}	$\overline{\text{RST}}$ pin Note 2	10			μs

- Notes**
1. During timing measurement, use 5 ns as the rise time and fall time for the digital input wave form and clock signal.
 2. The μPD9903 is initialized when high level input is applied to the $\overline{\text{RST}}$ pin after applying low level input for several clock widths. (However, use of the $\overline{\text{RST}}$ pin is not guaranteed during low level input. Also, low level input alone does not initialize the μPD9903.)

DC Characteristics ($T_A = 0$ to 70 °C, $V_{DD} = 5\text{ V} \pm 0.25\text{ V}$, $V_{DG} = V_{AG} = 0\text{ V}$, $f_{DCLK} = 2048\text{ kHz}$, all output pins are unloaded)

(1) Current consumption

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Circuit current	I_{DD}	During normal mode		15	21	mA
Power-down circuit current	I_{DDPD}	During power-down mode		46	6	

(2) Digital interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Digital input current	I_{ID}	$0 \leq V_{DIN} \leq V_{DD}$ for FS, DCLK, HW _R , RT _{IN0} , RT _{IN1} , and $\overline{\text{RST}}$ pins	-10		+10	μ A
Digital input pull-up current	I_{IL}	$V_{DIN} = 0\text{ V}$ for $\overline{\text{AUX/MODE}}$ pin	-50	-7	-0.5	
3-state leakage current	I_L	$0 \leq V_{DIN} \leq V_{DD}$ for HW _x pin	-10		+10	
Low level output voltage	V_{OL1}	$I_{OL} = 3.4\text{ mA}$ for HW _x pin			0.4	V
	V_{OL2}	$I_{OL} = 0.2\text{ mA}$ for RC ₁ , RC ₂ , RC ₃ , BCUT, ALM, $\overline{\text{PD}}$, $\overline{\text{EXS}}$, and EXD pins			0.4	
	V_{OL3}	$I_{OL} = 5\text{ mA}$ for $\overline{\text{BSY}}$ and $\overline{\text{SUS}}$ pins			1.1	
High level output voltage	V_{OH1}	$I_{OH} = -0.6\text{ mA}$ for HW _x and TYPE pins	2.4			
	V_{OH2}	$I_{OH} = -2.0\text{ mA}$ for RC ₁ , RC ₂ , RC ₃ , BCUT, ALM, $\overline{\text{PD}}$, $\overline{\text{EXS}}$, and EXD pins	2.4			
	V_{OH3}	$I_{OH} = 0\text{ mA}$ for $\overline{\text{BSY}}$ and $\overline{\text{SUS}}$ pins	$V_{DD} - 0.5$			
Output capacitance of digital output pin	C_{OD}	$f = 1\text{ MHz}$, unmeasured pins returned to 0 V			15	pF
Input capacitance of digital input pin	C_{ID}	$f = 1\text{ MHz}$, unmeasured pins returned to 0 V			10	

(3) A_{IN} pin

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input bias current	I_B	Input voltage:	-10		+10	μ A
Input resistance	R_{IN}		1			M Ω
Input capacitance	C_{IN}				10	pF

(4) A_{OUT} pin

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output offset voltage	V_{OA}	HW _R PCM data: zero PCM code, referenced to V_{ACOM}	-100		+100	mV
Output resistance	R_{OUT}	I/O current: -100 to +100 μ A			50	Ω

(5) ASCN and AGDT output pins

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input bias current	I_B	Input voltage: 0 to V_{DD}	-10		+10	μA
Input resistance	R_{IN}		1			$M\Omega$

(6) ACOM_{OUT} pin

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output voltage	V_{ACOM}	I/O current: -0.1 to +0.1 mA	2380		2420	mV

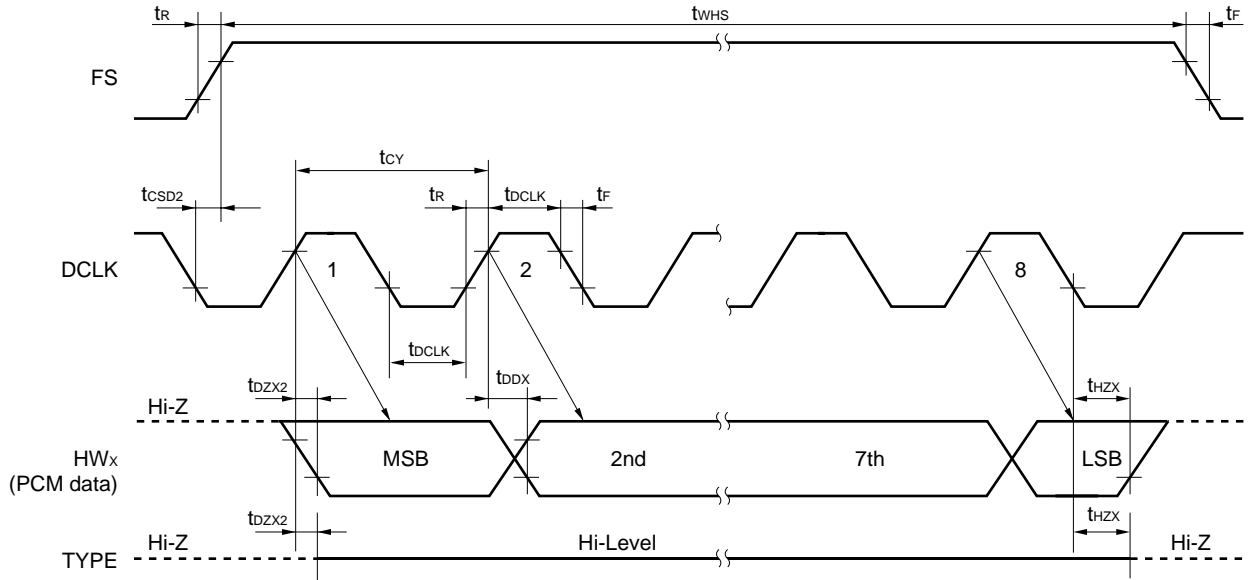
AC characteristics ($T_A = 0$ to 70 °C, $V_{DD} = 5\text{ V} \pm 0.25\text{ V}$, $V_{DG} = V_{AG} = 0$, $f_{DCLK} = 2048\text{ kHz}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Data enable delay time	t_{DZX1}	HW _x and TYPE pins, when FS is delayed longer than DCLK			170	ns
	t_{DZX2}	HW _x and TYPE pins, when DCLK is delayed longer than FS			170	ns
Data delay time	t_{DDX}	HW _x pin			180	ns
Data hold time	t_{HZX}	HW _x and TYPE pins	30		200	ns
Delay time to $\overline{\text{EXS}}$ falling edge	t_{DEXSf}	$\overline{\text{EXS}}$ pin			120	ns
Delay time to $\overline{\text{EXS}}$ rising edge	t_{DEXSr}	$\overline{\text{EXS}}$ pin			120	ns
EXD data delay time	t_{DEXD}	EXD pin			120	ns
Signaling bit set-up delay time	t_{DSIG}				2	μs
Status bit set-up delay time	t_{DST}				2	μs
LED driver set-up delay time	t_{DLED}	$\overline{\text{BSY}}$ and $\overline{\text{SUS}}$ pins			2	μs
Delay time to rising edge	t_{THL}				100	ns
Delay time to falling edge	t_{TLH}				100	ns
Transmit delay time to external bit	t_{DAUX}	$\overline{\text{AUX}}$ pin			125	μs

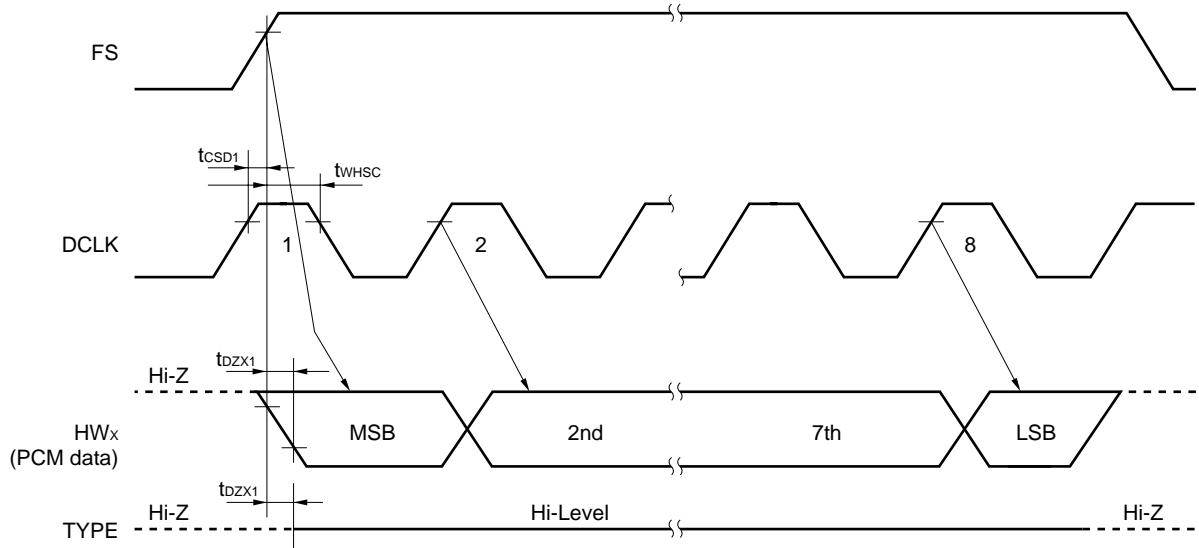
Timing charts

(1) PCM data transmission timing (HW_x pin)

(a) DCLK is later than FS

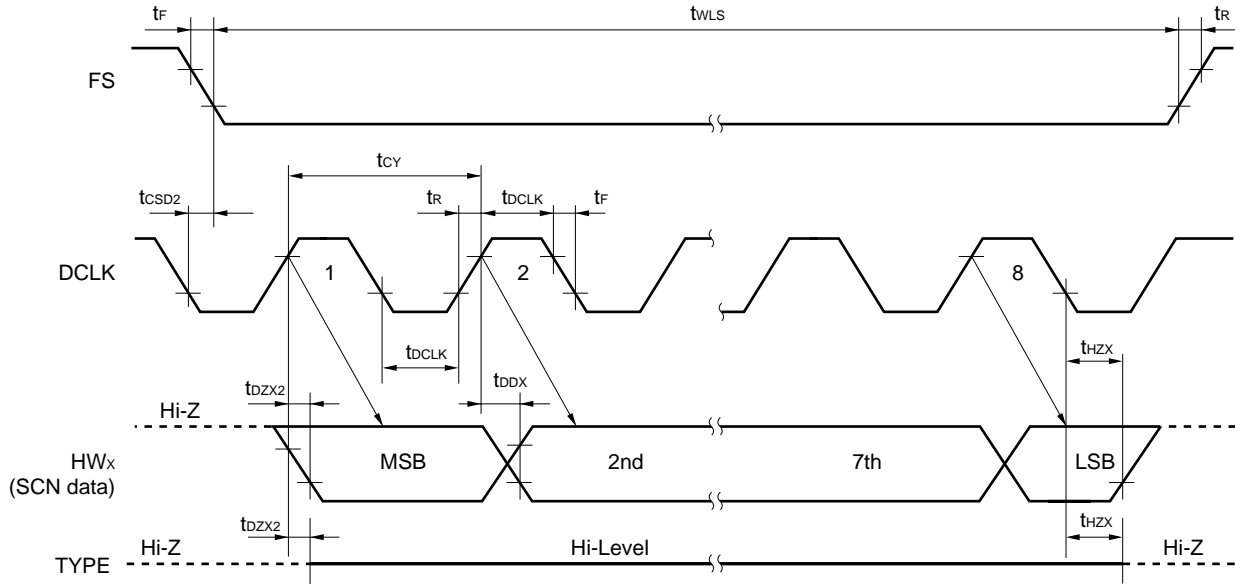


(b) FS is later than DCLK

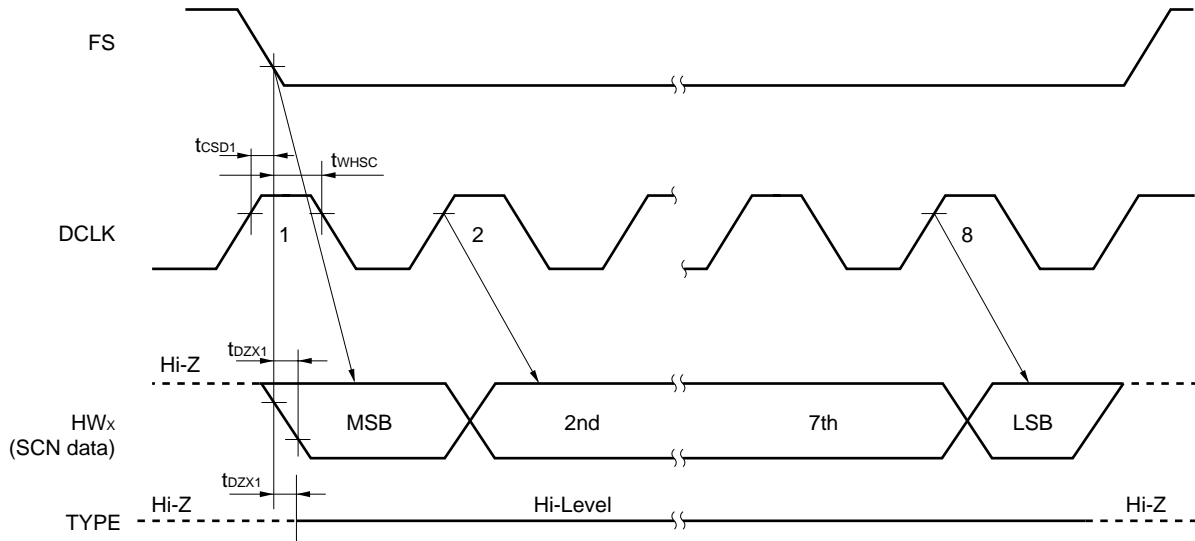


(2) SCN data transmission timing (HW_x pin)

(a) DCLK is later than FS

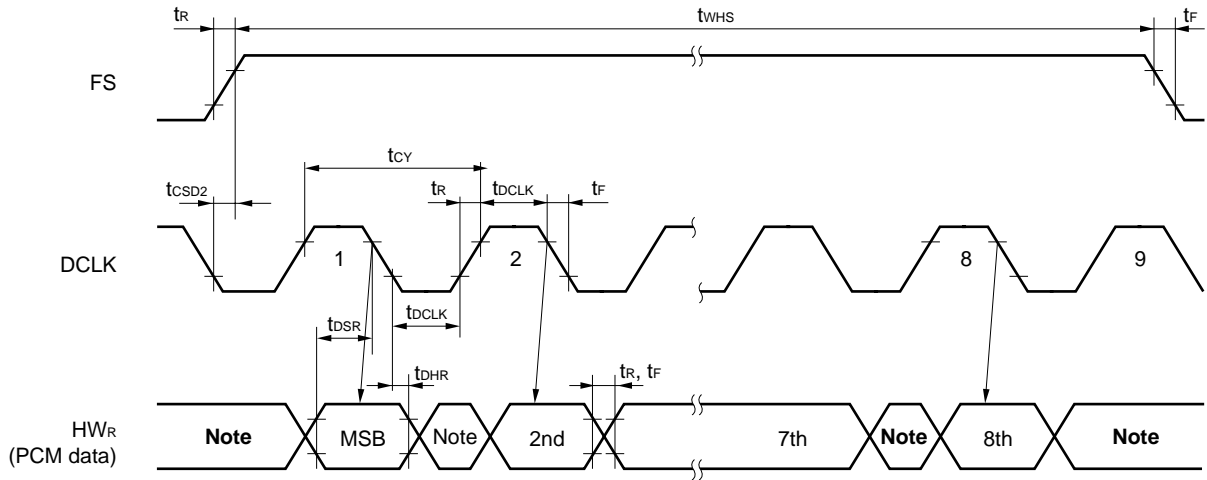


(b) FS is later than DCLK



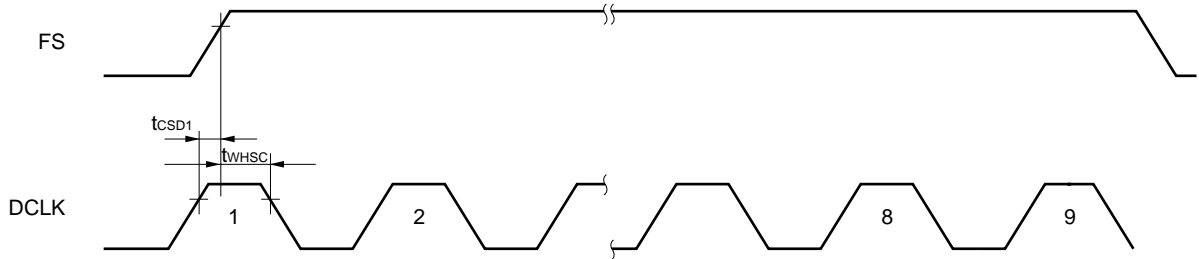
(3) PCM data reception timing (HW_R pin)

(a) DCLK is later than FS



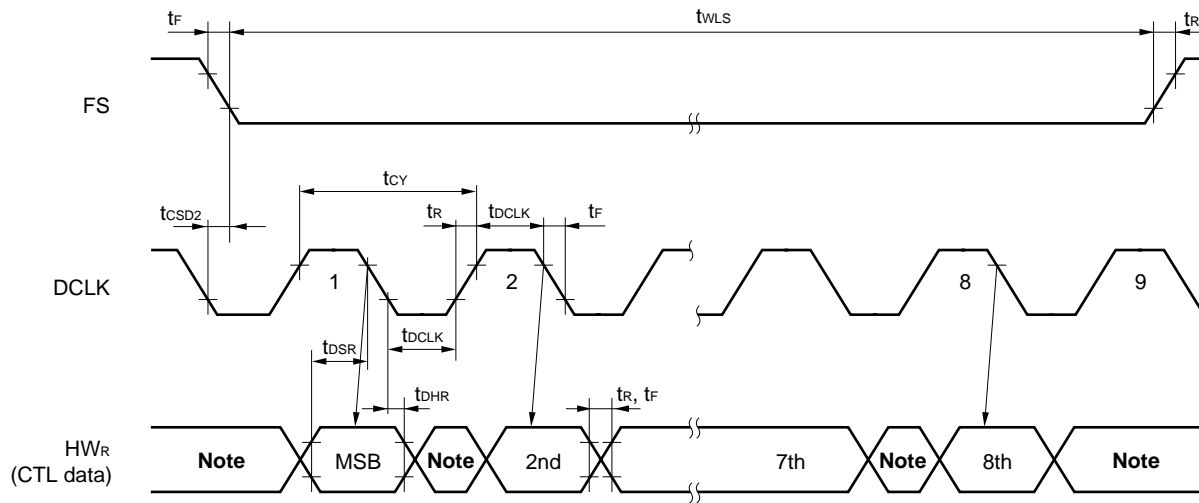
Note Don't care

(b) FS is later than DCLK



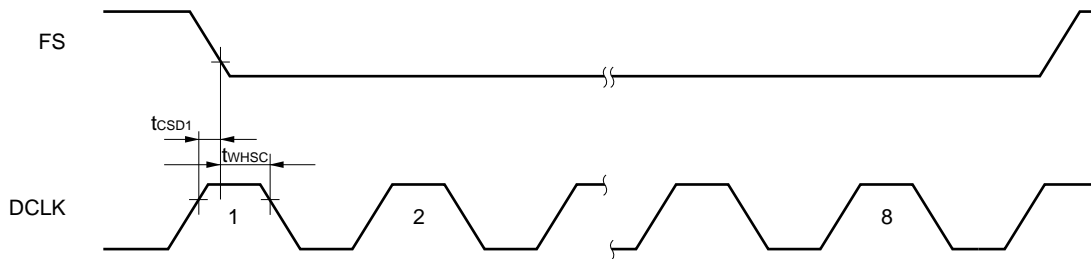
(4) CTL data reception timing (HW_R pin)

(a) DCLK is later than FS



Note Don't care

(b) FS is later than DCLK



3.2 Combined Specifications with the μPC7073

DC characteristics

μPC7073 ($V_{BB} = -42$ to -58 V, $V_{CC} = 5$ V \pm 0.25 V, $T_A = 0$ to 70 °C, $18 \leq I_L \leq I_{LMAX}$ (mA))

μPD9903 ($T_A = 0$ to 70 °C, $V_{DD} = 5$ V \pm 0.25 V, $V_{DG} = V_{AG} = 0$ V, $f_{DCLK} = 2048$ kHz)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Units
DC feed resistance	R _{BF}	200 Ω feed		180	200	220	Ω
		400 Ω feed		360	400	440	
Minimum loop current	I _{LMIN}	V _{BB} = -51 V R _L = 1900 Ω	200 Ω feed	21.7	22.2	22.6	mA
			400 Ω feed	18.2	18.8	19.3	
Maximum current setting value	I _{LMAX}	I _{LMAX} = 76 mA setting	200 Ω feed	70	76	82	mA
			400 Ω feed	50	55	60	
		I _{LMAX} = 45 mA setting	40	45	50		
Pin voltage during on-hook	V _{TS}	Normal on-hook, between Tip and GND, V _{BB} = -48 V		2.25	2.55	2.85	V
	V _{RS}	Normal on-hook, between Ring and V _{BB} , V _{BB} = -48 V		3.05	3.35	3.65	
	V _{TS}	On-hook transmission, between Tip and GND, V _{BB} = -48 V		2.25	2.55	2.85	
	V _{RS}	On-hook transmission, between Ring and V _{BB} , V _{BB} = -48 V		3.05	3.35	3.65	
Voltage between lines during on-hook	V _{TS}	V _{BB} = -48 V		V _{BB} - 7.0	V _{BB} - 5.9	V _{BB} - 5.0	V
Supervisory control - V _{BB} abnormal voltage	V _{BBF}			32	35	38	V

Parameter ^{Note}	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Loop detection operating resistance (during normal transmission)	R _{ON1}	Includes termination resistance	200 Ω feed		2500	Ω
			400 Ω feed		2100	
Loop detection non-operating resistance (during normal transmission)			200 Ω feed	3900		
			400 Ω feed	3500		
Loop detection operating resistance (during on hook transmission)	R _{ON2}	Includes termination resistance	200 Ω feed		1900	Ω
			400 Ω feed		1500	
Loop detection non-operating resistance (during on hook transmission)			200 Ω feed	2840		
			400 Ω feed	2440		
Loop release non-operating resistance	R _{ON3}	Includes termination resistance	200 Ω feed		2960	Ω
			400 Ω feed		2560	
Loop release operating resistance			200 Ω feed	4540		
			400 Ω feed	4140		
Ground detection 1 (C/O) operating resistance	R _{ON4}	Includes termination resistance			5.2	kΩ
Ground detection 1 (C/O) non-operating resistance				20		
Ground-fault/power line contact detection operating resistance	R _{ON6}	Includes termination resistance Off-hook state	I _{LMAX} = 45/76 mA		340	Ω
			I _{LMAX} = 35 mA		480	
Ground-fault/power line contact detection non-operating resistance		Includes termination resistance	I _{LMAX} = 45/76 mA	870		Ω
			I _{LMAX} = 35 mA	1130		
Ground-fault/power line contact release non-operating resistance	R _{ON7}	Includes termination resistance			1.4	kΩ
Ground-fault/power line contact release operating resistance				10		

Note The above values are resistance-converted values.

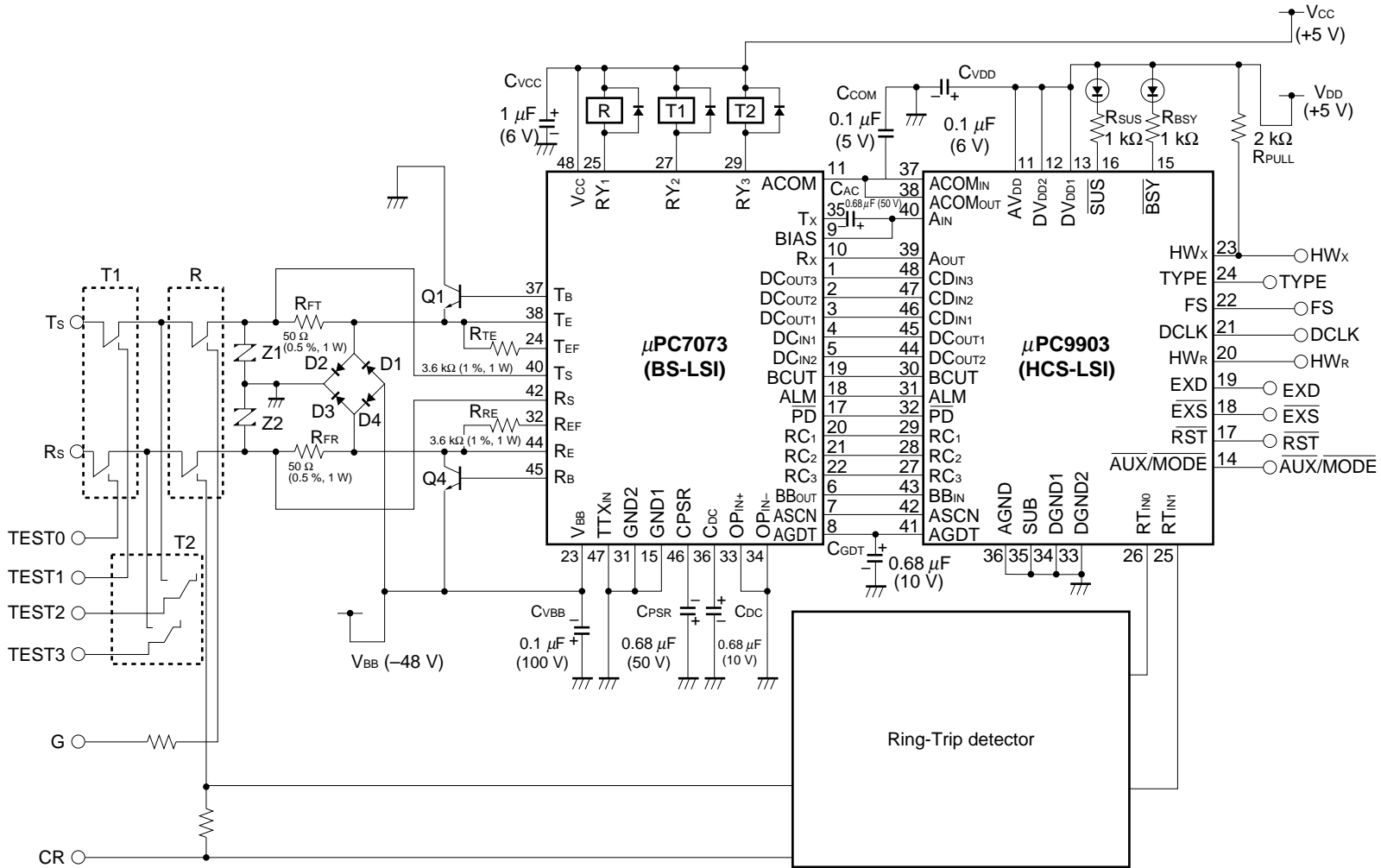
Transmission characteristics

μPC7073 ($V_{BB} = -42$ to -58 V, $V_{CC} = 5$ V \pm 0.25 V, $T_A = 0$ to 70 °C, $18 \leq I_L \leq I_{LMAX}$ (mA))

μPD9903 ($T_A = 0$ to 70 °C, $V_{DD} = 5$ V \pm 0.25 V, $V_{DG} = V_{AG} = 0$ V, $f_{DCLK} = 2048$ kHz)

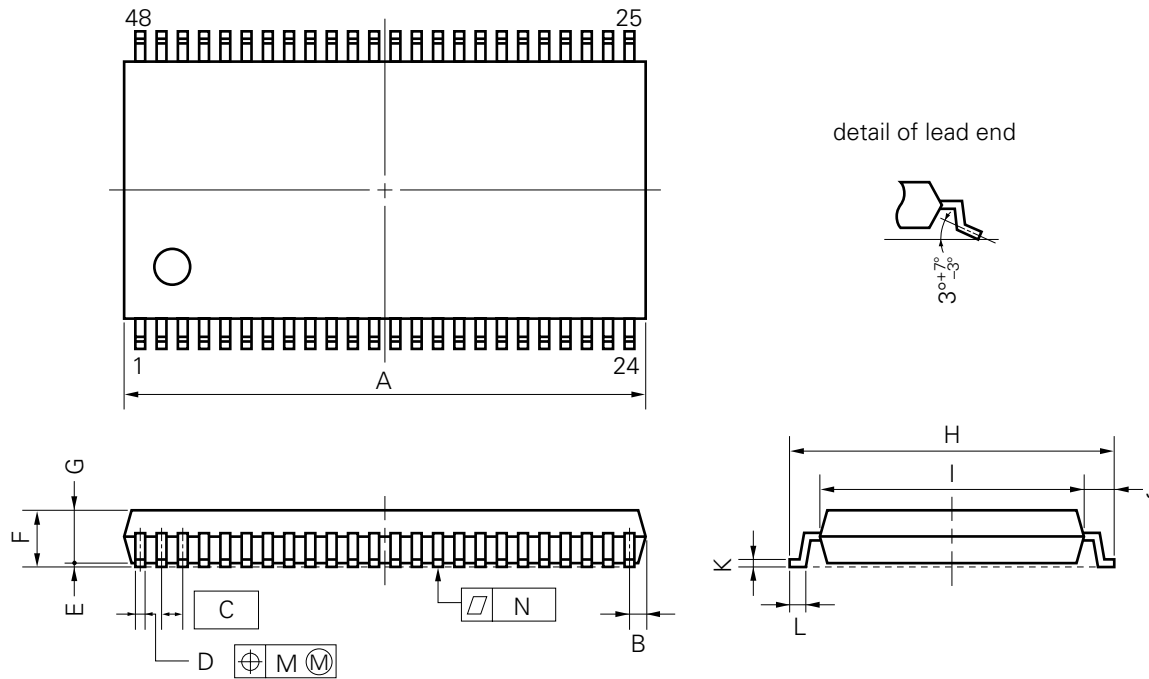
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Insertion loss	IL	A-D input signal 0 dBm0 1 kHz	-0.45	0.0	+0.45	dB
		D-A input signal 0 dBm0 1 kHz	-0.45	0.0	+0.45	
Transfer loss frequency characteristics	F _{RX}	A-D 60 Hz	24.0		-	dB
		Reference input signal 200 Hz	0.6		2.0	
		1015 Hz 0 dBm0 300 Hz	-0.15		+0.21	
		400 to 3000 Hz	-0.15		+0.15	
		3200 Hz	-0.15		+0.65	
	3400 Hz	0.2		0.8		
	F _{RR}	D-A 60 Hz	0.2		4.0	
		Reference input signal 200 Hz	0.1		1.0	
		1015 Hz 0 dBm0 300 Hz	-0.15		+0.25	
		400 to 3000 Hz	-0.15		+0.15	
3200 Hz		-0.15		+0.65		
3400 Hz	0.2		0.8			
Gain tracking (tone method)	GT _X	A-D +3 to -40 dBm0	-0.2		+0.2	dB
		Reference input signal -50 dBm0	-0.5		+0.5	
	-10 dBm0 -55 dBm0	-1.0		+1.0		
	f = 700 to 1100 Hz					
GT _R	D-A +3 to -40 dBm0	-0.2		+0.2		
	Reference input signal -50 dBm0	-0.4		+0.4		
		-10 dBm0 -55 dBm0	-0.8		+0.8	
		f = 700 to 1100 Hz				
Return loss	RL	Input signal 300 Hz	16			dB
		0 dBm0 500 to 2000 Hz	20			
		Z _T = 600 Ω + 2.16 μF 2000 to 3400 Hz	16			
Echo attenuation	TBRL	Input signal 300 Hz	18			dB
		0 dBm0 500 to 2500 Hz	22			
		Z _T = 600 Ω + 2.16 μF 3400 Hz	18			
Transmit channel total power distortion factor (tone method)	SD _X	A-D +3 to -30 dBm0	36			dB
		Input signal -40 dBm0	30			
		f = 700 to 1100 Hz -45 dBm0	25			
	SD _R	D-A +3 to -30 dBm0	36			
		Input signal -40 dBm0	30			
		f = 700 to 1100 Hz -45 dBm0	25			

4. SYSTEM APPLICATION EXAMPLE USING THE μPC7073 AND μPD9903



5. PACKAGE DRAWING

48 PIN PLASTIC SHRINK SOP (375 mil)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

P48GT-65-375B-1

ITEM	MILLIMETERS	INCHES
A	16.21 MAX.	0.639 MAX.
B	0.63 MAX.	0.025 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	0.012 ^{+0.004} _{-0.005}
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	10.0±0.3	0.394 ^{+0.012} _{-0.013}
I	8.0±0.2	0.315±0.008
J	1.0±0.2	0.039 ^{+0.009} _{-0.008}
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.10	0.004
N	0.10	0.004

6. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

μPC9903GT: 48-pin plastic shrink SOP (375 mil)

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Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared ray reflow	Package peak temperature: 235 °C Reflow time: 30 sec. max. (210 °C or above) Number of times: 1 time	IR35-00-1
Partial heating method	Pin temperature: 300 °C max. Heat time: 3 sec. max. (per each side of the device)	—

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.