



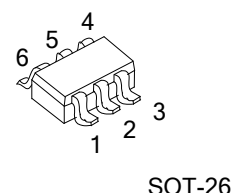
HIGH PRECISION CC/CV PRIMARY-SIDE PWM CONTROLLER

DESCRIPTION

The UTC **UPSR107** is a primary controller mode charger and adapter applications. The controlled variable is transferred by an auxiliary winding from the secondary to the primary side. The device integrates PWM controller to enhance the performance of Quasi Resonant (QR) mode flyback converters.

The UTC **UPSR107** operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. It also provides off-time modulation to linearly decrease PWM frequency under light-load conditions so that low standby power can be achieved.

The UTC **UPSR107** integrates functions and protections of Under Voltage Lockout (UVLO), V_{DD} Over Voltage Protection (V_{DD} OVP), Output Over Voltage Protection (Output OVP), OTP, Soft Start, Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, Gate Clamping, V_{DD} Clamping.



FEATURES

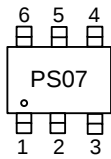
- * $\pm 5\%$ CC and CV Precision
- * Easily Meet EPS Level 6
- * QR Mode Control for High Efficiency and Low EMI
- * Programmable CV and CC Regulation
- * Less than 70mW Standby Power
- * Programmable Cable drop Compensation
- * Pin Floating Protection
- * Built-in Soft Start
- * Output Over Voltage Protection
- * Cycle-by-Cycle Current Limiting
- * Built-in Leading Edge Blanking (LEB)
- * V_{DD} Under Voltage Lockout with Hysteresis (UVLO)
- * V_{DD} OVP
- * V_{DD} Clamp

ORDERING INFORMATION

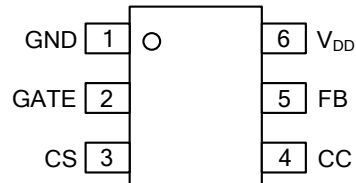
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UPSR107L-AG6-R	UPSR107G-AG6-R	SOT-26	Tape Reel

UPSR107G-AG6-R	
(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) AG6: SOT-26
(3) Green Package	(3) G : Halogen Free and Lead Free, L: Lead Free

MARKING



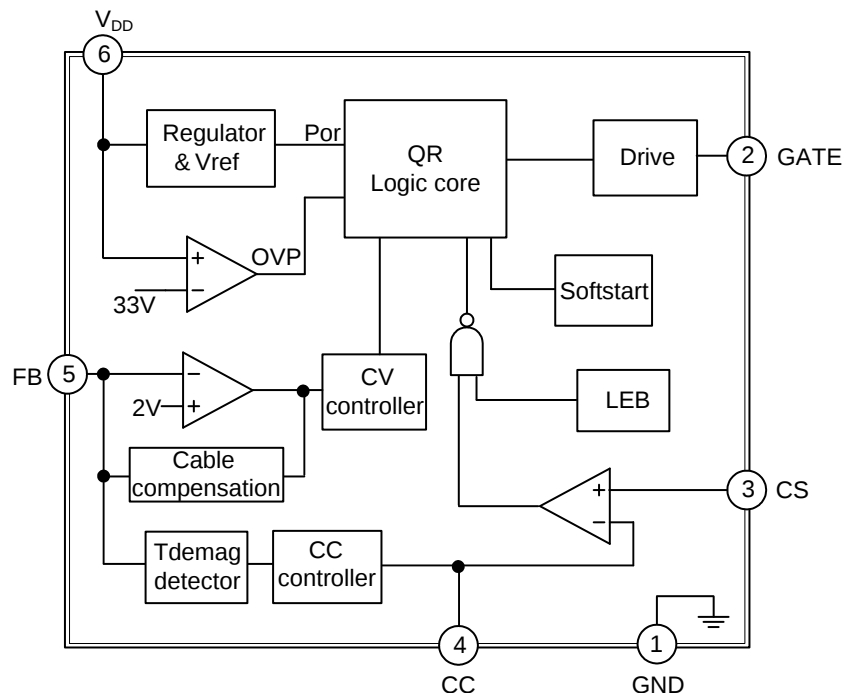
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground
2	GATE	Totem-pole gate drive output for power MOSFET.
3	CS	Current sense input. Connected to MOSFET current sensing resistor node.
4	CC	Connect a capacitor between this pin and GND for CC regulation.
5	FB	System feedback pin. This control input regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding.
6	V _{DD}	Power Supply

BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATING**

PARAMETER	SYMBOL	RATINGS	UNIT
V _{DD} DC Supply Voltage	V _{DD}	35	V
V _{DD} DC Clamp Current		10	mA
GATE Pin		20	V
CC, CS Voltage Range		-0.3 ~ 7	V
FB Voltage Range	V _{FB}	-0.7 ~ 7	V
Package Thermal Resistance		250	°C/W
Max Junction Temperature	T _J	+150	°C
Operating Temperature Range	T _{OPR}	-40 ~ +85	°C
Min/Max Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATION CONDITIONS**

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	10 ~ 30	V
Operating Ambient Temperature		-40 ~ +85	°C
Maximum Switching Frequency		120K	Hz

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$, $V_{DD}=16\text{V}$, if not otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD}) Section						
V_{DD} Start up Current	I_{DD_ST}	$V_{DD}=UVLO(ON)-1\text{V}$, Measure Current into V_{DD}		2	20	μA
Operation Current	I_{DD_OP}	$V_{FB}=1\text{V}$, $C_L=0.5\text{nF}$, $V_{DD}=20\text{V}$		1	1.5	mA
V_{DD} Under Voltage Lockout Enter	UVLO(ON)	V_{DD} falling	8.5	9.5	10.5	V
V_{DD} Under Voltage Lockout Exit	UVLO(OFF)	V_{DD} rising	14.0	15.5	16.5	V
Maximum V_{DD} Operation Voltage	V_{DD_CLAMP}	$I_{DD}=7\text{mA}$	33	35	37	V
Over Voltage Protection Threshold	V_{DD_OVP}		31	33	35	V
Current Sense Input Section (CS Pin)						
CS Input Leading Edge Blanking Time	T_{LEB}			500		ns
Over Current Detection and Control Delay	T_{D_OC}			100		ns
Feedback Input Section (FB Pin)						
Internal Error Amplifier (EA) Reference Input	V_{FB}		1.98	2.0	2.02	V
Output Over Voltage Protection Threshold	V_{FB_OVP}			2.4		V
Output Short Circuit Threshold	V_{FB_Short}			0.65		V
Output Short Circuit Frequency Clamp	F_{clamp_Short}			40		KHz
Demagnetization Comparator Threshold	V_{FB_DEM}			75		mV
Minimum OFF Time	T_{min_OFF}			2		μS
Maximum OFF Time	T_{max_OFF}			3		mS
Max Cable Compensation Current	I_{Cable_MAX}			40		μA
Constant Current Section (CC Pin)						
Internal CC Reference	V_{CC_ref}		490	500	510	mV
Gate Drive Output						
Output Low Level	V_{OL}	$I_O=20\text{mA}$ (Sink)			1	V
Output High Level	V_{OH}	$I_O=20\text{mA}$ (Source)	7.5			V
Output Clamp Voltage Level	V_{CLAMP}	$V_{DD}=24\text{V}$		16		V
Output Rising Time	T_r	$C_L=0.5\text{nF}$		700		ns
Output Falling Time	T_f	$C_L=0.5\text{nF}$		35		ns

■ OPERATION DESCRIPTION

The UTC **UPSR107** is a primary controller mode charger and adapter applications. It operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CV/CC performance. The device integrates PWM controller to enhance the performance of Quasi Resonant (QR) mode flyback converters.

Startup Control

The V_{DD} pin of UTC **UPSR107** is connected to the line input through a resistor. A large value startup resistor can be used to minimize the power loss in application because the start current of UTC **UPSR107** is very low. When the V_{DD} voltage reaches UVLO(OFF), the internal startup circuit is disabled and the IC turns on.

Operating Current

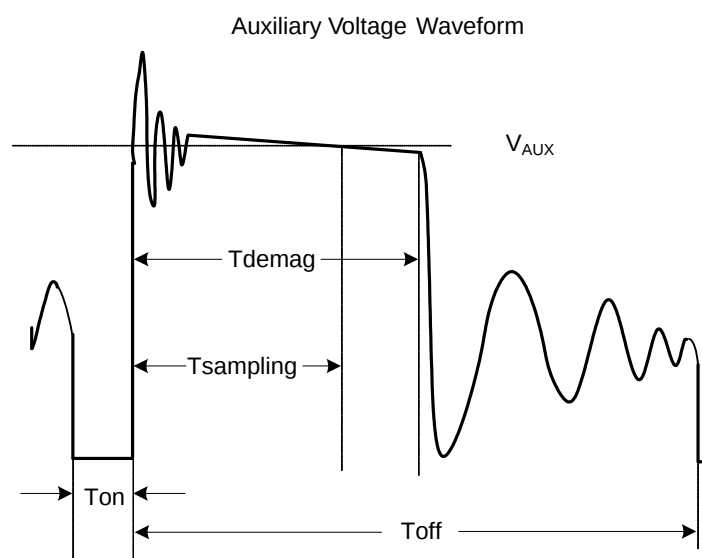
The Operating current of UTC **UPSR107** is as low as 1.0mA. Good efficiency and very low standby power can be achieved.

Constant Voltage Operation

The output voltage is defined by the transmission ratio between the secondary and auxiliary winding. The UTC **UPSR107** captures the auxiliary winding feedback voltage at FB pin and operates in constant-voltage (CV) mode to regulate the output voltage. The auxiliary voltage reflects the output voltage is given by:

$$V_{AUX} = \frac{N_A}{N_S} \times (V_O + \Delta V) \quad (1)$$

Where ΔV indicates the drop voltage of the output diode.



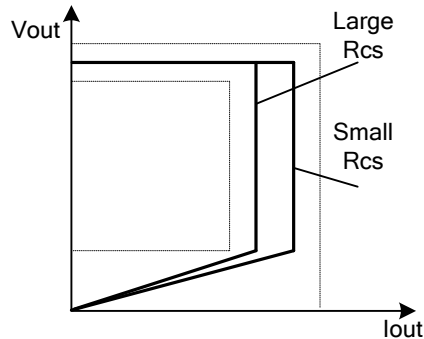
Via a resistor divider connected between the auxiliary winding and FB, the V_{AUX} is sampled at the $T_{sampling}$ end and it is hold until the next sampling. The sampled voltage is compared with 2.0V reference voltage and the error is amplified. The error amplifier output reflects the load condition and controls the T_{off} time and the I_{pk} to regulate the output voltage, thus constant output voltage can be achieved.

Constant Current Operation

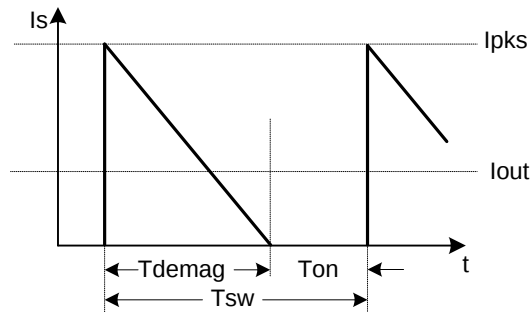
When the sampled voltage is below 2.0V reference voltage and the error amplifier output reaches its maximum, thus UTC **UPSR107** operates in constant-current (CC) mode. The CC point and maximum output power can be externally adjusted by external current sense resistor R_{cs} . The larger R_{cs} , the smaller CC point is, and the smaller output power becomes.

■ OPERATION DESCRIPTION (Cont.)

Adjustable Output Power By Changing Rcs



Secondary Current Waveform



In CC operation, the CC loop control function of UTC **UPSR107** will work in QR mode. Thus the output current is given by:

$$I_{pk} = \frac{500\text{mV}}{R_{CS}} \quad (2)$$

$$I_{out} = \frac{1}{2} \times \frac{N_p}{N_s} \times I_{pk} \quad (3)$$

Programmable Cable Drop Compensation

UTC **UPSR107** has a built-in cable voltage drop compensation to achieve good load regulation. An offset voltage is generated at FB pin by an internal current flowing into the resistor divider. The current is inversely proportional to the output load current. The voltage drop across the cable is compensated by this offset voltage at FB pin. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used.

Current Sensing and Leading Edge Blanking

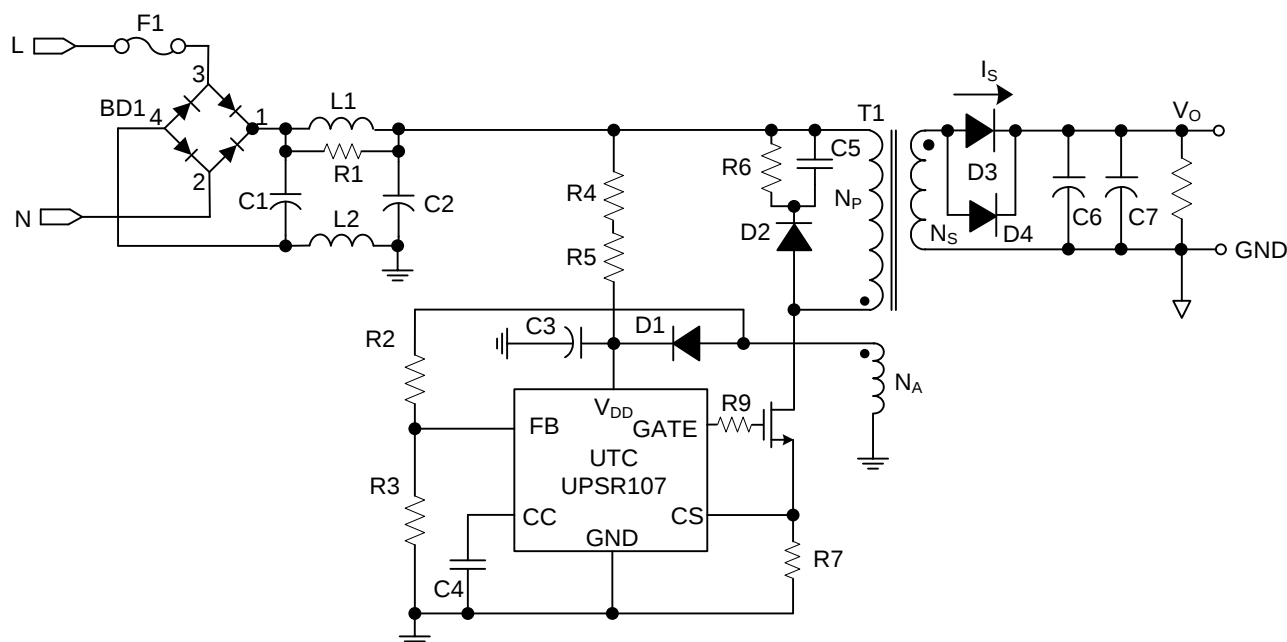
Cycle-by-cycle current limiting is offered in UTC **UPSR107**. The switch current is detected by a sense resistor into the CS pin. When the power switch is turned on, a turn-on spike will occur on this resistor. A 500ns leading-edge blanking is built in to avoid false-termination of the switching pulse so that the external RC filtering is no longer needed.

■ OPERATION DESCRIPTION (Cont.)**Protection Control**

Good power supply system reliability is achieved with its comprehensive protection features including V_{DD} over-voltage protection, V_{DD} Clamp, GATE Clamp, Power on soft start, Cycle-by-cycle current limiting, short circuit protection, leading edge blanking, OTP and UVLO, etc.

V_{DD} is supplied by transformer auxiliary winding output. The output of UTC **UPSR107** is shutdown when V_{DD} drops below UVLO(ON) and the power converter enters power on start-up sequence thereafter.

■ TYPICAL APPLICATION CIRCUIT (12V / 1.25A)



BOM

Reference	Component	Reference	Component
BD1	BD 1.5A/600V	R1	R 2.4KΩ 1206 ±5%
L1	500u H DR 6x8mm	R2	R 33KΩ 0805 ±1%
L2	4.7u H 1W	R3	R 4.3KΩ 0805 ±1%
C1	EC 10u F 400V 105°C	R4	R 1.5MΩ 1206 ±5%
C2	EC 22u F 400V 105°C	R5	R 1.5MΩ 1206 ±5%
C3	EC 4.7u F 50V 105°C	R6	R 200KΩ 1206 ±5%
C4	CC 10n F 50V 0805	R7	R 0.9Ω 1206 ±5%
C5	CC 1n F 1000V 1206	R8	R 2.7KΩ 1206 ±5%
C6	EC 680u F 16V 105°C Low-ESR	R9	R 30Ω 0805 ±5%
C7	EC 680u F 16V 105°C Low-ESR	Q1	N-MOSFET UTC 2N60
D1	Diode UTC 1N4007G	T1	EF-20
D2	Diode UTC 1N4007G	F1	FUSE 2A 250VAC
D3	Diode UTC SB3100		
D4	Diode UTC SB3100		

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.